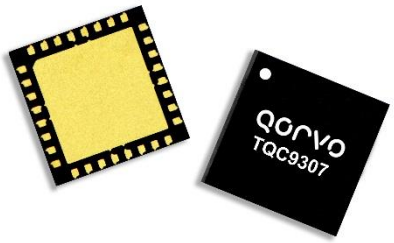
TQC9307

0.7 – 4.0 GHz Digital Variable Gain Amplifier

General Description

The TQC9307 is a digitally controlled variable gain amplifier (DVGA) with a broadband frequency range of 0.7 to 4.0 GHz. The DVGA features high linearity and low noise while providing digital variable gain with a 31 dB of range in 1 dB steps through a serial mode control interface. At 3.5 GHz, the DVGA typically provides 13.3 dB gain, +40.5 dBm OIP3, +21 dBm P1dB and 3.5 dB noise figure. This combination of performance parameters makes the DVGA ideal for receiver applications requiring gain control with high IIP3 and low noise figure. In addition, the DVGA integrates a shut-down biasing capability to allow for easy operation for TDD applications.

The TQC9307 integrates a high performance digital step attenuator followed by a high linearity, broadband gain block. Both stages are internally matched to 50 Ohms and do not require any external matching components. The TQC9307 is packaged in a RoHS-compliant, compact 5x5 mm surface-mount leadless package.

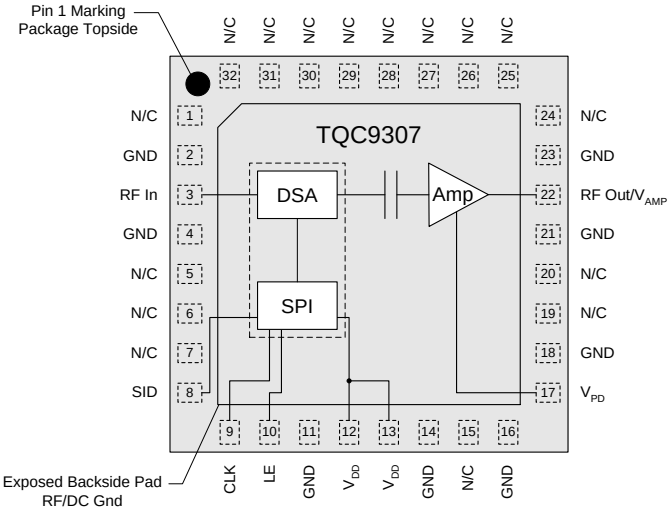


32 Pin 5X5 mm leadless SMT Package

Product Features

- Integrates DSA + Amp Functionality
- 0.7 – 4.0 GHz Broadband Performance
- 5-bit control, 31 dB range
- 13.3 dB Gain
- +20.6 dBm P1dB
- +27.7 dBm IIP3, +40.5 dBm OIP3
- Integrated on-chip matching, 50 ohm in/out
- Integrated shutdown control for TDD compatibility
- +5V Supply Voltage, 3.3V TTL logic compatible

Functional Block Diagram



Top View

Applications

- Wireless Infrastructure
- LTE / WCDMA / CDMA / GSM
- TDD or FDD systems
- General Purpose Wireless

Ordering Information

Part No.	Description
TQC9307-PCB	Evaluation Board
TQC9307TR13	2500pcs on a 13” reel

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-65 to 150 °C
RF Input Power, CW, 50Ω, 24 hr, 25°C	+22 dBm
V_{DD}, Power Supply Voltage	-0.3 to +5.5 V
Digital Input Voltage	-0.3 to V_{DD}+0.5 V

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V_{AMP}	+4.75	+5	+5.25	V
V_{DD}	+3		+5	V
T_{ch} (for >10^6 hours MTTF)			+190	°C
Case Temperature	-40		+105	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: V_{DD} = +5 V, Temp.=+25°C.

Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		0.7		4.0	GHz
Test Frequency			3.5		GHz
Gain	Max gain setting	11.5	13	14.5	dB
Gain Control Range			31		dB
Gain Control Step Size			1		dB
Gain Accuracy	3.3 – 3.8 GHz (major states)	± (0.3 + 10% of Atten. Setting)			dB
Input Return Loss			25		dB
Output Return Loss			13.5		dB
Output P1dB			+20.6		dBm
Output IP3	Pout/tone = 0 dBm, Δf = 1 MHz		+40.5		dBm
Input IP3	Pin/tone = -13 dBm, Δf = 1 MHz	+22	+27.7		dBm
Noise Figure	Max gain setting		3.5		dB
Amplifier Shutdown Control, V_{PD}	On state	0		0.8	V
	Off state (Power down)	2.1		V_{DD}	V
Shutdown pin current, I_{PD}	Off state		140		µA
Amplifier Current, I_{AMP} (pin 22)	On state	75	120	160	mA
	Off state (Power down)		3	8	mA
DSA Current, I_{DD} (pins 12, 13)			180		µA
Thermal Resistance (R_{th})	Channel to case		60		°C /W

1. Minimum specification listed is guaranteed by design. Not tested in production.
2. Input trace loss de-embedded from noise figure data.

Serial Control Interface

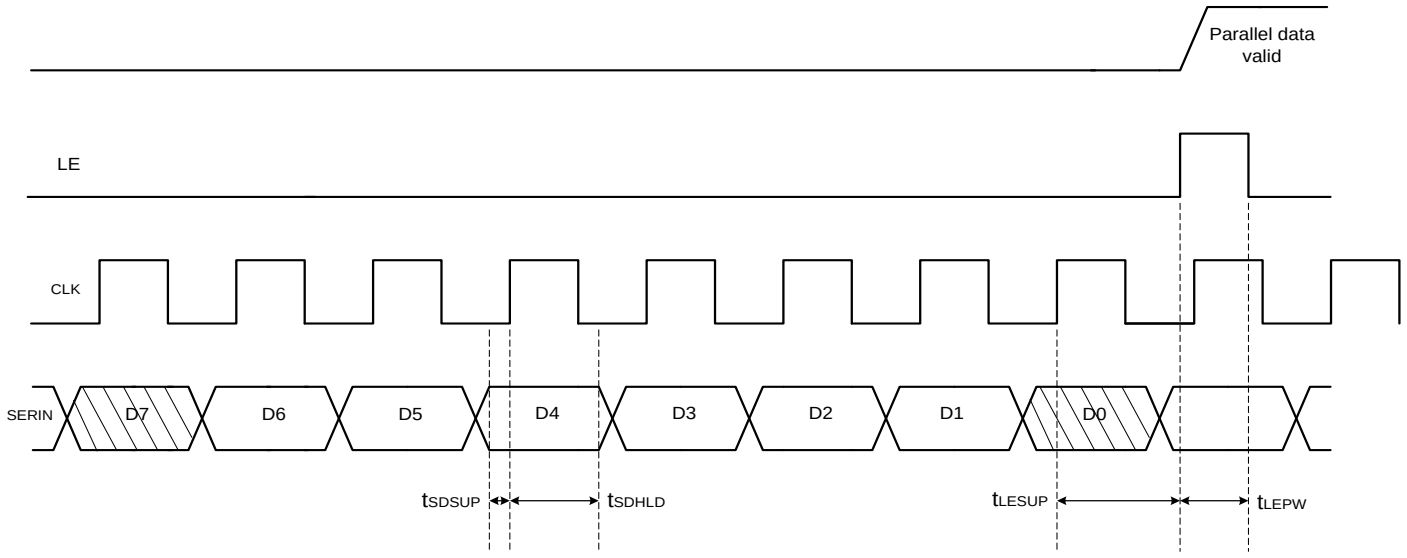
The TQC9307 has a CMOS SPI™ input compatible serial interface. This serial control interface converts the serial data input stream to parallel output word. The input is 3-wire (CLK, LE and SID) SPI™ input compatible. At power up, the serial control interface resets the DVGA to the minimum gain state (maximum attenuation setting). The 8-bit Serial Input Data (SID) word is loaded into the register on rising edge of the CLK, LSB first. When LE is high, CLK is internally disabled in the DVGA.

Serial Control Timing Characteristics (Test conditions: V_{DD} = +5 V, Temp.=25°C)

Parameter	Condition	Min	Max	Units
Clock Frequency	50% Duty Cycle		20	MHz
LE Setup Time, t_{LESUP}	after last CLK rising edge	5		ns
LE Pulse Width, t_{LEPW}		10		ns
SID set-up time, t_{SDSUP}	before CLK rising edge	5		ns
SID hold-time, t_{SDHLD}	after CLK rising edge	5		ns
Propagation Delay, t_{PLO}	LE to Parallel output valid	30		ns

Serial Control DC Logic Characteristics (Test conditions: V_{DD} = +5 V, Temp.=25°C)

Parameter	Condition	Min	Max	Units
Low State Input Voltage, V_{IL}		0	0.8	V
High State Input Voltage, V_{IH}		2.1	V_{DD}	V
Input Current, I_{IH} / I_{IL}	On SID, LE and CLK	-10	+10	µA



Serial Control Interface

Serial In Control Logic Truth Table, LSB in first

8-Bit Control Word								Attenuation
D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	Insertion loss
0	0	0	0	0	1	0	0	1 dB
0	0	0	0	1	0	0	0	2 dB
0	0	0	1	0	0	0	0	4 dB
0	0	1	0	0	0	0	0	8 dB
0	1	0	0	0	0	0	0	16 dB
0	1	1	1	1	1	0	0	31 dB
0	1	0	1	1	0	0	0	22 dB (example)

Note:

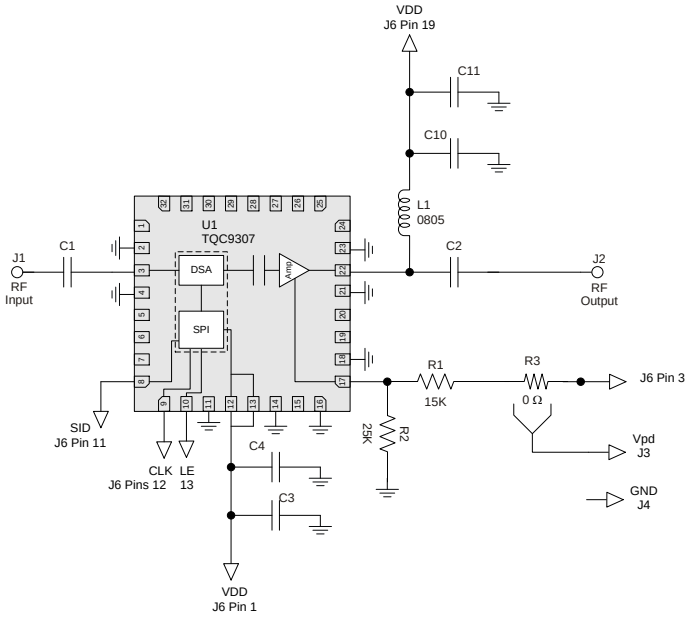
1) Bit D1 needs to be kept logic '0' to maintain the 1dB step for the DSA control.
2) Bits D0, D1 and D7 are 'don't care'.

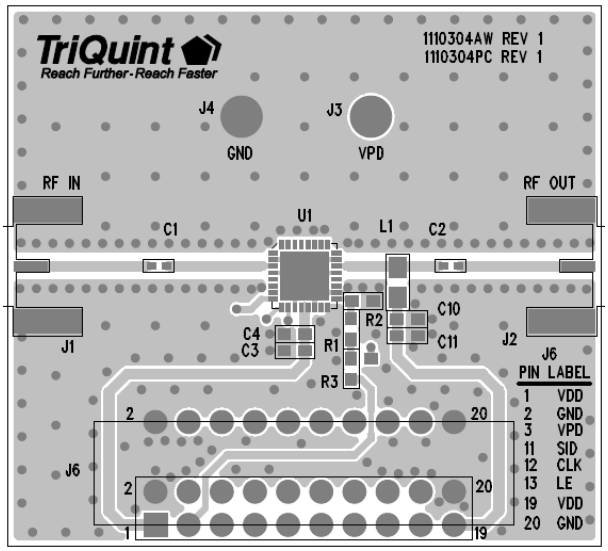
Performance Summary

Test conditions: T_{LEAD}=+25°C, V_{AMP} = V_{DD} =+5V

Frequency	900	1900	2600	3300	3500	3800	MHz
Gain	16.5	11.7	11.8	13	13.3	13.1	dB
Input Return Loss	21	9	12	20	30	13.6	dB
Output Return Loss	13	9	11.5	13	13.6	12.4	dB
Output P1dB	+16.7	+22.6	+21	+21.4	+20.6	+20.1	dBm
Output IP3 (Pout/tone=0dBm, Δf=1MHz)	+34.3	+38.5	+39	+40.5	+41.2	+40.8	dBm
Input IP3 (Pin/tone=-13dBm, Δf=1MHz)	+17.8	+27	+27.2	+27.5	+27.9	+27.7	dBm
Noise Figure		2.7	3.0	3.3	3.5	3.7	dB
Amplifier Current, I_{AMP}	126						mA

TQC9307-PCB Evaluation Board





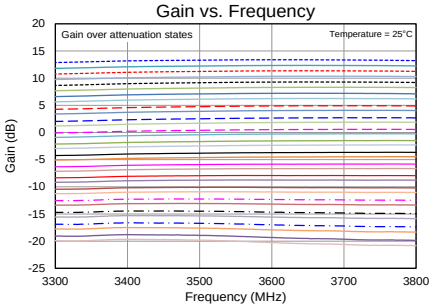
Bill of Material: TQC9307-PCB

Reference Desg.	Value	Description	Manufacturer	Part Number
U1	n/a	DVGA	Qorvo	TQC9307
C1	33 pF	Cap, chip, 0402	Various	
C2	100 pF	Cap, chip, 0402	Various	
C4, C10	1000pF	Cap, chip, 0402, 10%, 50V	Various	
C3, C11	1.0uF	Cap, chip, 0603, 10%, 10V	Various	
L1	22nH	Ind, coil, 5%, 0603	Coilcraft	0603CS-22NXJL
R1	15K	Res, chip, 0603, 5%, 1/16W	Various	
R2	25K	Res, chip, 0603, 5%, 1/16W	Various	
R3	0 Ω	Res, chip, 0603, 5%, 1/16W	Various	

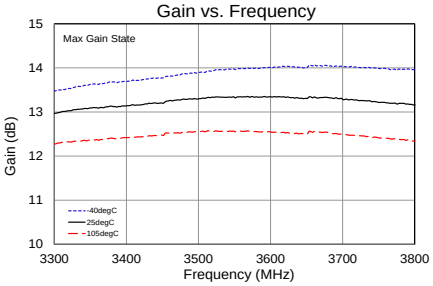
Performance Plots

Test conditions: $V_{AMP} = V_{DD} = +5V$

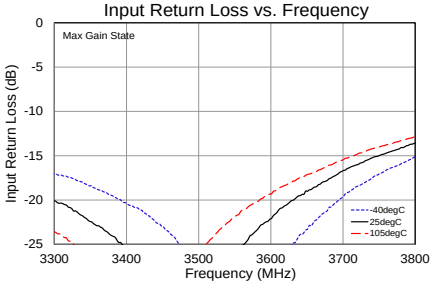
Gain vs. Frequency



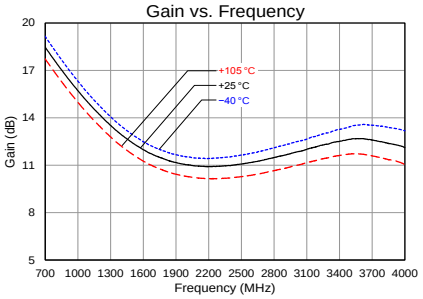
Gain vs. Frequency



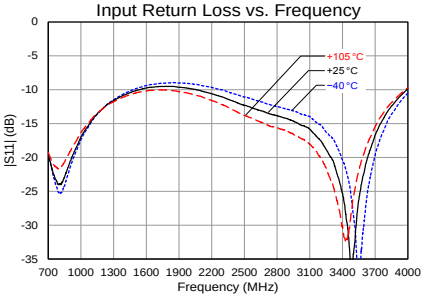
Input Return Loss vs. Frequency



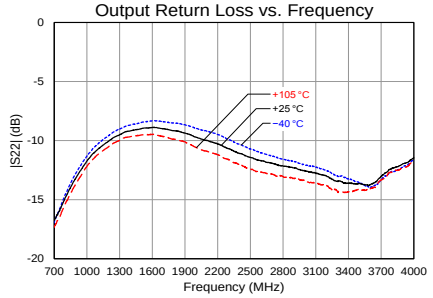
Gain vs. Frequency



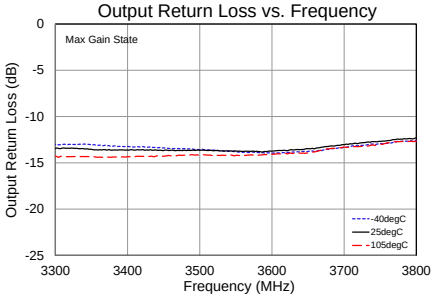
Input Return Loss vs. Frequency



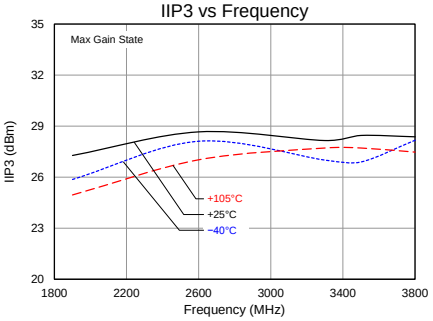
Output Return Loss vs. Frequency



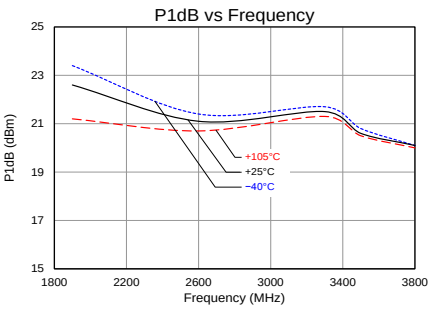
Output Return Loss vs. Frequency



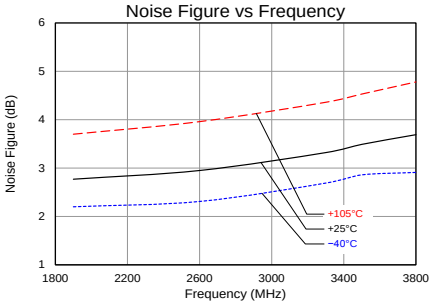
IIP3 vs Frequency



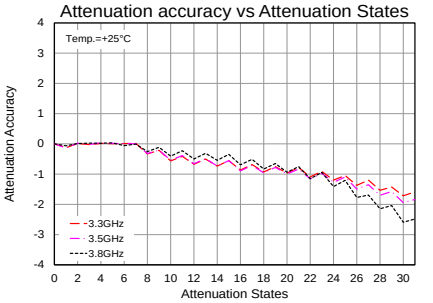
P1dB vs Frequency



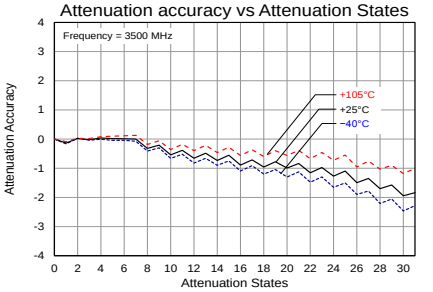
Noise Figure vs Frequency



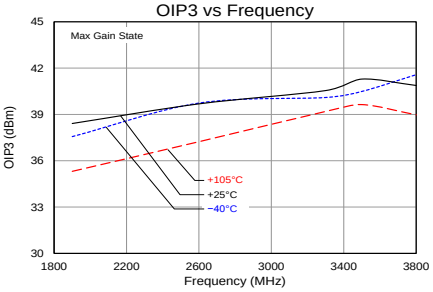
Attenuation accuracy vs Attenuation States



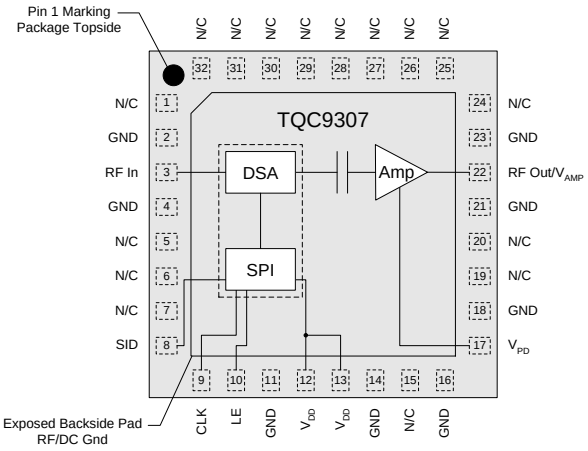
Attenuation accuracy vs Attenuation States



OIP3 vs Frequency



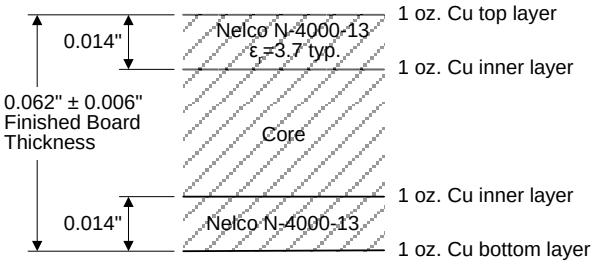
Pin Configuration and Description



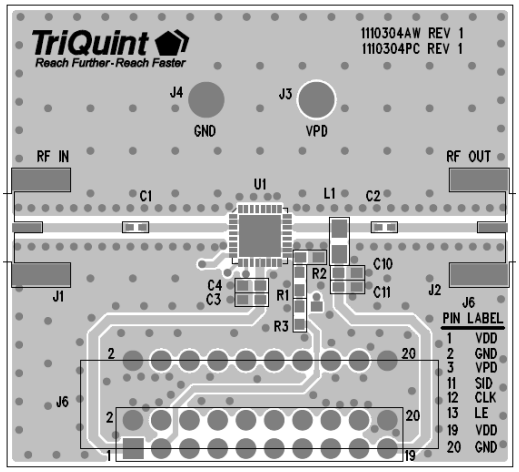
Pin No.	Label	Description
1, 5, 6, 7, 15, 19, 20, 24-32	N/C	No internal connection but can be grounded
2, 4, 11, 14, 16, 18, 21, 23	GND	DC/RF ground connection
3	RF In	RF input. Does not need a DC block capacitor if the input signal is DC free.
8	SID	Serial data input
9	CLK	Clock signal in
10	LE	Latch Enable pin
12, 13	V_{DD}	DC Supply Voltage for SPI and DSA. Pins are internally tied together
17	V_{PD}	Amplifier power down control pin. A 20K shunt resistor needs to be placed at this pin.
22	RF Out / V_{AMP}	RF output and DC bias for amplifier. Needs to be capacitively coupled
Backside Pad	RF/DC Ground	Ground connection for proper thermal dissipation

Evaluation Board Material Information

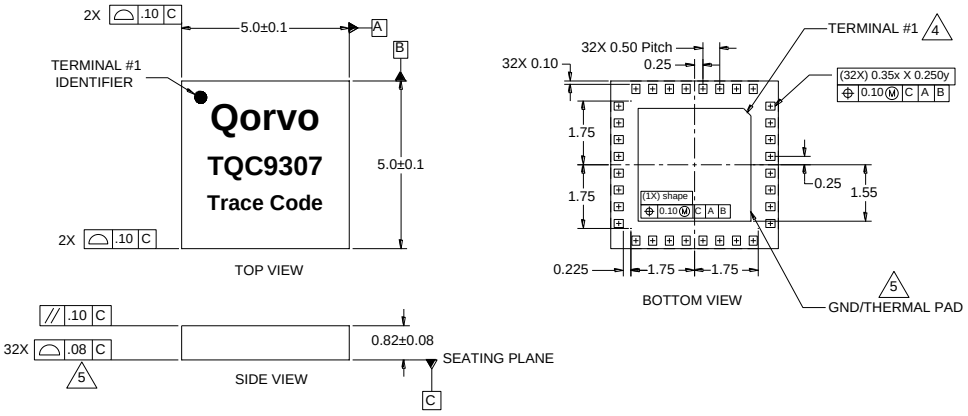
Qorvo PCB 1110304 Material and Stack-up



50 ohm line dimensions: width = .026”, spacing = .032”.



Package Marking and Dimensions

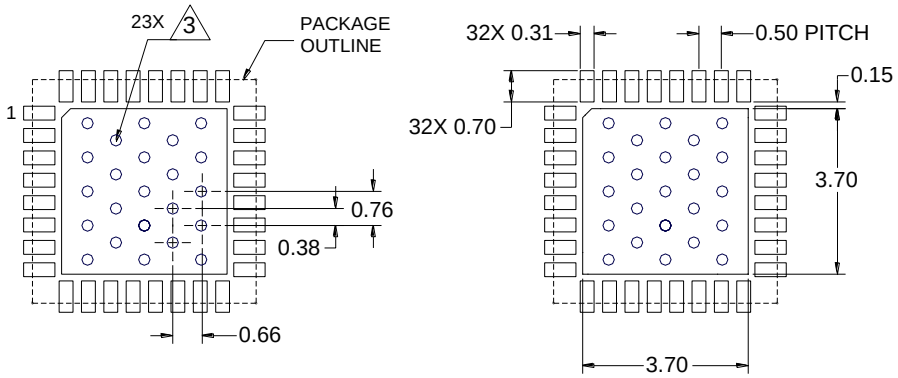


Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.
4. Co-planarity applies to the exposed ground/thermal pad as well as the contact pins.

PCB Mounting Pattern

All dimensions are in millimeters (inches). Angles are in degrees.



COMPONENT SIDE

Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25mm (0.10").
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1C	ESDA / JEDEC JS-001-2014
ESD – Charged Device Model (CDM)	Class C3	ESDA / JEDEC JS-002-2014
MSL – Moisture Sensitivity Level	Level 3	IPC/JEDEC J-STD-020

Caution!
ESD-Sensitive Device

Solderability

Compatible with lead-free (260°C max. reflow temp.) soldering process.
Solder profiles available upon request.

Contact plating: Electrolytic plated Au over Ni.

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

For technical questions and application information: **Email:** appsupport@qorvo.com

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