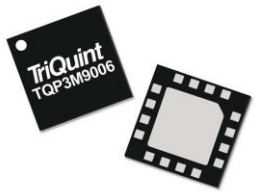
TQP3M9006

High Linearity LNA Gain Block

Applications

- Repeaters
- Mobile Infrastructure
- LTE / WCDMA / CDMA / EDGE
- General Purpose Wireless

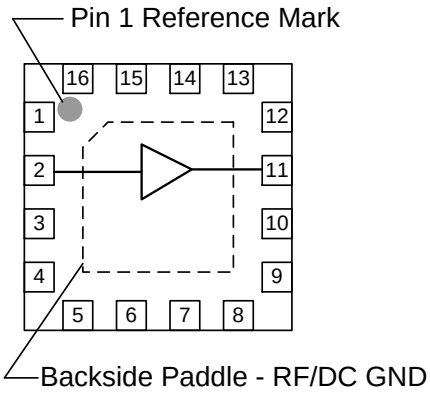


16-Pin 3 x 3 mm QFN Package

Product Features

- 500 – 4000 MHz
- 13.5 dB Gain at 1.9 GHz
- 1.0 dB Noise Figure at 1.9 GHz
- +38.5 dBm Output IP3
- +22.4 dBm P1dB
- 50 Ohm Cascadable Gain Block
- Unconditionally Stable
- High Input Power Capability
- +5 V Single Supply, 90 mA Current
- 3 x 3 mm QFN Package

Functional Block Diagram



General Description

The TQP3M9006 is a high linearity low noise gain block amplifier in a low-cost surface-mount package. At 1.9 GHz, the amplifier typically provides 13.5 dB gain, +38.5 dBm OIP3, and 1.2 dB Noise Figure while only drawing 90 mA current. The device is housed in a leadfree / green / RoHS-compliant industry-standard 16-pin 3 x 3 mm QFN package.

The TQP3M9006 has the benefit of having high linearity while also providing very low noise across a broad range of frequencies. This allows the device to be used in both receive and transmit chains for high performance systems. The amplifier is internally matched using a high performance E-pHEMT process and only requires an external RF choke and blocking/bypass capacitors for operation from a single +5 V supply. The internal active bias circuit also enables stable operation over bias and temperature variations.

The TQP3M9006 covers the 0.5 – 4 GHz frequency band and is targeted for wireless infrastructure or other applications requiring high linearity and/or low noise figure.

Pin Configuration

Pin No.	Label
2	RF Input
11	RF Output / V_{DD}
All Other Pins	N/C or GND
Backside Paddle	GND

Ordering Information

Part No.	Description
TQP3M9006	High Linearity LNA Gain Block
TQP3M9006-PCB	0.5 – 4 GHz Evaluation Board

Standard T/R size = 2500 pieces on a 7” reel

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−55 to 150 °C
RF Input Power, CW, 50Ω, T=25°C	+20 dBm
Device Voltage (V_{DD})	+7 V

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Device Voltage (V_{DD})	+3.0	+5.0	+5.25	V
T_{CASE}	−40		+85	°C
Tj for >10^6 hours MTTF			+190	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

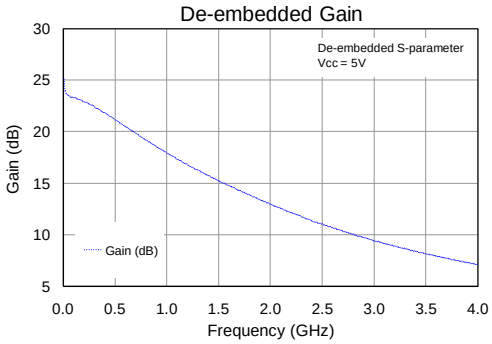
Electrical Specifications

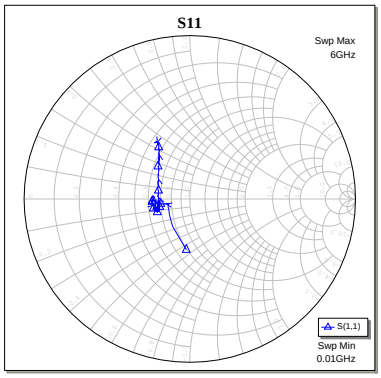
Test conditions unless otherwise noted: V_{DD}=+5 V, Temp=+25 °C, 50 Ω system

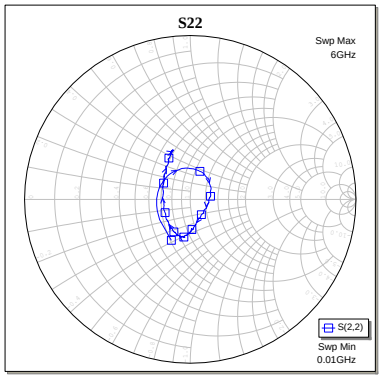
Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		500		4000	MHz
Test Frequency			1900		MHz
Gain		12	13.5	15	dB
Input Return Loss			13		dB
Output Return Loss			19		dB
Output P1dB			+22.4		dBm
Output IP3	See Note 1.	+35	+38.5		dBm
Noise Figure			1.0		dB
Current, I_{DD}		68	90	112	mA
Thermal Resistance, θ_{jc}	Junction to case		54.5		°C/W

Notes:
1. OIP3 is measured with two tones at an output power of 4 dBm / tone separated by 1 MHz. The suppression on the largest IM3 product is used to calculate the OIP3 using 2:1 rule. 2:1 rule gives relative value with respect to fundamental tone.

Device Characterization Data





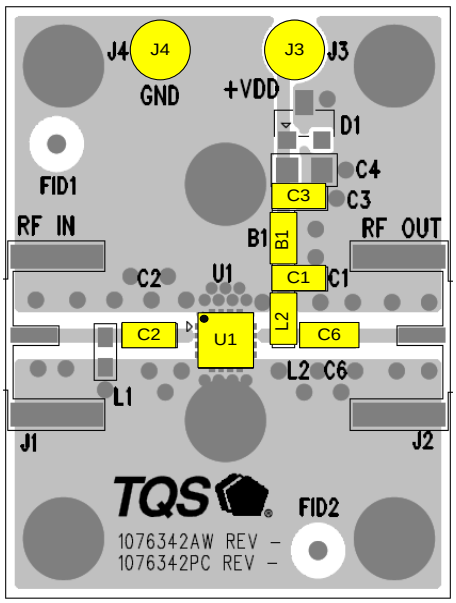


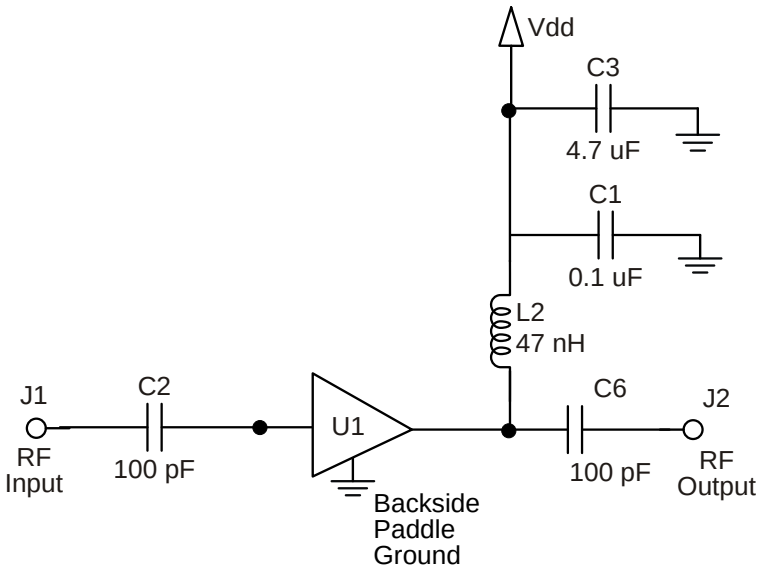
S-Parameters

Test Conditions: V_{DD}=+5 V, I_{DD}=90 mA, T=+25 °C, 50 ohm system, calibrated to device leads

Freq (MHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)
50	−16.84	−151.32	23.531	168.18	−28.093	6.4819	−13.835	−175.95
100	−17.401	−164.51	23.315	165.29	−28.064	6.2924	−14.006	164.09
200	−17.287	−168.02	22.903	156.16	−27.93	10.039	−14.114	138.62
400	−16.259	−169.15	21.851	138.35	−27.459	17.79	−14.288	101.29
800	−14.058	−173.2	19.184	111.93	−25.857	30.27	−15.59	50.117
1000	−13.461	−175.46	17.931	102.1	−24.902	33.496	−16.791	30.427
1200	−13.096	−177.29	16.795	93.532	−23.936	36.097	−18.092	9.8602
1500	−12.757	−177.2	15.241	81.983	−22.616	37.018	−19.269	−24.674
1900	−12.718	−173.31	13.397	68.817	−21.104	36.304	−18.018	−60.918
2000	−12.97	−172.34	12.969	65.789	−20.821	36.102	−17.678	−67.922
2200	−13.043	−169.97	12.161	60.064	−20.183	34.744	−16.05	−77.206
2500	−13.062	−163.57	11.043	52.376	−19.352	32.905	−14.575	−88.454
2600	−13.221	−163	10.671	49.934	−19.117	32.135	−14.005	−90.198
3000	−13.475	−157.55	9.3978	40.398	−18.141	28.959	−12.674	−99.96
3500	−14.256	−162.42	8.1567	28.943	−17.037	24.266	−12.843	−111.14
4000	−14.52	178.56	7.1124	16.613	−16.013	16.846	−14.488	−134.94

Application Circuit Configuration





Notes:
1. See PC Board Layout, under Applications Information section, for more information.
2. Components shown on the silkscreen but not on the schematic are not used.
3. B1 (0 Ω jumper) may be replaced with copper trace in the target application layout.

Bill of Material – TQP3M9006-PCB

Reference Designation	Value	Description	Manufacturer	Part Number
U1		High Linearity LNA Gain Block	TriQuint	TQP3M9006
C2, C6	100 pF	Cap, Chip, 0603, 50V, NPO, 5%	various	
C1	0.1 µF	Cap, Chip, 0603, 16V, X7R, 10%	various	
L2	47 nH	Ind, Chip, 0603, 5%	various	
C3	4.7 µF	Cap, Chip, 0603, 6.3V, X5R, 20%	various	
B1	0 Ω	Res, Chip, 0603, 1/16W, 5%	various	
L1, D1, C4	Do Not Place	Cap, Chip, 0603, 50V, NPO, 5%	various	

Typical Performance – TQP3M9006-PCB

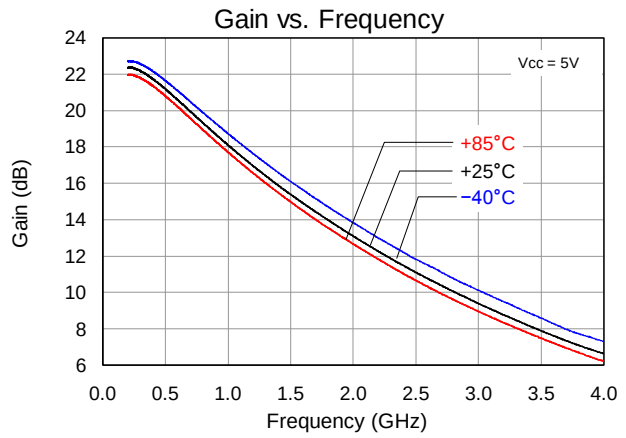
Test conditions unless otherwise noted: V_{DD}=+5V, I_{DD}=90 mA, Temp=+25°C, 50 Ω system.

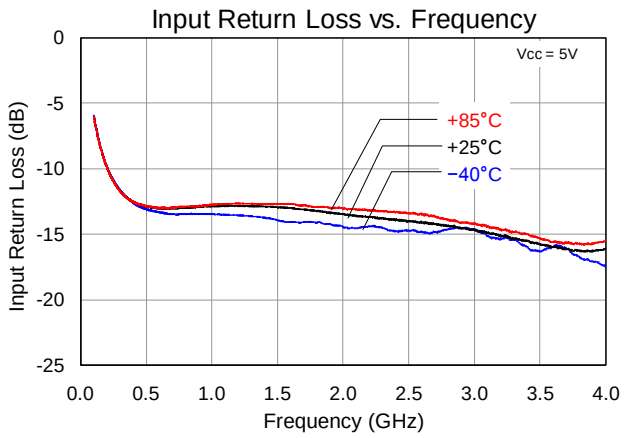
Parameter	Typical Value				Units
Frequency	500	900	1900	2600	MHz
Gain	21.2	18.7	13.5	10.7	dB
Input Return Loss	13	13	13	14	dB
Output Return Loss	10	14	19	15	dB
Output P1dB	+22.3	+22.3	+22.4	+22.6	dBm
OIP3 (1)	+36.8	+37.3	+38.5	+38.9	dBm
Noise figure (2)	1.0	1.1	1.0	1.5	dB

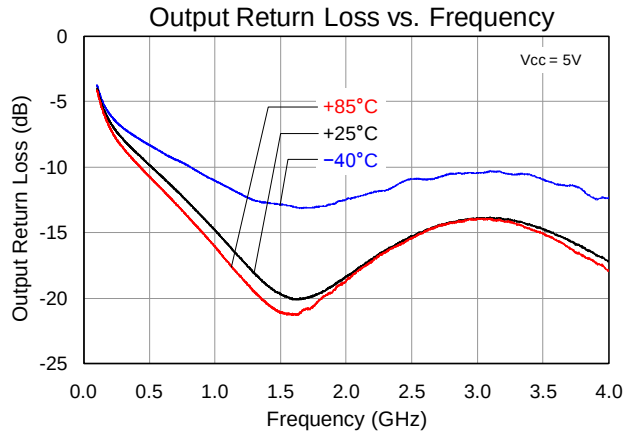
Notes:
1. OIP3 measured with two tones at an output power of +4 dBm / tone separated by 1 MHz. The suppression on the largest IM3 product is used to calculate the OIP3 using 2:1 rule.
2. Noise figure data shown in the table above is measured on evaluation board and corrected for the board loss of around 0.13 dB at 1.9 GHz.

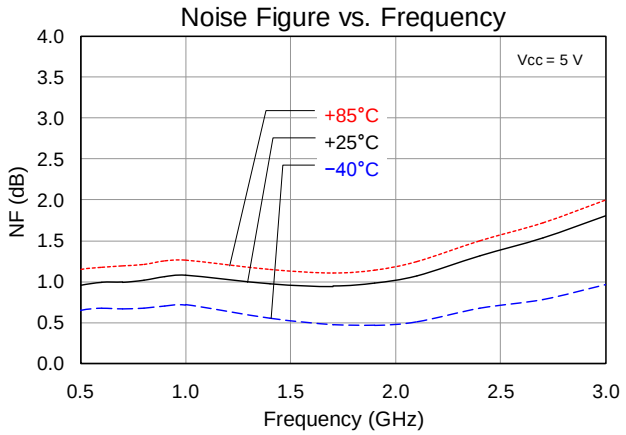
Performance Plots – TQP3M9006-PCB

Test conditions unless otherwise noted: V_{DD}=+5 V, I_{DD}=90 mA, Temp=+25°C, 50 Ω system.



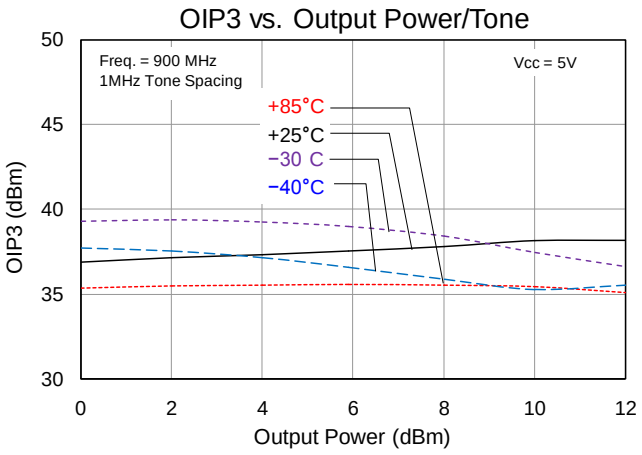


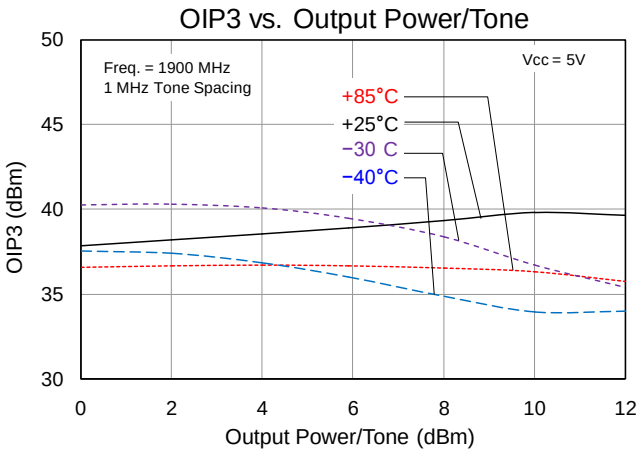


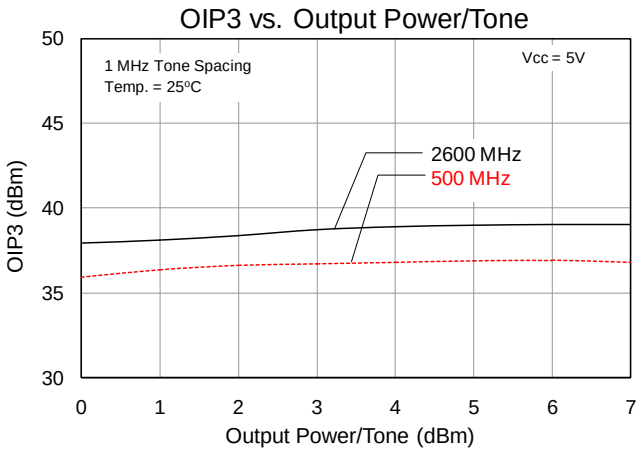


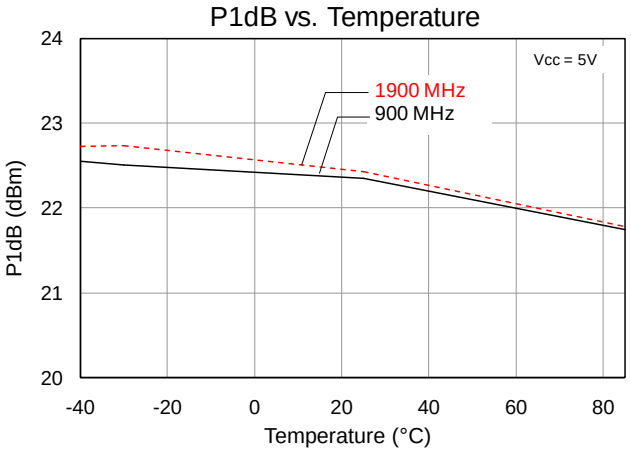
Performance Plots – TQP3M9006-PCB

Test conditions unless otherwise noted: V_{DD}=+5 V, I_{DD}=90 mA, Temp=+25°C, 50 Ω system.

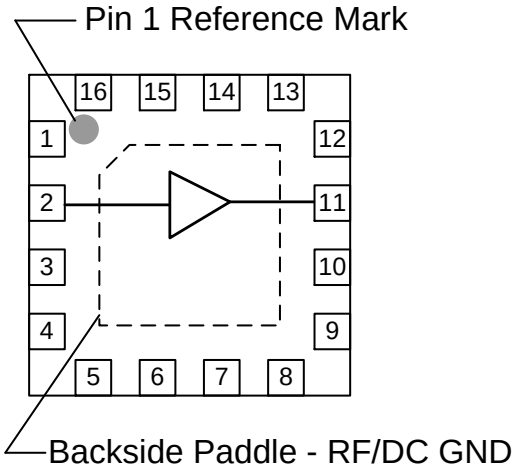








Pin Configuration and Description



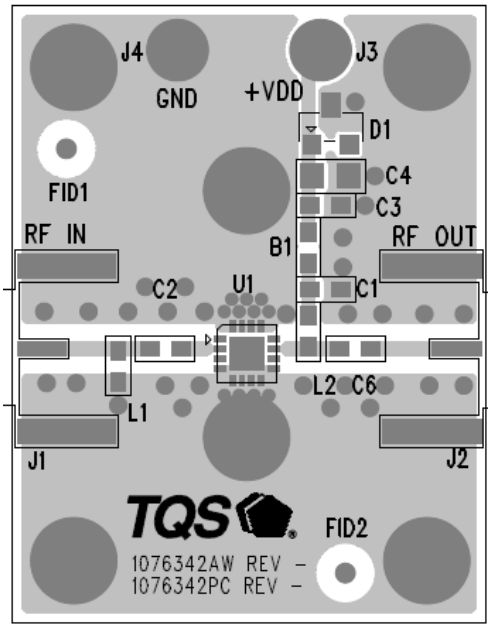
Pin No.	Label	Description
2	RF Input	Input, matched to 50 ohms. External DC Block is required.
11	V_{DD} / RF_{OUT}	Output, matched to 50 ohms, External DC Block is required and supply voltage.
All other pins	GND	These pins are not connected internally but are recommended to be grounded on the PCB for optimal isolation.
	GND Paddle	Backside Paddle. Multiple vias should be employed to minimize inductance and thermal resistance; see page 7 for mounting configuration.

Applications Information

Top RF layer is .014" NELCO N4000-13, ϵ_r = 3.9, 4 total layers (0.062" thick) for mechanical rigidity. Metal layers are 1-oz copper. 50 ohm Microstrip line details: width = .029", spacing = .035"

The pad pattern shown has been developed and tested for optimized assembly at TriQuint Semiconductor. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

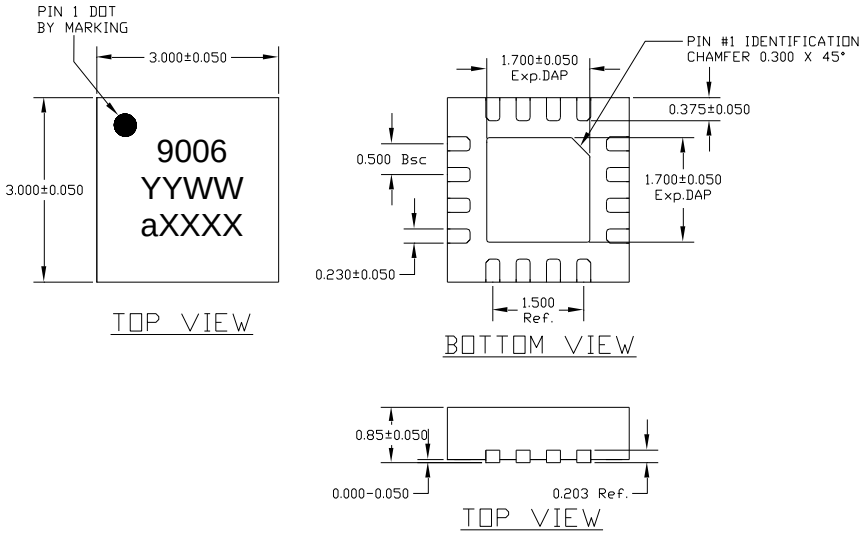
For further technical information, Refer to www.TriQuint.com



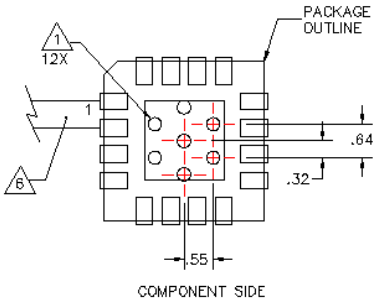
Package Marking and Dimensions

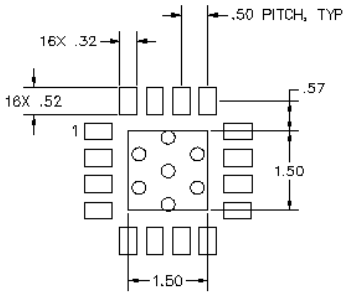
This package is lead-free/RoHS-compliant. The plating material on the leads is annealed matte tin. It is compatible with both lead-free (maximum 260 °C reflow temperature) and lead (maximum 245 °C reflow temperature) soldering processes.

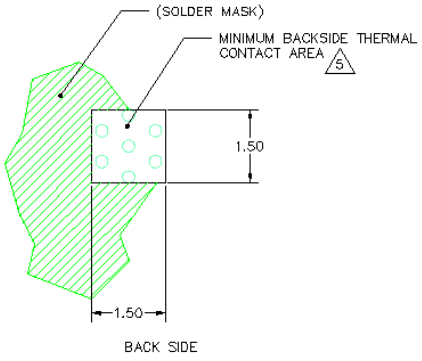
The component will be marked with a "9006" designator with an alphanumeric lot code on the top surface of package.



PCB Mounting Pattern







NOTES:

1. GROUND/THERMAL VIAS ARE CRITICAL FOR THE PROPER PERFORMANCE OF THIS DEVICE. VIAS SHOULD USE A .35mm (#80/.0135") DIAMETER DRILL AND HAVE A FINAL, PLATED THRU DIAMETER OF .25mm (.010").
2. ADD AS MUCH COPPER AS POSSIBLE TO INNER AND OUTER LAYERS NEAR THE PART TO ENSURE OPTIMAL THERMAL PERFORMANCE.
3. TO ENSURE RELIABLE OPERATION, DEVICE GROUND PADDLE-TO-GROUND PAD SOLDER JOINT IS CRITICAL.
4. ADD MOUNTING SCREWS NEAR THE PART TO FASTEN THE BOARD TO A HEATSINK. ENSURE THAT THE GROUND/THERMAL VIA REGION CONTACTS THE HEATSINK.
5. DO NOT PUT SOLDER MASK ON THE BACK SIDE OF THE PC BOARD IN THE REGION WHERE THE BOARD CONTACTS THE HEATSINK.
6. RF TRACE WIDTH DEPENDS UPON THE PC BOARD MATERIAL AND CONSTRUCTION.
7. USE 1 OZ. COPPER MINIMUM.
8. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.

Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35mm (#80 / .0135") diameter drill and have a final plated thru diameter of .25 mm (.010").
3. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.

Product Compliance Information

ESD Sensitivity Ratings

Caution! ESD-Sensitive Device

ESD Rating: Class 1A
Value: ≥ 250 V to < 500 V
Test: Human Body Model (HBM)
Standard: JEDEC Standard JS-001-2012

ESD Rating: Class C3
Value: ≥ 1000 V
Test: Charged Device Model (CDM)
Standard: JEDEC Standard JESD22-C101F

MSL Rating

MSL Rating: Level 1
Test: 260 °C convection reflow
Standard: JEDEC Standard IPC/JEDEC J-STD-020

Solderability

Compatible with both lead-free (260°C maximum reflow temperature) and tin/lead (245°C maximum reflow temperature) soldering processes.

Contact plating: Annealed Matte Tin

RoHs Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

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