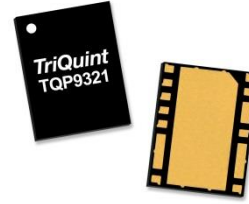


General Description

The TQP9321 is a high-efficiency, two-stage power amplifier with integrated bias and temperature control circuits in a low-cost surface-mount package. This 0.5 watt power amplifier is ideal for small cell base station applications.

TQP9321 provides high gain (30 dB) and +27 dBm linear power with pre-distortion correction over the 1.8 – 2.2 GHz frequency range for bands 1, 2, 3, 4, 10 and 25. With pre-distortion, the amplifier is able to achieve –50 dBc ACLR at +27 dBm output power using an LTE signal.

The TQP9321 integrates two high performance amplifier stages to allow for a compact system design and requires very few external components for operation. The amplifier is bias adjustable allowing the amplifier's power consumption to be optimized for specific applications. The TQP9321 is available in a lead-free/RoHS-compliant 3.5 x 4.5 mm surface mount package and is pin-compatible to the 0.7 – 1.0 GHz TQP9309 and 2.5 – 2.7 GHz TQP9326.

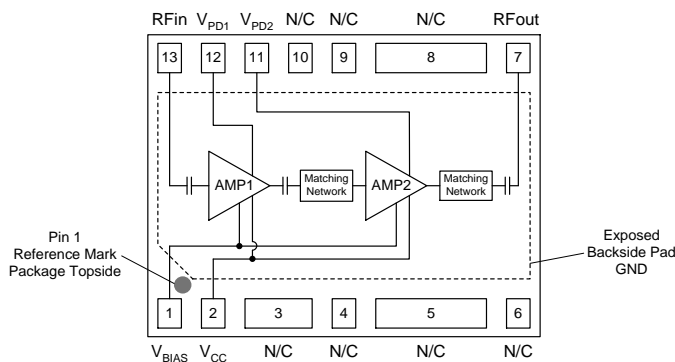


3.5 x 4.5 mm Leadless SMT Package

Product Features

- Frequency Range: 1.8 – 2.17 GHz
- Covers Multiple Bands with One Component
- Fully Integrated, 2-Stage Power Amplifier
- Internally Matched 50 Ω Input/Output
- ACLR: –50 dBc ACLR at $P_{avg} = +27$ dBm
- Gain: 30 dB
- High Efficiency: 27% at +27 dBm
- Quiescent Current: 110 mA
- Integrated Bias Control and Temp. Comp Circuit
- Single Supply Voltage: +5 V
- Lead-free / RoHS compliant
- POE Capable

Functional Block Diagram



Applications

- Small Cell / Picocell
- Enterprise Femtocell
- Bands 1, 2, 3, 4, 10 and 25

Ordering Information

Part No.	Description
TQP9321	0.5 W Small Cell PA
TQP9321-PCB	Evaluation board

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-40 to 150 °C
Supply Voltage (V _{CC})	+6 V
RF Input Power, CW, 50 Ω, T=25 °C	+10 dBm

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V _{DD}		+5		V
T _{AMB}	-40	25	+85	°C
T _j for >10 ⁶ hours MTTF			+175	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: V_{CC} = +5 V, V_{PD1} = V_{PD2} = +5 V, Temp. = +25 °C.

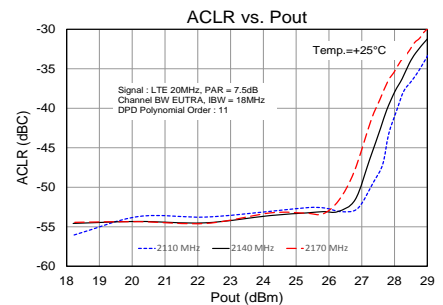
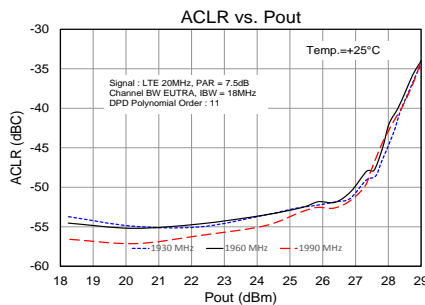
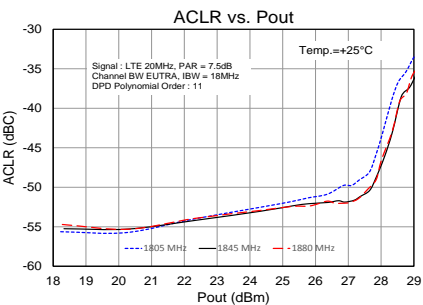
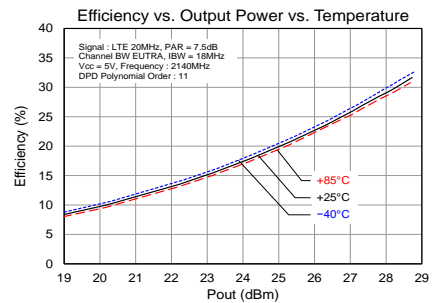
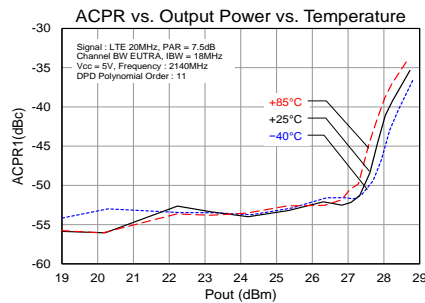
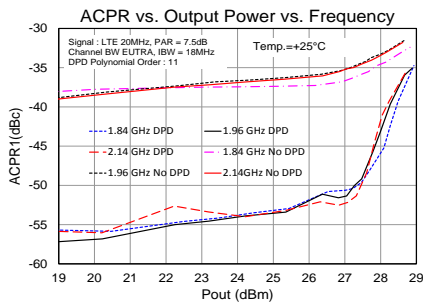
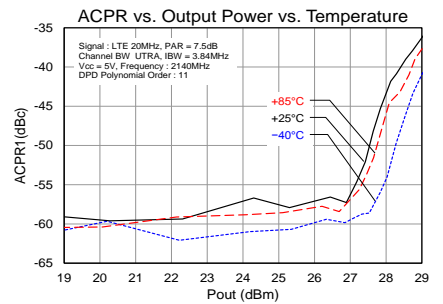
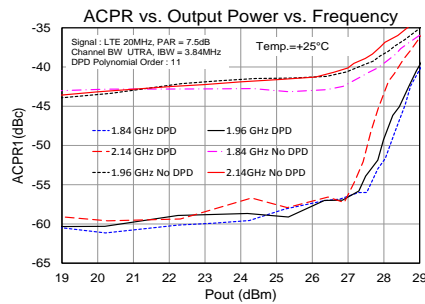
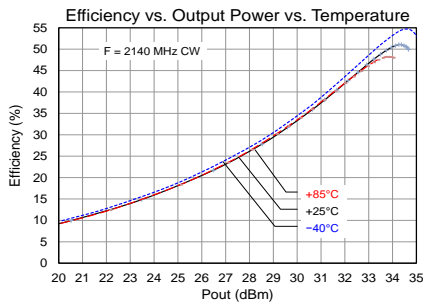
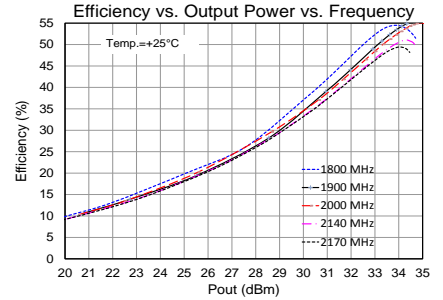
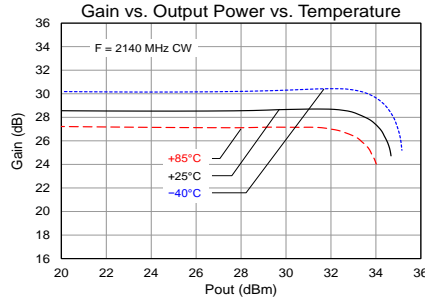
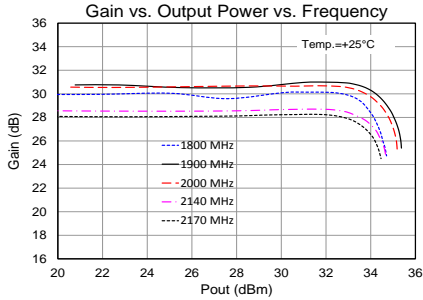
Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		1800		2170	MHz
Output Channel Power			+27		dBm
Gain	1805 – 1880 MHz	28.1	30		dB
	1930 – 1990 MHz	27.1	29		dB
	2110 – 2170 MHz	27.1	29	30.8	dB
Gain Temperature Coefficient			-0.024		dB/°C
ACLR Uncorrected	See note 1		-35		dBc
ACLR Corrected	See note 1		-50		dBc
Power Added Efficiency	1805 – 1880 MHz, See note 1		29		%
	1930 – 1990 MHz, See note 1		28		%
	2110 – 2170 MHz, See note 1		27		%
Output P3dB	1805 – 1880 MHz	+33.6	+34.7		dBm
	1930 – 1990 MHz	+33.6	+34.7		dBm
	2110 – 2170 MHz	+33.6	+34.7		dBm
P3dB Temperature Coefficient			-0.008		dBm/°C
Noise Figure			3.5		dB
Quiescent Current, I _{CQ}		90	110	136	mA
Reference Current, I _{PD}			2		mA
Operational Current, I _{CC}	P _{out} = +27 dBm		340		mA
VSWR Survivability	P _{out} = +26 dBm Signal : WCDMA 1C, PAR = 8 dB	10:1			–
Thermal Resistance, θ _{jc}	Module (junction to case)		27		°C/W

Notes:

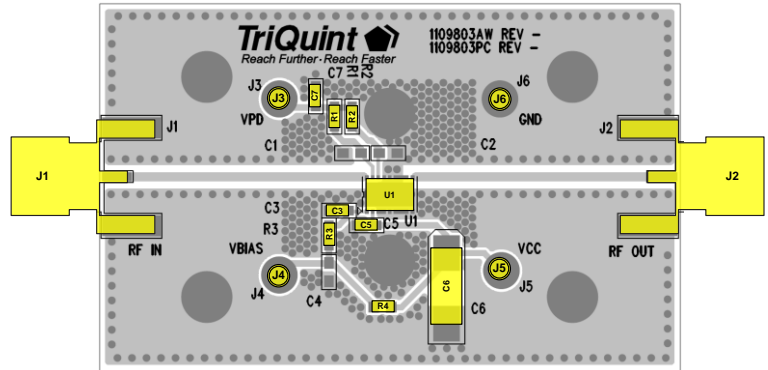
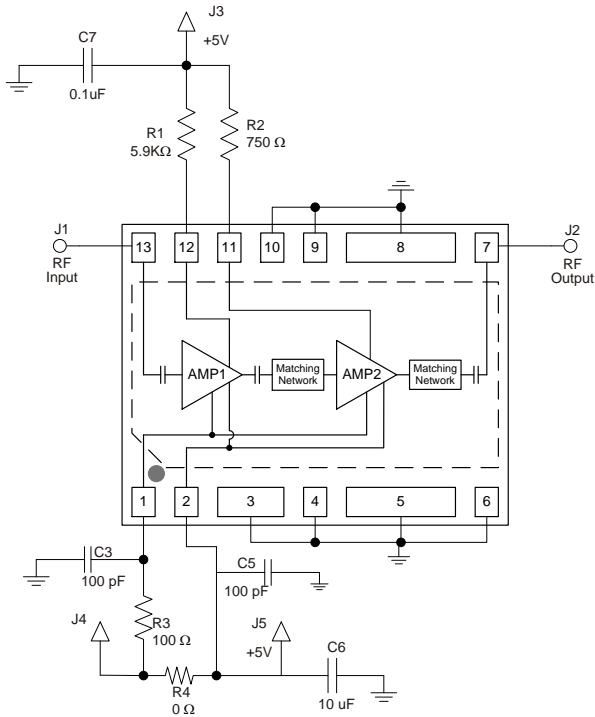
- Using LTE signal, 20 MHz/Carrier, IBW = 18.02 MHz, PAR 7.5 dB, P_{out} = +27 dBm.
- Items in min/max columns in bold at guaranteed by production test at 2.14 GHz.
- Items in min/max columns that are not a bold font are guaranteed by design characterization.

Performance Plots

Test conditions unless otherwise noted: $V_{CC} = +5V$, $V_{pd} = +5V$, $Temp = +25^{\circ}C$



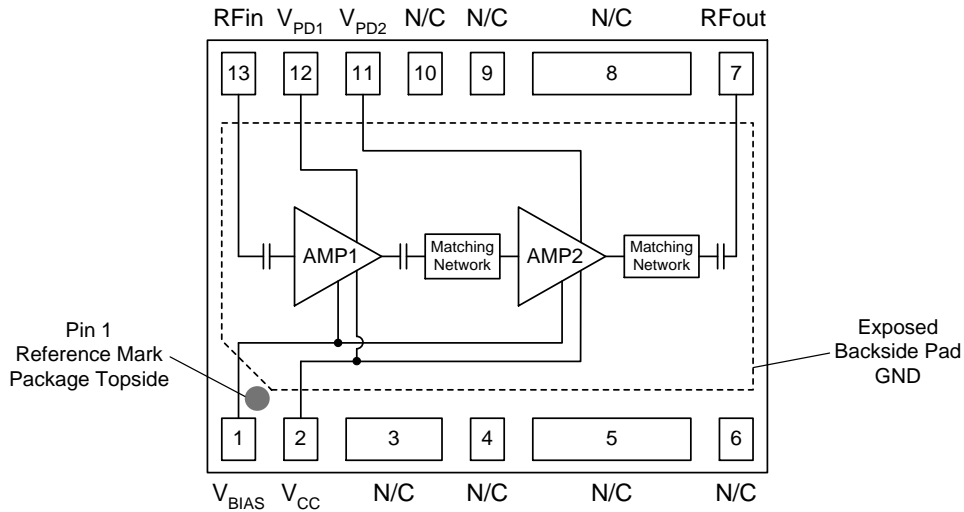
TQP9321-PCB Evaluation Board



Bill of Material TQP9321-PCB

Ref Des	Value	Description	Manuf.	Part Number
n/a	n/a	Printed Circuit Board		1109803
U1	n/a	High Efficiency 2-stage PA	TriQuint	TQP9321
R4	0 Ω	Resistor, Chip, 0603, 5%	various	
R3	100 Ω	Resistor, Chip, 0603, 1%	various	
C7	0.1 uF	Capacitor, Chip, 0603, 5%	various	
C6	10 uF	Capacitor, Chip, 6032, 10%, Tantalum	various	
C3, C5	100 pF	Capacitor, Chip, 0603, NPO/COG, 5%	various	
R2	750 Ω	Resistor, Chip, 0603, 5%, 1/16W	various	
R1	5.9 kΩ	Resistor, Chip, 0603, 5%, 1/16W	various	
C1, C2, C4		Do Not Place		

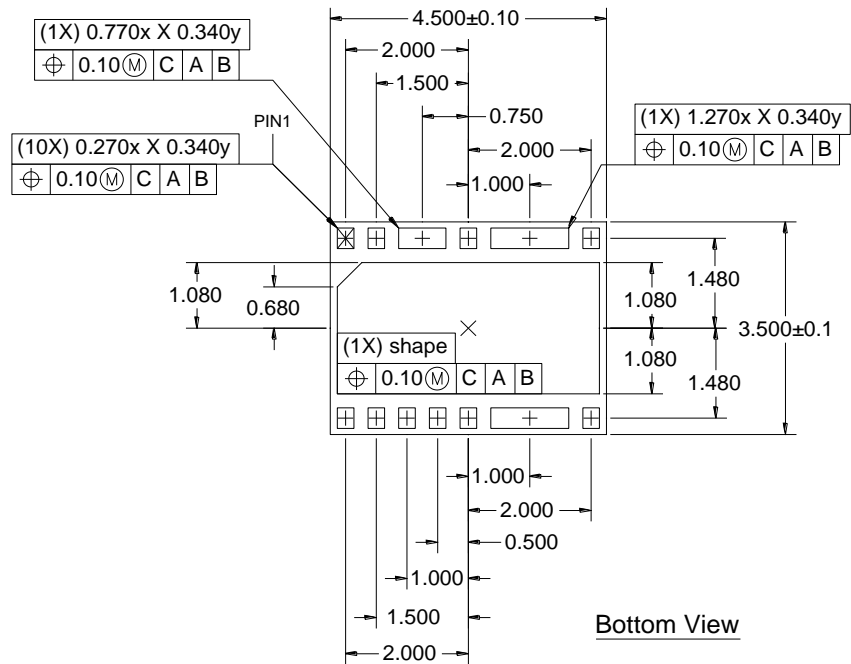
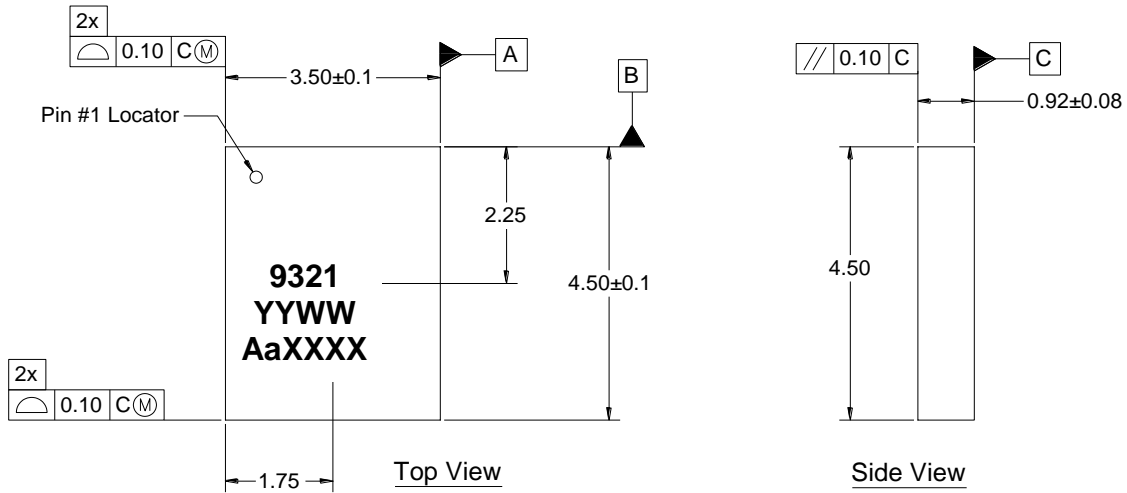
Pin Configuration and Description



Pin No.	Label	Description
1	V_{BIAS}	Provides reference voltage for internal active biasing circuit
2	V_{CC}	DC voltage supply connection
3, 4, 5, 6, 8, 9, 10	GND/NC	No internal connection. Provide grounded land pads for PCB mounting integrity.
7	RFout	RF output pin. The DC is internally blocked at this pin.
11	V_{PD2}	Power down for Amp 1. This voltage adjusts for the current draw in Amp 1.
12	V_{PD1}	Power down for Amp 2. This voltage adjusts for the current draw in Amp 2.
13	RFin	RF input pin. The DC is internally blocked at this pin.
Backside Pad	RF/DC GND	RF/DC ground. Use recommended via pattern to minimize inductance and thermal resistance; see PCB Mounting Pattern for suggested footprint.

Package Marking and Dimensions

Marking: Part Identifier – 9321
 Assembly Code - YYWW
 Lot code –AaXXXX

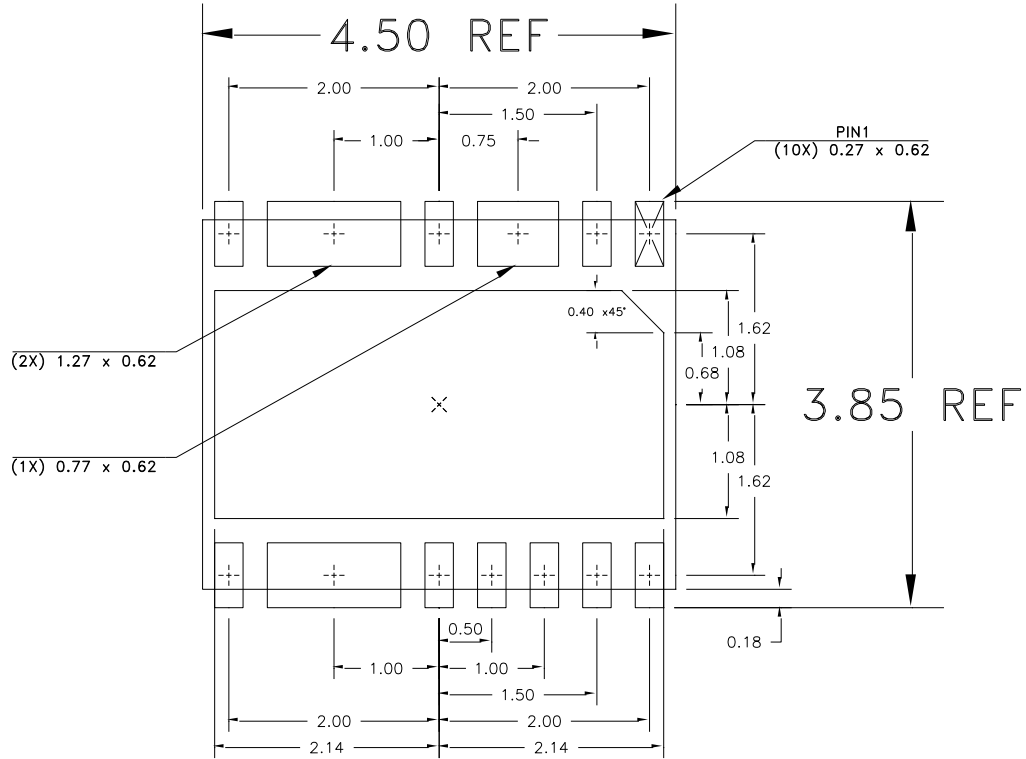


Notes:

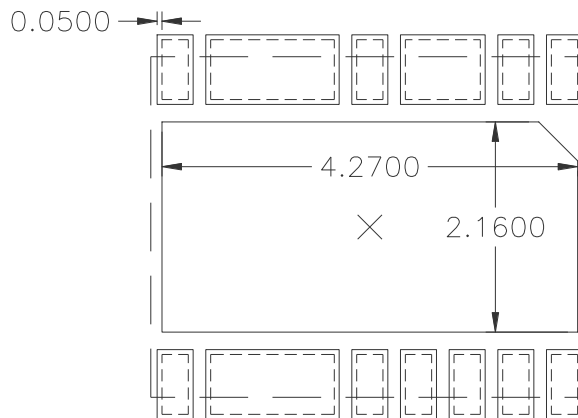
1. All dimensions are in millimeters. Angles are in degrees.
2. Except where noted, this part outline conforms to JEDEC standard MO-229.
3. Dimension and tolerance formats conform to ASME Y14.4M-1994.
4. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

PCB Mounting Pattern

Recommend PCB land-pad pattern metallization (Top View)



Recommended PCB solder mask opening (Top View)



Notes:

1. A heat sink underneath the area of the PCB for the mounted device is strictly required for proper thermal operation. Damage to the device can occur without the use of one.
2. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35mm (#80 / .0135") diameter drill and have a final plated thru diameter of .25 mm (.010").
3. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 2	ESDA / JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	Class C3	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	Level 3	IPC/JEDEC J-STD-020



Caution!
ESD-Sensitive Device

Solderability

Compatible with both lead-free (260°C max. reflow temp.) and tin/lead (245°C max. reflow temp.) soldering processes.
Solder profiles available upon request.
Contact plating: Electrolytic plated Au over Ni

RoHS Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment). This product also has the following attributes:

- Product uses RoHS Exemption 7c-I to meet RoHS Compliance requirements
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C₁₅H₁₂Br₄O₂) Free
- PFOS Free
- SVHC Free
- Qorvo Green



Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Tel: 1-844-890-8163

Web: www.qorvo.com

Email: customer.support@qorvo.com

For technical questions and application information: **Email:** appsupport@qorvo.com

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