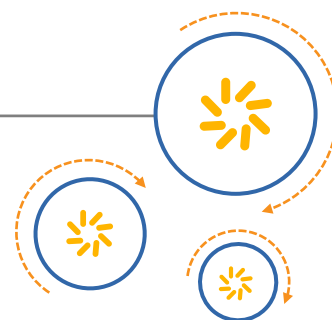




Qualcomm Atheros, Inc.



QCA4002 Low-Energy Wi-Fi Single-Band 802.11b/g/n SoC

Device Specification

80-Y6806-5 Rev. D

January 7, 2015

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Revision history

Revision	Date	Description
A	April 2014	Initial release. For regular distribution as part of PDK via Qualcomm Developer Network.
B	September 2014	<ul style="list-style-type: none"> ■ Global change: Converted the data sheet to device specification. The content movings below are not marked with change bar. <ul style="list-style-type: none"> □ Moved functional description to Section 1.5 through Section 1.15. □ Moved voltage regulator and bootstrap mode to Section 1.16 and Section 1.17. □ Moved package dimensions, ordering information, and thermal characteristics to Chapter 4. □ Moved power sequence to Section 3.3 and clock/timing to Section 3.5. ■ Section 1.1, Section 1.4: Added document overview and special marks. ■ Section 1.15: Added DNS, SNTP, bridging/routing, and raw socket support. ■ Figure 2-1, Table 2-1: Changed pin 41, 46, 47, 51, 52 to reserved. ■ Chapter 4: Added the Mechanical information chapter. ■ Section 4.1: Updated the package drawing and dimensions according to NT90-Y5241-1. ■ Section 4.3: Updated ordering number for chip revision B. ■ Chapter 5: Added Carrier, Storage, and Handling Information. ■ Chapter 6: Added PCB Mounting Guidelines. ■ Chapter 7: Added chip reliability data.
C	October 2014	Table 3-2: Corrected the chip case temperature for industrial part.
D	January 2015	Cover page: Replaced the cover with new branding and legal statements. Table 3-1 : Deleted legacy ESD-HBM, ESD-CDM, ESD-CDM-RF rows.

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1 Introduction

1.1 Document overview

Technical information for the QCA4002 is primarily covered by the documents listed in [Table 1-1](#). Each is a self-contained document, but a thorough understanding of the device and its applications requires familiarization with all of them. The device description in is a good place to start.

Table 1-1 Primary QCA4002 documentation

Document No.	Title/Description
80-Y6805-6 (this document)	QCA4002 Low-Energy Wi-Fi Single-Band 802.11b/g/n SoC Device Specification Conveys all QCA4002 IC electrical and mechanical specifications. Additional material includes pin assignments; shipping, storage, and handling instructions; PCB mounting guidelines; and part reliability. This document can be used by company purchasing departments to facilitate procurement.

The QCA4002 Low-Energy Wi-Fi Single-Band 802.11b/g/n SoC Device Specification is organized as follows:

- [Chapter 1](#) Gives a high-level functional description of the device, lists the device features, and defines marking conventions, terms, and acronyms used throughout this document.
- [Chapter 2](#) Defines the device pin assignments.
- [Chapter 3](#) Defines the device electrical characteristics, including absolute maximum ratings and recommended operating conditions.
- [Chapter 4](#) Provides IC mechanical information, including dimensions, markings, ordering information, moisture sensitivity, and thermal characteristics.
- [Chapter 5](#) Describes carrier, storage and handing information of the QCA4002 device.
- [Chapter 6](#) Presents procedures and specifications for mounting the QCA4002 device onto printed circuit boards (PCBs).
- [Chapter 7](#) Presents the QCA4002 device reliability data, including a definition of the qualification samples and a summary of qualification test results.

1.2 QCA4002 device description

The QCA4002 is an intelligent platform for the Internet of Everything that contains a low-power Wi-Fi connectivity solution on a single chip. It includes a number of TCP/IP-based connectivity protocols along with SSL, enabling a low-cost, low-complexity system to obtain full-featured internet connectivity and reliable information exchange.

The QCA4002 provides two interfaces for connecting to local system controllers. A UART-based host interface can be used for rapid development and deployment of simple data streams between the local device and the internet cloud. An SPI slave interface is available for applications that require more advanced connectivity to the network.

The QCA4002 Wi-Fi link is a full-featured, single-band, single stream 802.11n solution. The Wi-Fi link is highly integrated, and includes an energy efficient on-board power amplifier and LNA. RF switches are also integrated. The QCA4002 Wi-Fi link is optimized for low system cost, and minimizes the number and cost of any components required to achieve a reliable Wi-Fi link.

1.3 Product features

Wi-Fi link

- Support for IEEE 802.11b/g/n
- Single stream 1 × 1
- Single-band 2.4 GHz
- Integrated PA, LNA, with support for external PA and external LNA
- Single Rx front end for multiple applications
- Green Tx power saving mode
- Low power listen mode
- Data rates up to 150 Mbps
- Full security support: WPS, WPA, WPA2, WAPI, WEP, TKIP

System cost optimization

- Highly-Integrated Wi-Fi solution that requires only a single crystal, antenna, and antenna matching components to complete the RF link.
- Integrated IPv4/IPv6 TCP/IP stack
- Integrated Network services such as HTTP, DNS, FTP
- 7 mm x 7 mm, 56-pin QFN package
- QCA4002 patch firmware is stored and automatically loaded from a low cost serial flash memory

Manufacturing interface

- USB 2.0 device interface, providing a simplified, high-speed, and scalable manufacturing test and configuration interface for QCA4002-based systems

Host interfaces

- SPI slave interface

Allows for simplified connection to local host microcontrollers.
Host driver source code and programming APIs are available.

- UART/SPI host interface allows simple interfacing to microcontrollers.
- UART with an AT style command set

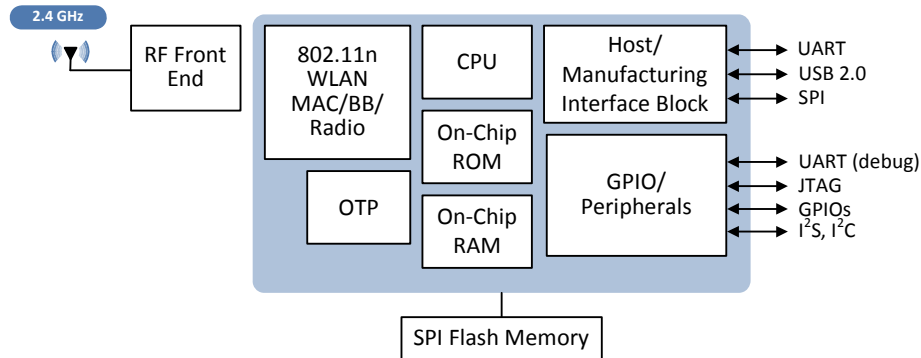


Figure 1-1 QCA4002 functional block diagram

1.4 Special marks

Table 1-2 defines special marks used in this document.

Table 1-2 Special marks

Mark	Definition
[]	Brackets ([]) sometimes follow a pin, register, or bit name. These brackets enclose a range of numbers. For example, SDC1_DATA[7:4] may indicate a range that is 4 bits in length, or DATA[7:0] may refer to all eight DATA pins.
_N	A suffix of _N indicates an active low signal. For example, RESIN_N.
0x000	Hexadecimal numbers are identified with an x in the number (for example, 0x0000). All numbers are decimal (base 10) unless otherwise specified. Non-obvious binary numbers have the term binary enclosed in parentheses at the end of the number; for example, 0011 (binary).
	A blue vertical bar in the outside margin of a page indicates that a change was made since the previous revision of this document.

1.5 Integrated network processor

The QCA4002 includes a network processor that provides IP services and manages Wi-Fi link operations. The network processor code is loaded automatically from ROM off-chip serial flash memory. The flash memory is also used to store system configuration and persistent data sets. The

network processor is optimized for energy efficient communications and includes multiple power states (see [Section 1.8](#)) that are managed by the external host CPU.

1.6 Serial interface

The QCA4002 includes two high-speed Universal Asynchronous Receiver/Transmitter (UART) interfaces, which may be configured to serve as either a host interface link or a debug message console.

1.7 Reset and startup sequence

The QCA4002 CHIP_PWD_L pin can be used to completely reset the entire chip. After this signal has been de-asserted, if configured for SPI slave operation, the QCA4002 waits in a low-power state until communication from the host, indicating that the Wi-Fi and the network services should be started. When configured for UART host mode, the QCA4002 begins its boot up process and starts network services as soon as CHIP_PWD_L is de-asserted.

1.7.1 Detailed SPI slave startup sequence

After a COLD_RESET event (e.g., the host toggles CHIP_PWD_L), the QCA4002 enters the HOST_OFF state and awaits communication from the host indicating that Wi-Fi and network services should be started. When configured for UART host mode, the QCA4002 begins its boot up process and starts network services as soon as CHIP_PWD_L pin is de-asserted.

- When the host is ready to use the QCA4002, it initiates communication via SPI slave and enables network services by writing to a specific register via the SPI slave interface.
- When the QCA4002 enters the WAKEUP state for some duration and transits to the ON state, the on-chip network processor configures the QCA4002 functions and interfaces, as per the configuration and customization data set provided by the serial flash memory. When the QCA4002 is ready to receive commands from the host, it sets a specific flag that is accessible from the Host CPU via the SPI slave interface.
- The host reads the ready bit and can now send function commands to the QCA4002.

1.7.2 Power management unit

The QCA4002 has an integrated power management unit (PMU) that generates all the power supplies required by its internal circuitry either from an external battery or a 3.3 V supply. The main components of the PMU include:

- A switching regulator (SWREG) that produces a 1.2 V supply from the 3.3 V supply.
- A linear regulator (SREG) which converts the host I/O supply to a 1.2 V supply for some small control blocks which are turned on when CHIP_PWD_L is de-asserted.
- A linear regulator which produces a 1.2 V supply from a 3.3 V supply (can be used instead of the SWREG to reduce the BOM cost).

1.8 Power transition

The QCA4002 provides integrated power management and control functions and extremely low power operation for maximum battery life across all operational states by:

- Gating clocks for logic when not needed
- Shutting down unneeded high speed clock sources
- Reducing voltage levels to specific blocks in some states

1.8.1 Sleep state management

SLEEP state minimizes power consumption while network services are not required, yet the system must remain ready for use within a short time. In SLEEP state, all high speed clocks are gated off and the external reference clock source is powered off. The network processor and Wi-Fi link are also suspended and not operational. All state information in the network processor (and its memory) and the Wi-Fi link are preserved to allow a fast resume to full network services.

The system remains in sleep state until a wakeup event causes the system to enter the WAKEUP state. Once WAKEUP state is entered, the QCA4002 restores all voltage levels and clocks, then automatically moves to the ON state. This wakeup event can be either a pin event or internal timer based event. The pin event may be triggered by the host CPU, or some system level event.

1.8.2 Hardware power states

[Table 1-3](#) describes the top level hardware power states in the QCA4002.

Table 1-3 Power management states

State	Description
POWER_DOWN	CHIP_PWD_L pin assertion immediately brings the chip to this state.
	Sleep clock is disabled.
	No state is preserved.
HOST_OFF	Network services and WLAN are off. Only the SPI host interface is powered on, the rest of the chip is power gated (off).
	The host can transition QCA4002 to WAKEUP (followed by ON) at any time by writing a register in the host interface domain.
	WLAN and CPU states are not retained.
	For UART hosted, or USB manufacturing configurations, this state is bypassed by pulling GPIO0 low at the de-assertion of CHIP_PWD_L. This state applies only to SPI designs.
SLEEP	Only the sleep clock is operating.
	The crystal or oscillator is disabled.
	Any wakeup events (MAC, host, LF timer, GPIO interrupt force a transition to WAKEUP.
	All internal states are maintained.
	Host interface is idle (USB is in SUSPEND).

Table 1-3 Power management states

State	Description
WAKEUP	The system transition from sleep OFF states to ON.
	The high frequency clock is gated off as the oscillator is brought up and the PLL is enabled.
	WAKEUP duration is less than 2 ms.
ON	The high speed clock is operational.
	Lower-level clock gating is implemented at the block level, including the CPU, which can be gated off using WAITI instructions while the system is on.

Figure 1-2 depicts the SPI power state transition diagrams.

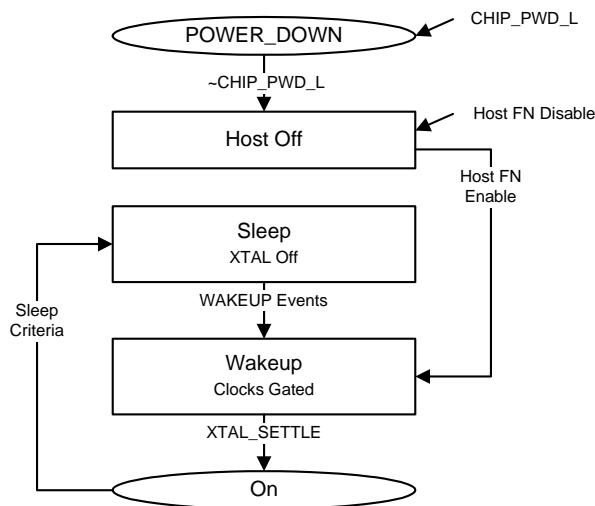


Figure 1-2 QCA4002 power state: SPI host modes

Figure 1-3 depicts the USB and UART power state transition diagrams.

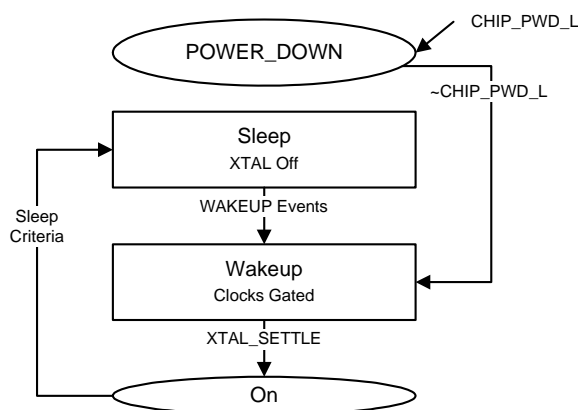


Figure 1-3 QCA4002 Power State: USB and UART Host Modes

1.9 System clocking (RTC block)

The QCA4002 has an RTC block which controls the clocks and power going to other internal modules. Its inputs consist of sleep requests from these modules and its outputs consist of clock enable and power signals which are used to gate the clocks going to these modules. The RTC block also manages resets going to other modules with the device. The QCA4002's clocking is grouped into two types:

- High-speed
- Low-speed

1.9.1 High speed clocking

The reference clock source drives the PLL and RF synthesizer within the QCA4002. It can be either an external crystal or oscillator. To minimize power consumption, the reference clock source is powered off in SLEEP, HOST_OFF, POWER_DOWN and after HOST_OFF states. For an external crystal, the QCA4002 disables the on-chip oscillator driver. For an external oscillator, the QCA4002 de-asserts its CLK_REQ signal to indicate that a reference clock is not needed.

When exiting SLEEP state, the QCA4002 waits in WAKEUP state for a programmable duration. During this time, the CLK_REQ signal is asserted to allow for the reference clock source to settle. The CLK_REQ signal remains asserted in ON state.

The QCA4002 supports reference clock sharing in all power states. For an external crystal, the on-chip oscillator driver drives a reference clock output whenever an external clock request signal is asserted. For an external oscillator, the external clock request signal is forwarded on the CLK_REQ signal, and the input clock is passed along to the reference clock output.

1.9.2 Low-speed clocking

The QCA4002 has eliminated the need for an external sleep clock source thereby reducing system cost. Instead, an internal ring oscillator is used to generate a low frequency sleep clock. It is also used to run the state machines and counters related to low power states.

The QCA4002 has an internal calibration module which produces a 32.768 KHz output with minimal variation. For this, it uses the reference clock source as the golden clock. As a result, the calibration module adjusts for process and temperature variations in the ring oscillator when the system is in ON state.

1.9.3 Interface clock

The host interface clock represents another clock domain for the QCA4002. This clock comes from the host and is completely independent from the other internal clocks. It drives the host interface logic as well as certain registers which can be accessed by the host in HOST_OFF and SLEEP states.

1.10 MAC block

The QCA4002 Wireless MAC consists of these major blocks:

- Host interface unit (HIU) for bridging to the AHB for bulk data accesses and APB for register accesses
- 10 queue control units (QCU) for transferring Tx data
- 10 DCF control units (DCU) for managing channel access
- Protocol control unit (PCU) for interfacing to baseband
- DMA receive unit (DRU) for transferring Rx data

1.11 Baseband block

The QCA4002 baseband (BB) module is the physical layer controller for the 1x1 802.11b/g/n air interface. It is responsible for modulating data packets in the transmit direction, and detecting and demodulating data packets in the receive direction. It has a direct control interface to the radio to enable hardware to adjust analog gains and modes dynamically.

1.12 Active power save

1.12.1 Low Power Listen (LPL)

To minimize active current consumption, the QCA4002 firmware will set the receiver in a low power listen mode, thus saving active power in between frames, when the transceiver is awaiting frames, as well as during active reception. It can be enabled in most conditions with minimal performance impact, between 1 and 2 dB. If harsh channel conditions require it, firmware will automatically revert to full power mode.

1.12.2 Green Tx

To minimize active current consumption during transmission, the QCA4002 will utilize Green Tx. This feature allows the device to save power when communicating with a nearby station or access point when high output power is not required to sustain reliable communications. In such cases, the transmitter will reduce the transmit power to obtain current saving, while maintaining its high uplink throughput.

1.13 IPv4/IPv6 networking

The QCA4002 includes a TCP/IP and UDP offload capability. This capability can reduce Flash requirements on a host MCU by up to 100 KBytes and also free up CPU cycles. The IP stack is a simultaneous IPv4/IPv6 stack with a BSD-like interface to simplify porting and integration with common embedded operating systems. The supported features of the QCA4002 (support for DHCP, multicast, and ARP) include:

- ARP
- Forwarding
- Fragmentation/reassembly (supported with limitation)
- IPv4/v6 header processing
- UDP/TCP socket support
- DHCP v4
- Neighbor discovery
- Broadcast/multicast
- Address auto-configuration
- Multicast
- TCP zero-copy feature
- HTTP/SSL client/server feature
- DNS proxy server and client
- SNTP client
- Bridging/Routing
- Raw sockets

The QCA4002 supports many key IPv4 and IPv6 RFCs as shown in [Table 1-4](#) and [Table 1-5](#).

Table 1-4 QCA4002 IPv4 supported RFCs

IPv4 RFC Number
RFC1122: TCP Timeout/retransmission
RFC1122: TCP Keep-alive
RFC1122: TCP Zero-Window-Probe
RFC1122: TCP Sliding window protocol

Table 1-5 QCA4002 IPv6 supported RFCs

IPv6 RFC Number
RFC2464: Transmission of IPv6 packets over Ethernet networks
RFC2460: Internet Protocol version 6
RFC2462: Duplicate Address Detection (DAD)
RFC2463: ICMPv6
RFC3513: IP version 6 addressing architecture
RFC3484: Default Address Selection
RFC2461: Neighbor discovery for IPv6 host
RFC4862: Stateless Address Auto-configuration

1.14 Internal voltage regulator

The QCA4002 supports two regulator modes for its on-chip 1.2 V regulator; see [Section 1.15.3](#) for more information.

1.14.1 Switching 1.2 V regulator

[Figure 1-4](#) depicts the switching 1.2 V switching power supply regulated by the QCA4002. Refer to the reference design schematics for details.

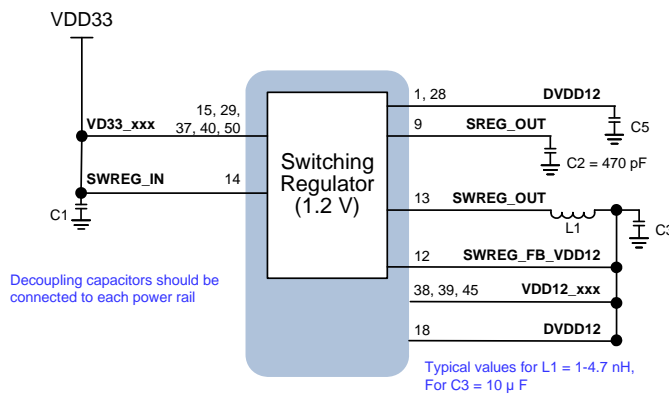


Figure 1-4 1.2 V switching power supply regulated by the QCA4002

1.14.2 Linear 1.2 V regulator

[Figure 1-5](#) depicts the switching 1.2 V linear power supply regulated by the QCA4002. Refer to the reference design schematics for details.

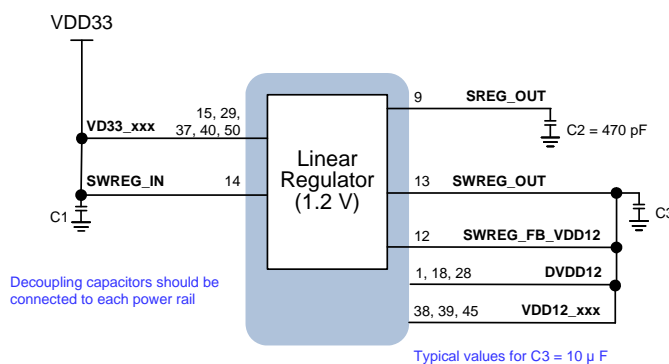


Figure 1-5 1.2 V linear power supply regulated by the QCA4002

1.15 Bootstrap modes and pins

Certain pins in the QCA4002 are sampled at startup, and these sampled values are used to select among various bootstrap modes and chip configurations.

1.15.1 Host mode configuration

Table 1-6 lists the QCA4002 bootstrap pins that select the interface used to communicate with the external host CPU. Host mode selection affects pin behavior of host interface pins as well as bootup processes in the PCM state machine. It informs the QCA4002 about the presence of an external CPU (referred to as the host controller) and the interface used to exchange messages.

Table 1-6 Host mode configuration

Pin name	Bootstrap function name	On chip biasing	GPIO [0,2]	Description
GPIO0, GPIO2	hostmode	—	00	QCA4002 CPU bootup is under control of the host CPU via the USB interface. The external CPU is required and the host interface is USB.
			01	No host required at startup time. The QCA4002 CPU self boots and firmware may configure any of the available interfaces. No external CPU is required.
			10	The QCA4002 CPU bootup is under control of host CPU via SPI Slave interface. The external CPU is required and the SPI interface is the host interface.
			11	Reserved

1.15.2 Crystal value configuration

Table 1-7 shows the bootstrap pin to configure the crystal value.

Table 1-7 Crystal value configuration

Pin name	Bootstrap function name	On chip biasing	Description	
GPIO20	xtal_freq[0]	—	0	Reserved
			1	40 MHz

1.15.3 1.2 V regulator configuration

The QCA4002 supports two regulator modes for its on-chip 1.2 V regulator: switching and linear. Linear mode requires fewer board-level components, but at a slightly higher power consumption than switching mode. Table 1-8 shows the bootstrap pin to configure the 1.2 V regulator.

Table 1-8 1.2 V regulator configuration

Pin name	Bootstrap function name	On chip biasing	Description	
GPIO13	en_linear	—	0	Switching regulator
			1	Linear regulator

2 Pin Descriptions

The QCA4002 device is available in the 56-pin QFN that includes several ground pins for electrical grounding, mechanical strength, and thermal continuity. See [Chapter 4](#) for package details. A high-level view of the pin assignments is shown in [Figure 2-1](#).

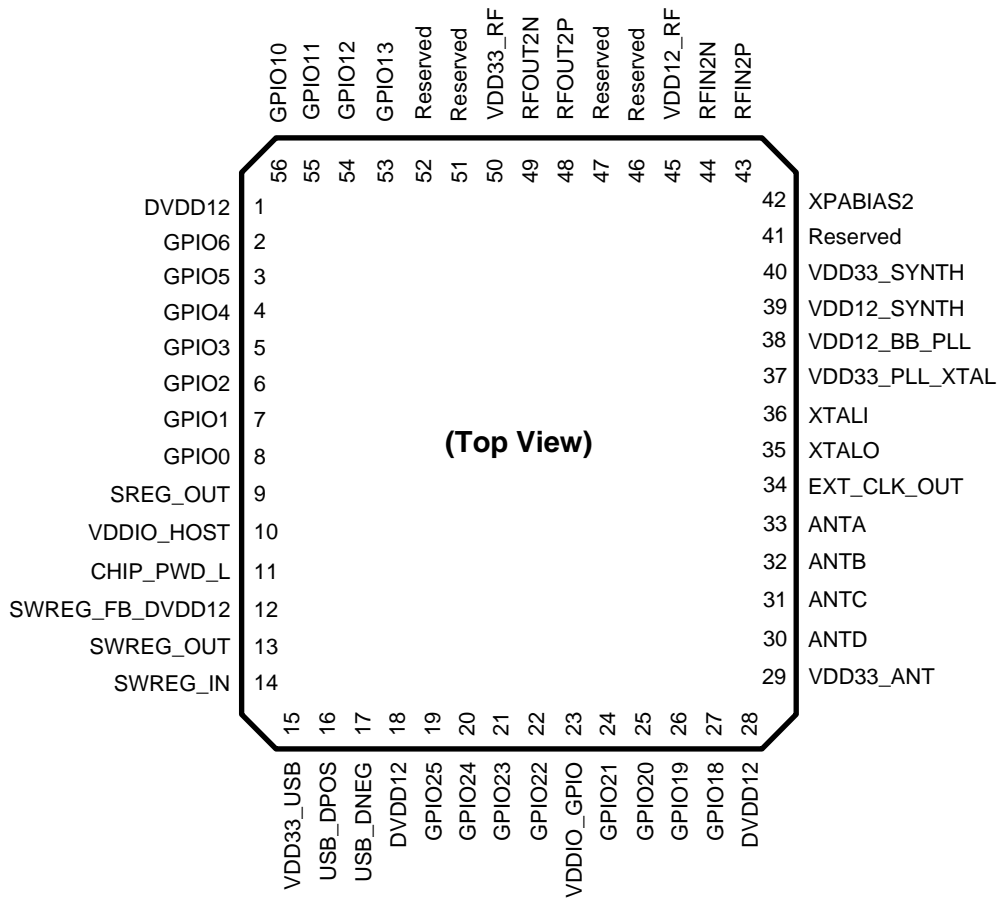


Figure 2-1 QCA4002 pin assignments (top view)

2.1 I/O parameter definitions

The following nomenclature is used for signal names:

NC/Reserved	No connection should be made to this pin
_L	At the end of the signal name, indicates active low signals
P	At the end of the signal name, indicates the positive side of a differential signal
N	At the end of the signal name indicates the negative side of a differential signal

The following nomenclature is used for signal types:

IA	Analog input signal
I	Digital input signal
IH	Input signals with weak internal pull-up, to prevent signals from floating when left open
IL	Input signals with weak internal pull-down, to prevent signals from floating when left open
I/O	A digital bidirectional signal
OA	An analog output signal
O	A digital output signal
P	A power or ground signal

Table 2-1 provides the signal-to-pin relationship information for the QCA4002.

Table 2-1 Pin description

Signal Name	Pin	Type	Description
General			
EXT_CLK_OUT	34	O	External clock out, 1.2 V level. Its corresponding half rate is available when configured.
XTALI	36	I/O	Supports 40 MHz crystal.
XTALO	35	I	When an external reference clock is used, connect the clock signal to the XTALO pin and ground the XTALI pin.
Radio			
CHIP_PWD_L	11	I	Chip power-down control
RFIN2N	44	IA	Differential 2.4 GHz RF inputs
RFIN2P	43	IA	
Reserved	46	IA	Reserved
Reserved	47	IA	
RFOUT2N	49	OA	Differential 2.4 GHz RF outputs
RFOUT2P	48	OA	
Reserved	51	OA	Reserved
Reserved	52	OA	

Table 2-1 Pin description (cont.)

Signal Name	Pin	Type	Description
GPIO			
GPIO0	8	I/O	General purpose input/output.
GPIO1	7	I/O	The QCA4002 supports SPI, I ² C, I ² S, UART, and JTAG interfaces. The QCA4002 can be configured to support these interfaces by tying certain inputs externally during boot up.
GPIO2	6	I/O	
GPIO3	5	I/O	
GPIO4	4	I/O	
GPIO5	3	I/O	
GPIO6	2	I/O	
GPIO10	56	I/O	
GPIO11	55	I/O	
GPIO12	54	I/O	
GPIO13	53	I/O	
GPIO18	27	I/O	
GPIO19	26	I/O	
GPIO20	25	I/O	
GPIO21	24	I/O	
GPIO22	22	I/O	
GPIO23	21	I/O	
GPIO24	20	I/O	
GPIO25	19	I/O	
Analog Interface			
XPABIAS2	42	OA	Bias for optional external power amplifier in 2.4 GHz
Reserved	41	OA	Reserved
External Switch Control			
ANTA	33	O	External RF switch control
ANTB	32	O	
ANTC	31	O	
ANTD	30	O	
USB			
USB_DPOS	16	IA/OA	USB D+ signal; carries USB data to and from the USB 2.0 PHY
USB_DNEG	17	IA/OA	USB D- signal; carries USB data to and from the USB 2.0 PHY
Internal Switching Regulator			
SREG_OUT	9	P	1.2 V SDIO regulator output, connect to a 470 pF bypass capacitor on the board.
SWREG_OUT	13	P	1.2 V switching regulator output to an LC filter or LDO
SWREG_IN	14	P	Connect to 3.3 V supply for the internal switching regulator or LDO
Power			
DVDD12	1, 18, 28	P	Digital 1.2 V power supply, should be connected to the SWREG_FB_VDD12 pin.

Table 2-1 Pin description (cont.)

Signal Name	Pin	Type	Description
SWREG_FB_DVDD12	12	P	Reference feedback voltage to the internal switching regulator or LDO
VDD12_BB_PLL	38	P	Analog 1.2 V power supply, should be connected to the SWREG_FB_VDD12 pin.
VDD12_RF	45	P	
VDD12_SYNTN	39	P	
VDD33_SYNTN	40	P	Analog 3.3 V power supply
VDD33_ANT	29	P	
VDD33_RF	50	P	
VDD33_PLL_XTAL	37	P	
VDD33_USB	15	P	
VDDIO_HOST	10	P	Connect to 3.3 V host I/O supply
VDDIO_GPIO	23	P	Connect to 3.3 V host I/O supply or 1.8 V peripheral I/O supply
Ground			
GND	–	P	Exposed ground pad (Mechanical Information)

3 Electrical Characteristics

3.1 Absolute maximum ratings

Absolute maximum ratings are those values beyond which damage to the device can occur. Functional operation under these conditions, or at any other condition beyond those indicated in this chapter, is not recommended.

[Table 3-1](#) summarizes the absolute maximum ratings for the QCA4002 device. [Table 3-2](#) shows the recommended operating conditions.

NOTE Maximum rating for signals follows the supply domain of the signals.

Table 3-1 Absolute maximum ratings

Symbol (Domain)	Description	Max rating	Unit
VDDIO_GPIO	I/O supply for GPIO18-GPIO25 pins	-0.3 to 4.0	V
VDDIO_HOST	I/O supply for GPIO0-GPIO13 pins	-0.3 to 4.0	V
DVDD12	Digital 1.2 V supply ¹	-0.3 to 1.32	V
SWREG_FB_VDD12			
VDD12_BB_PLL	1.2 V supply for analog BB PLL	-0.3 to 1.32	V
VDD12_RF	1.2 V supply for analog RF	-0.3 to 1.32	V
VDD12_SYNT	1.2 V supply for analog SYNT	-0.3 to 1.32	V
VDD33_ANT	Antenna control I/O supply	-0.3 to 4.0	V
VDD33_RF	3.3 V supply for analog RFs	-0.3 to 4.0	V
VDD33_SYNT	3.3 V supply for analog SYNT	-0.3 to 4.0	V
VDD33	3.3 V supply for switching regulator/PMU	-0.3 to 4.0	V
SWREG_IN			
VDD33_PLL_XTAL	3.3 V supply for XTAL/PLL	-0.3 to 4.0	V
VDD33_USB	3.3 V supply for USB	-0.3 to 4.0	V
V _{IH} MIN	Minimum Digital I/O Input Voltage for 1.8 V or 3.3 V I/O Supply	-0.3	V
3.3 V I/O V _{IH} MAX	Maximum Digital I/O Input Voltage for 3.3 V I/O Supply	V _{dd} +0.3	V
RF _{in}	Maximum RF input (reference to 50-Ω input)	+10	dBm
T _{store}	Storage Temperature	-45 to 135	°C
T _j	Junction Temperature	125	°C

1. DVDD12 and SWREG_FB are connected through an external LC filter to the SWREG_OUT pin. See [Figure 1-4](#).

3.2 Recommended operating conditions

Table 3-2 Recommended operating conditions

Symbol (Domain)	Parameter	Min	Typ	Max	Unit
VDDIO_GPIO	I/O supply for GPIO18-GPIO25 pins	1.71	–	3.46	V
VDDIO_HOST	I/O supply for GPIO0-GPIO13 pins	3.0	–	3.6	V
DVDD12	Digital 1.2 V supply ¹	1.20	1.26	1.32	V
SWREG_FB_VDD12					
VDD12_BB_PLL, VDD12_SYNT _H , VDD12_RF	Analog 1.2 V supplies	1.20	1.26	1.32	V
VDD33	Internal switching regulator supply	3.14	3.3	3.46	V
SWREG_IN					
VDD33_ANT	Antenna control I/O supply	3.14	3.3	3.46	V
VDD33_RF, VDD33_SYNT _H , VDD33_PLL_XTAL, VDD33_USB	Analog 3.3 V supplies	3.14	3.3	3.46	V
T _{case}	Standard case temperature	0	–	85	°C
	Industrial case temperature	-40	–	105	°C

1. DVDD12 and SWREG_FB_VDD12 are connected through an external LC filter to the SWREG_OUT pin. See Figure 1-4.

3.3 Power sequencing

If a host processor controls the QCA4002 CHIP_PWD_L reset pin, then all supplies should be stable for a minimum of 5 μ s before CHIP_PWD_L is de-asserted (that is, is greater than V_{IL} for VDDIO_SDIO).

In the case where CHIP_PWD_L is not driven, but is a delayed version of VDD33 (power-on reset), the timing diagram in Figure 3-1 applies.

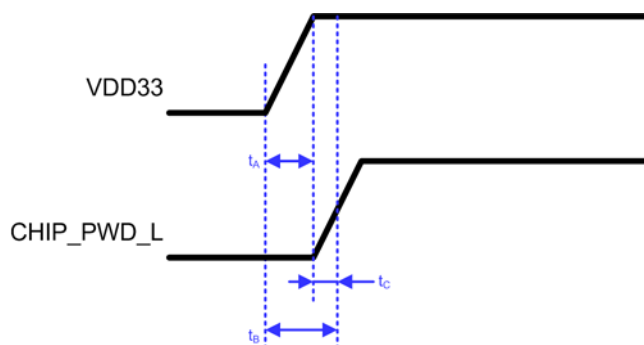


Figure 3-1 Power-On-Reset Timing

Table 3-3 shows the values for timing for power on reset.

Table 3-3 Power-on-reset timing

Parameter	Description	Min	Max	Unit
t_A	Rise time of VDD33 to 90% of 3.3 V	–	25	mS
t_C	Time from VDD33 reaching 90% of 3.3 V to the level of CHIP_PWD_L going above $0.5 \times VDD33$	5	—	μ S
t_B	The value is $t_A + t_C$; during this time, the level of CHIP_PWD_L should stay below $0.5 \times VDD33$			

3.4 Digital logic characteristics

These conditions apply to all DC characteristics unless otherwise specified:

$$T_{amb} = 25 \text{ }^\circ\text{C}, V_{dd33} = 3.3 \text{ V}$$

Table 3-4 DC electrical characteristics for digital I/Os

Symbol	Parameter	Min	Typ	Max	Unit
V_{IH}	High Level Input Voltage	1.8	–	3.6	V
V_{IL}	Low Level Input Voltage	-0.3	–	0.3	V
V_{OH}	High Level Output Voltage	2.2	–	3.3	V
V_{OL}	Low Level Output Voltage	0	–	0.4	V
I_{IH}	High Level Input Current	–	–	0.1	μ A
I_{IL}	Low Level Input Current	–	–	0.1	μ A
I_{OH}	High Level Output Current for GPIO0 to GPIO13	–	–	8	mA
	High Level Output Current for GPIO18 to GPIO25	–	–	20	
I_{OL}	Low Level Output Current for GPIO0 to GPIO13	–	–	20	mA
	Low Level Output Current for GPIO18 to GPIO25	–	–	20	
C_{IN}	Input Capacitance for GPIO0 to GPIO13	–	5	–	pF
	Input Capacitance for GPIO18 to GPIO25	–	3	–	

3.5 Clock requirements

3.5.1 External reference clock timing

Figure 3-2 and Table 3-5 show the external 40 MHz reference input clock timing requirements.

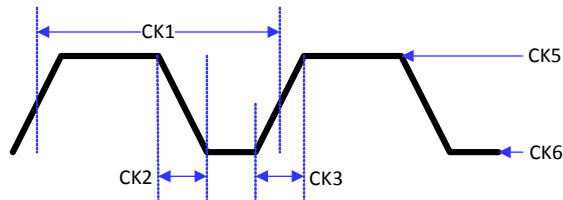


Figure 3-2 External reference input clock timing

Table 3-5 External 40 MHz reference input clock timing

Symbol	Description	Min	Typ	Max	Unit
CK1	Frequency accuracy	-20	–	20	ppm
	Frequency	–	40	–	MHz
CK2	Fall time	–	–	0.1 x period	ns
CK3	Rise time	–	–	0.1 x period	ns
CK4	Duty cycle (high-to-low ratio)	40	–	60	%
CK5	Input high voltage	0.75	–	1.26	V
CK6	Input low voltage	-0.55	–	0.3	V

3.5.2 SPI slave interface timing

Figure 3-3 shows the write timing for SPI slave style transactions.

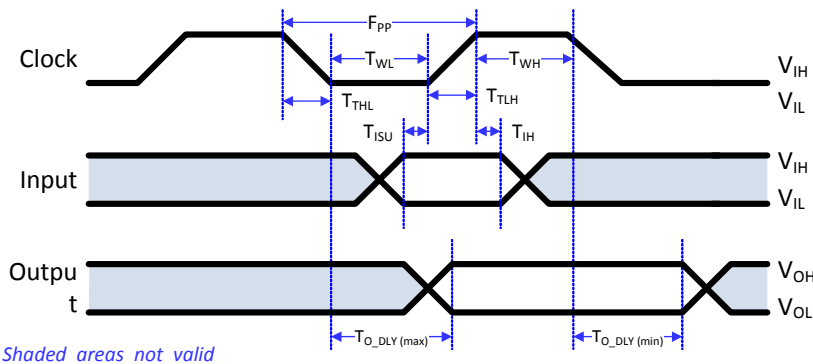


Figure 3-3 SPI slave timing

Table 3-6 shows the values for timing constraints for SPI slave.

Table 3-6 SPI slave timing constraints

Parameter	Description	Min	Max	Unit
f _{pp}	Clock frequency	0	48	MHz
t _{WL}	Clock low time	8.3	–	ns
t _{WH}	Clock high time	8.3	–	ns
t _{TLH}	Clock rise time	–	2	ns

Table 3-6 SPI slave timing constraints

Parameter	Description	Min	Max	Unit
t_{THL}	Clock fall time	–	2	ns
t_{ISU}	Input setup time	5	–	ns
t_{IH}	Input hold time	5	–	ns
t_{O_DLY}	Output delay	0	5	ns

3.5.3 SPI master interface timing

Figure 3-4 shows the write timing for SPI master style transactions.

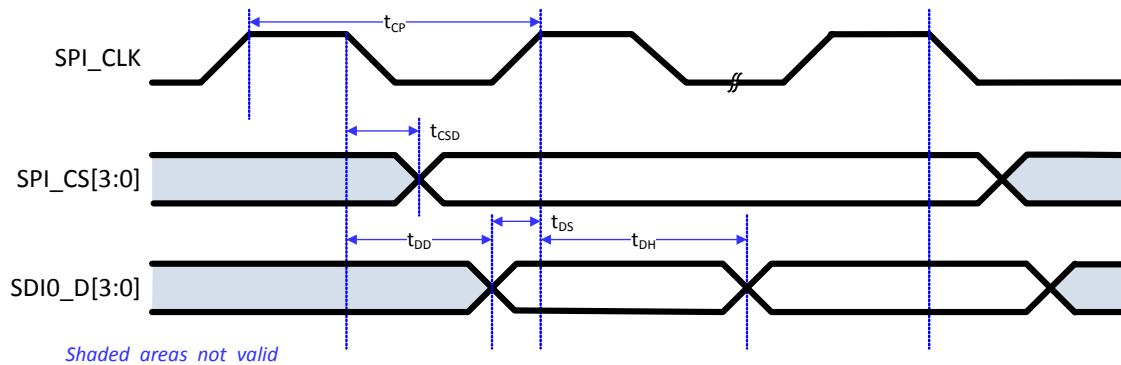
**Figure 3-4 SPI master timing**

Table 3-6 shows the values for timing constraints for SPI master.

Table 3-7 SPI master timing constraints

Parameter	Description	Min	Max	Unit
t_{CP}	Clock period	30.7	1000	ns
t_{CSD}	Chip select valid delay	-5.5	5	ns
t_{DD}	Data valid delay	-5.5	5	ns
t_{DS}	Data setup	3	–	ns
t_{DH}	Data hold	0	–	ns

4 Mechanical Information

4.1 Device physical dimensions

The QCA4002 device is available in the 7 mm × 7 mm × 0.85 mm Micro Quad Flat pack No-lead (MQFN) package that includes a ground pad for improved grounding, mechanical strength, and thermal continuity. Pin 1 is located by an indicator mark on the top of the package.

Figure 4-1 shows the QCA4002 device mechanical dimensions, top and bottom views.

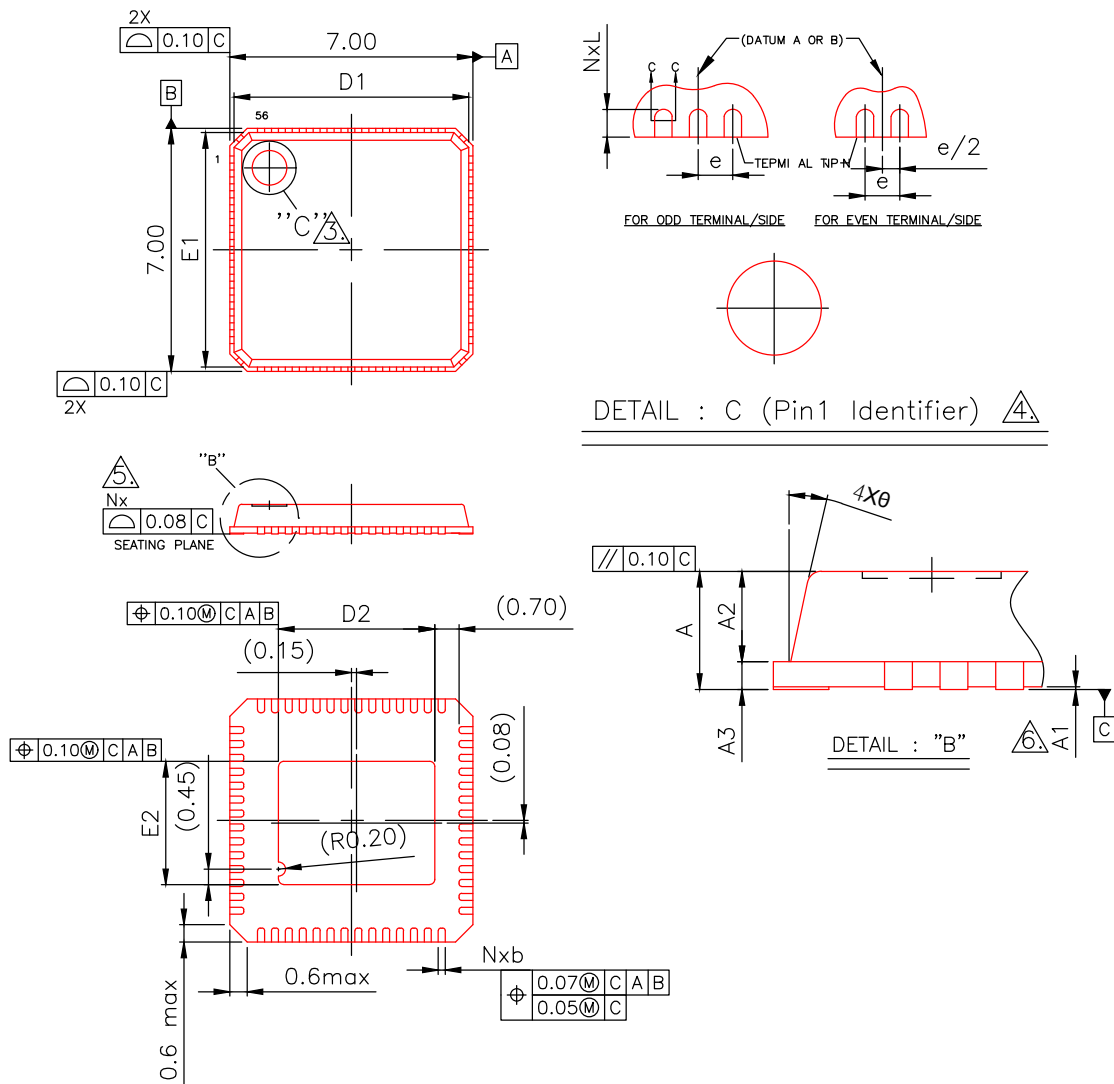


Figure 4-1 QCA4002 mechanical dimensions, top and bottom views

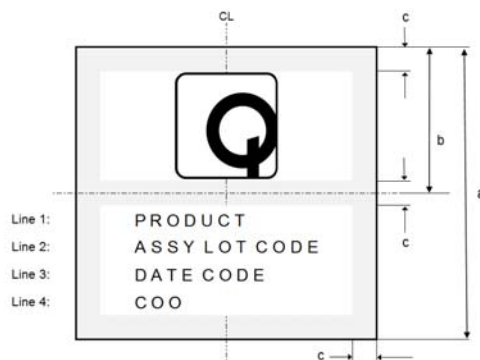
Table 4-1 Mechanical dimensions ¹

Dimension label	Min	Nom	Max	Unit
A	–	–	0.90	mm
A1	0.00	0.02	0.05	mm
A2	0.60	0.65	0.70	mm
A3	0.20 REF			mm
b	0.15	0.20	0.25	mm
L	0.30	0.40	0.50	mm
D1/E1	6.75 BSC			
D2	4.35	4.50	4.65	
E2	3.40	3.55	3.70	
e	0.40 BSC			mm
θ	0	–	14	°

1. Reference document: NT90-Y5241-1

4.2 Part marking

This device can be ordered using the identification code shown in [Section 4.3](#).

**Figure 4-2 Package marking layout****Table 4-2 Package marking identifiers**

Line	Marking
Line 1	QCA4002
Line 2	Assembly lot code
Line 3	Date code (YYWW)
Line 4	Country of origin (COO)

4.3 Device ordering information

QCA4002X-AL3A: a lead-free halogen-free standard-temperature version of the QCA4002.

QCA4002X-AL3B: a lead-free halogen-free industrial-temperature version of the QCA4002.

QCA4002X-BL3A: a lead-free halogen-free standard-temperature version of the QCA4002.

QCA4002X-BL3B: a lead-free halogen-free industrial-temperature version of the QCA4002.

4.4 Device moisture-sensitivity level

During device qualification, Qualcomm Atheros follows the latest revision IPC/JEDEC J-STD-020 standard to determine the IC's moisture-sensitivity level (MSL). See [Chapter 7](#) for more information.

To ensure proper SMT assembly, procedures must follow the MSL and maximum reflow temperature specified on the shipping bag labels or barcode labels accompanying all QCA4002 IC shipments.

Additional MSL information is included in:

- [Section 5.2](#) – Storage
- [Section 5.3](#) – Handling
- [Section 7.1](#) – Reliability qualifications summary
- *ASIC Packing Methods and Materials Specification (80-VK055-1)*

4.5 Thermal characteristics

Table 4-3 Device thermal resistance

Parameter	Comment	Typ	Unit
Ψ_{jT}	Thermal parameter	8.4	°C/W

5 Carrier, Storage, and Handling Information

5.1 Carrier

5.1.1 Tape and reel information

Carrier tape system conforms to the EIA-481 standard.

Simplified sketches of the QCA4002 tape carrier is shown in [Figure 5-1](#) and [Figure 5-2](#), including the part orientation. Tape and reel details for the QCA4002 are as follows:

- Reel diameter: 330 mm
- Hub size: 102 mm
- Tape width: 16 mm
- Tape pocket pitch: 12 mm
- Feed: Single
- Units per reel: 2,500

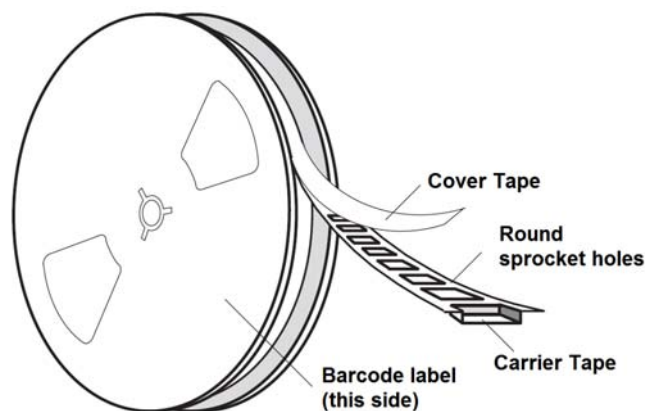


Figure 5-1 Tape orientation on reel

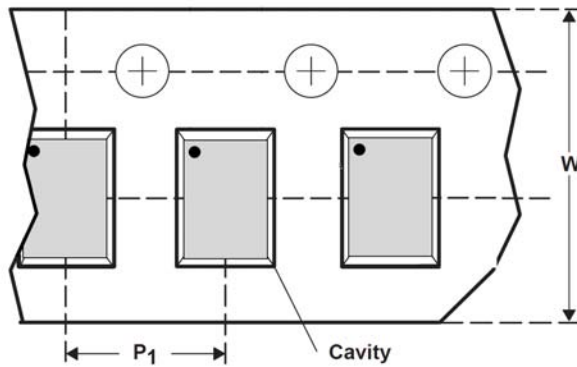


Figure 5-2 Part orientation in tape

5.1.2 Matrix tray information

All Qualcomm Atheros matrix tray carriers conform to JEDEC standards. The device pin 1 is oriented to the chamfered corner of the matrix tray. Each tray of the QCA4002 device contains up to 260 devices. See Figure 5-3 for matrix-tray key attributes and dimensions.

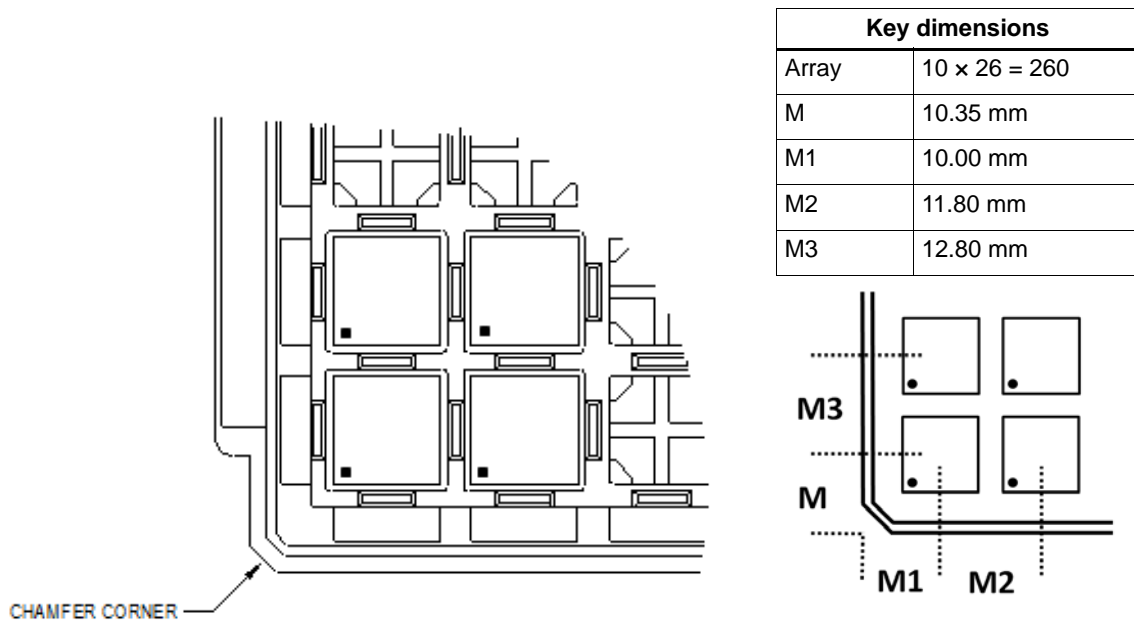


Figure 5-3 Matrix tray part orientation

5.2 Storage

5.2.1 Bag storage conditions

The packages described in this document must be stored in a nitrogen-purged, sealed moisture barrier antistatic bag. The Qualcomm-calculated shelf life in a sealed moisture bag is 60 months at < 40°C and < 90% relative humidity (RH).

5.2.2 Out of bag duration

After unpacking, the package must be soldered to the PCB within the factory floor life according to the MSL rating when factory conditions are < 30°C and < 60% RH, as specified in the IPC/JEDEC-STD-033 standard.

5.3 Handling

Tape handling was described in [Section 5.1.1](#). Other handling guidelines are presented below.

5.3.1 Baking

It is not necessary to bake the QCA4002 if the conditions specified in [Section 5.2.1](#) and [Section 5.2.2](#) have not been exceeded.

It is necessary to bake the QCA4002 if any condition specified in [Section 5.2.1](#) or [Section 5.2.2](#) has been exceeded. The baking conditions are specified on the moisture-sensitive caution label attached to each bag. See *ASIC Packing Methods and Materials Specification (80-VK055-1)* for details.

CAUTION If baking is required, the devices must be transferred into trays that can be baked to at least 125°C. Devices should not be baked in tape and reel carriers at any temperature.

5.3.2 Electrostatic discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result.

ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site.

Qualcomm products must be handled according to the ESD Association standard: *ANSI/ESD S20.20-1999, Protection of Electrical and Electronic Parts, Assemblies, and Equipment*.

5.4 Barcode label and packing for shipment

Refer to the *ASIC Packing and Materials Specification* (80-VK055-1) document for all packing-related information, including barcode label details.

6 PCB Mounting Guidelines

Guidelines for mounting the QCA4002 device onto a PCB are presented in this chapter, including land pad and stencil design details, surface mount technology (SMT) process characterization, and SMT process verification.

6.1 RoHS compliance

The device is externally lead-free and RoHS-compliant. Qualcomm Atheros defines its lead-free (or Pb-free) semiconductor products as having a maximum lead concentration of 1000 ppm (0.1% by weight) in raw (homogeneous) materials and end products. Qualcomm Atheros package environmental programs, RoHS compliance details, and tables defining pertinent characteristics of all Qualcomm Atheros IC products are described in the *IC Package Environmental Roadmap* (80-V6921-1).

6.2 SMT parameters

The information presented in this section describes Qualcomm Atheros board-level characterization process parameters. It is included to assist customers when starting their SMT process development; it is not intended to be a specification for customer SMT processes.

NOTE Qualcomm Atheros recommends that customers follow their solder paste vendor recommendations for the screen-printing process parameters and reflow profile conditions.

Qualcomm Atheros characterization tests attempt to optimize the SMT process for the best board-level reliability possible. This is done by performing physical tests on evaluation boards, which may include:

- Drop shock
- Temperature cycling
- Bend cycle (optional)

6.2.1 Land pad and stencil design

Qualcomm Atheros recommends characterizing the land patterns according to each customer's processes, materials, equipment, stencil design, and reflow profile **prior to PCB production**. Optimizing the solder stencil-pattern design and print process is critical to ensure print uniformity,

decrease voiding, and increase board-level reliability. See *PCB Land and Stencil Design Guide* (LS90-NG134-1) for characterization.

6.2.2 Reflow profile

Reflow profile conditions typically used by Qualcomm Atheros for SnPb and lead-free systems are given in [Table 6-1](#).

Table 6-1 Qualcomm Atheros typical SMT reflow profile conditions (for reference only)

Profile stage	Description	Temp range	Lead-free (high temperature condition limits)
Preheat	Initial ramp	< 150°C	3°C/sec max
Soak	Dry out and flux activation	150 to 190°C	60 to 120 sec
Ramp	Transition to liquidus (solder-paste melting point)	190 to 220°C	< 30 sec
Reflow	Time above liquidus	220 to 245°C ¹	50 to 70 sec
Cool down	Cool rate – ramp-to-ambient	< 220°C	6°C/sec max

1. During the reflow state, the peak temperature should not exceed 245°C. This temperature should not be confused with the peak temperature reached during MSL testing.

[Figure 6-1](#) shows the typical SMT reflow profile.

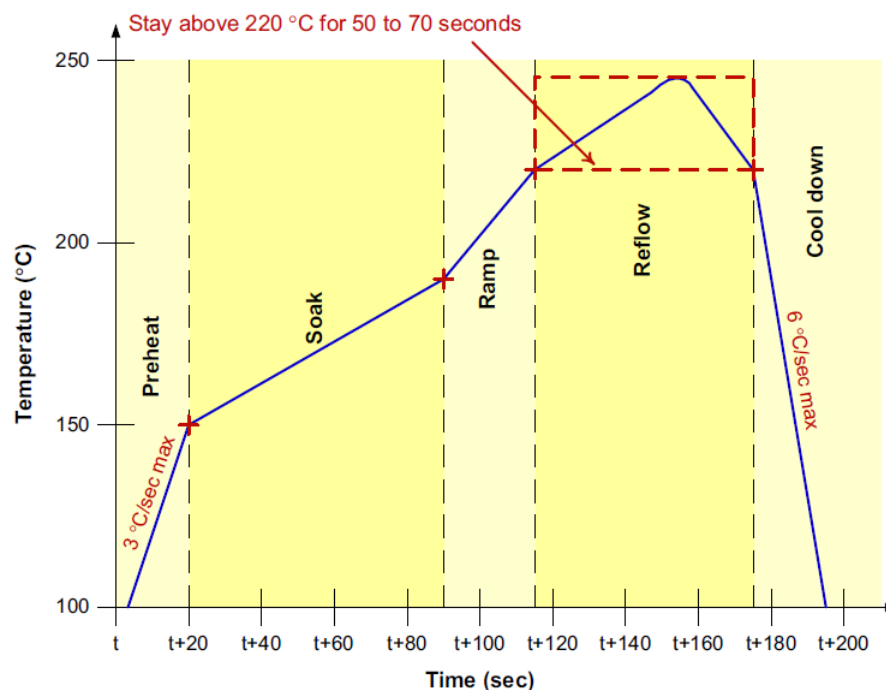


Figure 6-1 Typical SMT reflow profile

6.2.3 SMT peak package-body temperature

During a production board's reflow process, the temperature for the package must be controlled. The recommended peak temperature during production assembly is 245°C. This is comfortably above the solder melting point (220°C), yet well below the proven temperature reached during qualification (255°C or more).

Although the solder-paste manufacturer's recommendations for optimum temperature and duration for solder reflow must be followed, the Qualcomm Atheros recommended limits must not be exceeded.

6.2.4 SMT process verification

Qualcomm Atheros recommends verification of the SMT process prior to high-volume PCB fabrication, including:

- Electrical continuity
- X-ray inspection of the package installation for proper alignment, solder voids, solder balls, and solder bridging
- Visual inspection
- Cross-section inspection of solder joints to confirm registration, fillet shape, and print volume

6.3 Board-level reliability

Qualcomm Atheros conducts characterization tests to assess the device's board-level reliability, including the following physical tests on evaluation boards:

- Drop shock (JESD22-B111)
- Temperature cycling (JESD22-A104)
- (Optional) Cyclic bend testing (JESD22-B113)

See *Board-level Reliability* (BR80-NT096-1) for details.

7 Part Reliability

7.1 Reliability qualifications summary

Table 7-1 QCA4002 reliability evaluation

Reliability tests, standards, and conditions	Sample # Lots	Result	Assembly1	Assembly2
Average failure rate (AFR) in FIT (λ) Failure in billion device-hours Functional HTOL: JESD22-A108	231 3 lots	$\lambda = 20$ FIT	–	–
ESD – (HBM) human body model rating JESD22-A114-B	3	Pass ± 2000 V, all pins	–	–
ESD – (CDM) charge device model rating JESD22-C101-C	3	Pass ± 500 V, all pins except RFIN2P1 and RFIN2N1 pass ± 400 V	–	–
Latch-up (Overcurrent test): EIA/JESD78 Trigger current: ± 200 mA; temperature: 25°C	6 1 lot	Pass	–	–
Latch-up (Overvoltage test): EIA/JESD78 Trigger voltage: 1.6 x Vnom; temperature: 25°C	6 1 lot	Pass	–	–
High Temperature Storage Life (HTSL) JESD-22 A104, -50 to +150°C, 1000 hrs	462 3 + 3 lots	–	Pass	Pass
Moisture/Reflow Sensitivity Classification: MSL3; JSTD-020D, (30C/60% RH, 192 hrs, 3 x IR @ 260°C)	1078 3 + 3 lots	–	Pass	Pass
Temperature cycle: JESD22-A104 Temperature: -65 to +150 °C Number of cycles: 1000 Min soak time at min/max temperature: 5 minutes Cycle rate: 2 cycles per hour (cph) Prerequisite: All samples subjected to preconditioning MSL 3 and reflow (260°C) 3X prior to TC	462 3 + 3 lots	–	Pass	Pass
Highly accelerated stress test, unbiased (HAST) JESD22-A118 Prerequisite: All samples subjected to preconditioning MSL 3 and reflow (260°C) 3X prior to HAST	474 3 + 3 lots	–	Pass	Pass

Table 7-1 QCA4002 reliability evaluation

Reliability tests, standards, and conditions	Sample # Lots	Result	Assembly1	Assembly2
Highly accelerated stress test, biased (bHAST) JESD22-A118 Prerequisite: All samples subjected to preconditioning MSL 3 and reflow (260°C) 3X prior to HAST	158 1 + 1 lots	–	Pass	Pass
Die shear (5 kg)	5	–	Pass	Pass

7.2 Qualification sample description

- Device name: QCA4002
- Package type: QFN 56L
- Package body size: 7 mm × 7 mm × 0.85 mm
- Lead count: 56
- Lead pitch: 0.4 mm

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