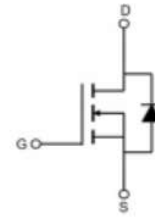


# AP12N10S

## N-Channel Enhancement Mosfet

### Feature

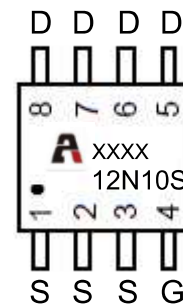
- 100V,12A  
 $R_{DS(ON)} < 10m\Omega @ V_{GS}=10V$  (TYP:8m $\Omega$ )  
 $R_{DS(ON)} < 13.5m\Omega @ V_{GS}=4.5V$  (TYP:11m $\Omega$ )
- Split Gate Trench Technology
- Lead free product is acquired
- Excellent  $R_{DS(ON)}$  and Low Gate Charge



Schematic Diagram

### Application

- PWM applications
- Load Switch
- Power management



Marking and pin assignment

### Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity (PCS)
12N10S	AP12N10S	SOP-8	13 inch	-	4000

### ABSOLUTE MAXIMUM RATINGS ( $T_a=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	$V_{DS}$	100	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current ( $T_a=25^\circ\text{C}$ )	$I_D$	12	A
Continuous Drain Current ( $T_a=100^\circ\text{C}$ )	$I_D$	9.6	A
Pulsed Drain Current <sup>(1)</sup>	$I_{DM}$	120	A
Singel Pulsed Avalanche Energy <sup>(2)</sup>	$E_{AS}$	45	mJ
Power Dissipation	$P_D$	3.1	W
Thermal Resistance from Junction to Ambient	$R_{\theta JA}$	40	$^\circ\text{C}/\text{W}$
Junction Temperature	$T_J$	150	$^\circ\text{C}$
Storage Temperature	$T_{STG}$	-55~ +150	$^\circ\text{C}$

# AP12N10S

N-Channel Enhancement Mosfet

# AIIPOWER

DATA SHEET

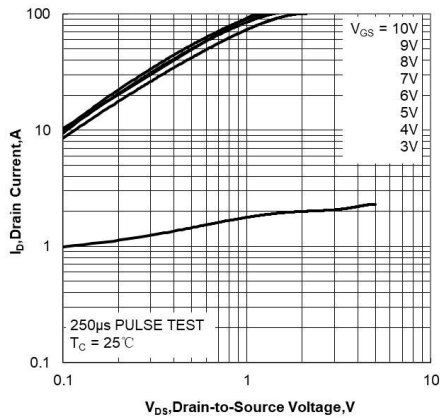
## MOSFET ELECTRICAL CHARACTERISTICS( $T_a=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Type	Max	Unit
<b>Static Characteristics</b>						
Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	100	-	-	V
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = 80V, V_{GS} = 0V$	-	-	1	$\mu A$
Gate-body leakage current	$I_{GSS}$	$V_{GS} = \pm 20V, V_{DS} = 0V$	-	-	$\pm 100$	nA
Gate threshold voltage <sup>(3)</sup>	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	1.2	2.0	2.5	V
Drain-source on-resistance <sup>(3)</sup>	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 12A$	-	8.0	10	m $\Omega$
		$V_{GS} = 4.5V, I_D = 8A$	-	11	13.5	
Forward Threshold Voltage	$g_{fs}$	$V_{DS} = 5V, I_D = 8A$	-	13.5	-	S
Gate Resistance	$R_g$	$V_{DS} = V_{GS} = 0V, f = 1MHz$	-	1.94	-	$\Omega$
<b>Dynamic characteristics</b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 50V, V_{GS} = 0V, f = 1MHz$	-	2122	-	pF
Output Capacitance	$C_{oss}$		-	618	-	
Reverse Transfer Capacitance	$C_{rss}$		-	25	-	
<b>Switching characteristics</b>						
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 50V, I_D = 10A,$ $V_{GS} = 10V, R_G = 3\Omega$	-	17	-	ns
Turn-on rise time	$t_r$		-	4	-	
Turn-off delay time	$t_{d(off)}$		-	32	-	
Turn-off fall time	$t_f$		-	8	-	
Total Gate Charge	$Q_g$	$V_{DS} = 50V, I_D = 10A,$ $V_{GS} = 10V$	-	41.8	-	nC
Gate-Source Charge	$Q_{gs}$		-	9	-	
Gate-Drain Charge	$Q_{gd}$		-	10	-	
Reverse Recovery Charge	$Q_{rr}$	$I_F = 10A, di/dt = 100A/\mu s$		71.5		nC
Reverse Recovery Time	$T_{rr}$	$I_F = 10A, di/dt = 100A/\mu s$		50.5		ns
<b>Source-Drain Diode characteristics</b>						
Diode Forward voltage <sup>(3)</sup>	$V_{DS}$	$V_{GS} = 0V, I_S = 10A$	-	-	1.2	V
Diode Forward current <sup>(4)</sup>	$I_S$		-	-	12	A

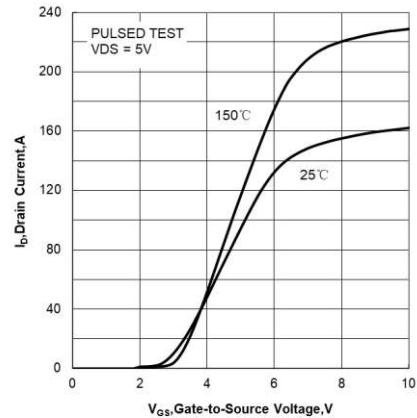
### Notes:

1. Repetitive Rating: pulse width limited by maximum junction temperature
2. EAS Condition:  $T_J = 25^{\circ}\text{C}, V_{DD} = 50V, R_G = 25\Omega, L = 0.5mH$
3. Pulse Test: pulse width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$
4. Surface Mounted on FR4 Board,  $t \leq 10$  sec

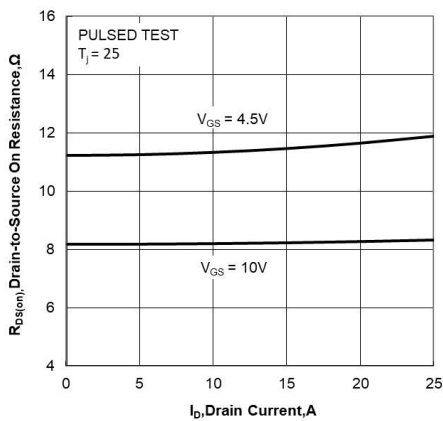
**Typical Performance Characteristics**



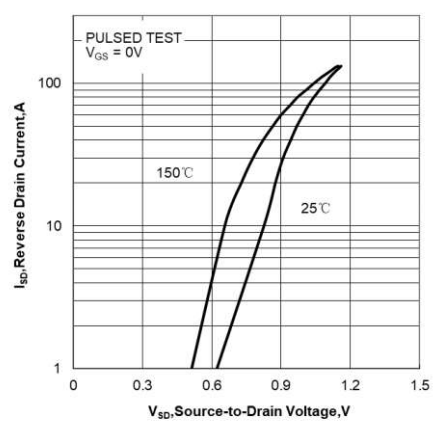
**Figure 1. Output Characteristics**



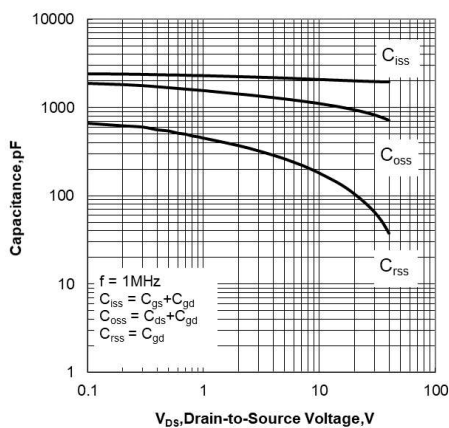
**Figure 2. Transfer Characteristics**



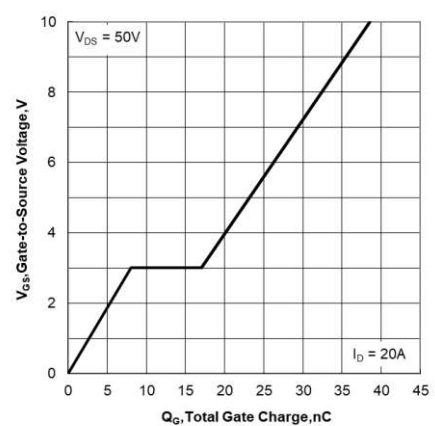
**Figure 3. Drain-to-Source On Resistance vs Drain Current**



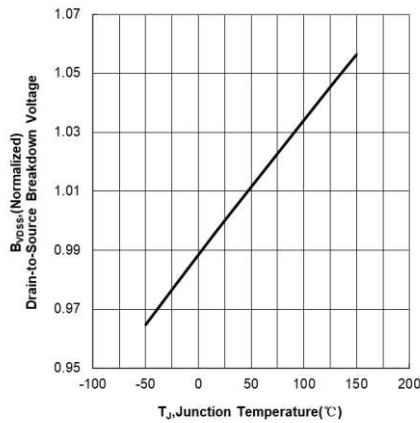
**Figure 4. Body Diode Forward Voltage vs Source Current and Temperature**



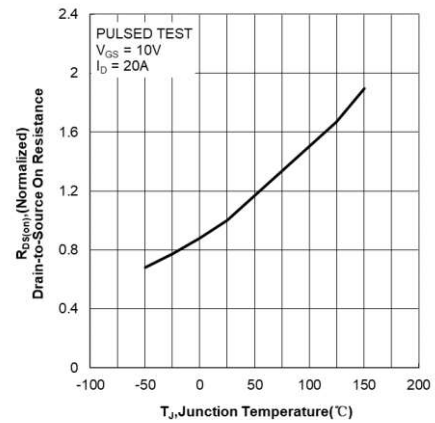
**Figure 5. Capacitance Characteristics**



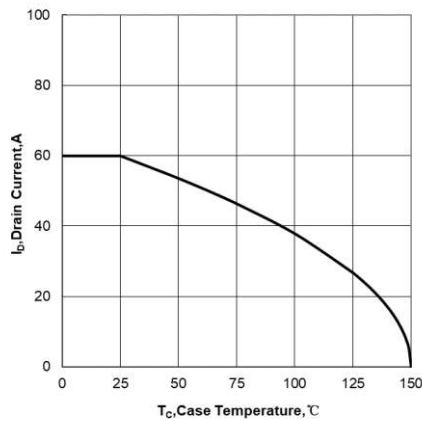
**Figure 6. Gate Charge Characteristics**



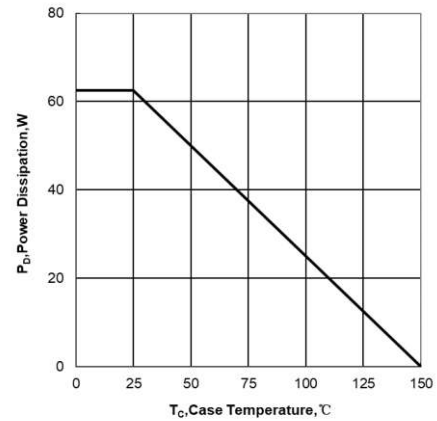
**Figure 7. Normalized Breakdown Voltage vs Junction Temperature**



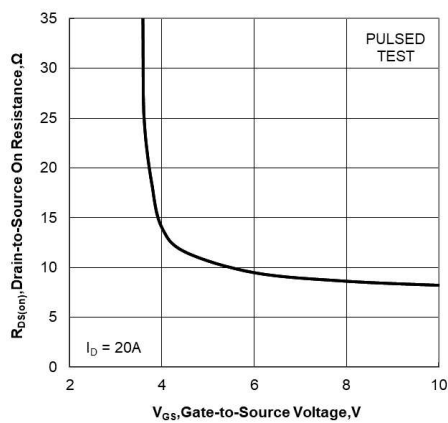
**Figure 8. Normalized On Resistance vs Junction Temperature**



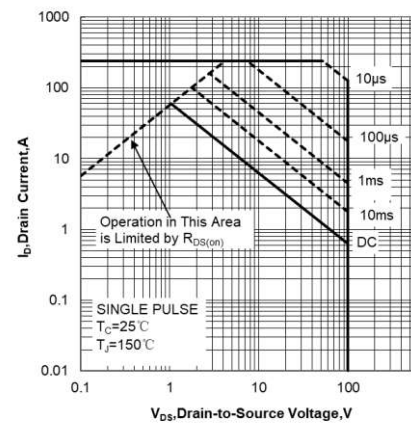
**Figure 9. Maximum Continuous Drain Current vs Case Temperature**



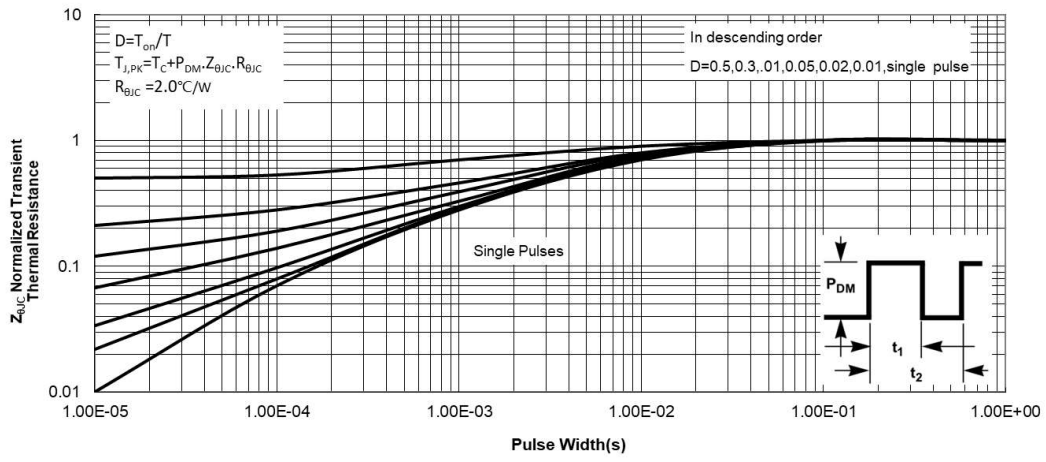
**Figure 10. Maximum Power Dissipation vs Case Temperature**



**Figure 11. Drain-to-Source On Resistance vs Gate Voltage and Drain Current**



**Figure 12. Maximum Safe Operating Area**

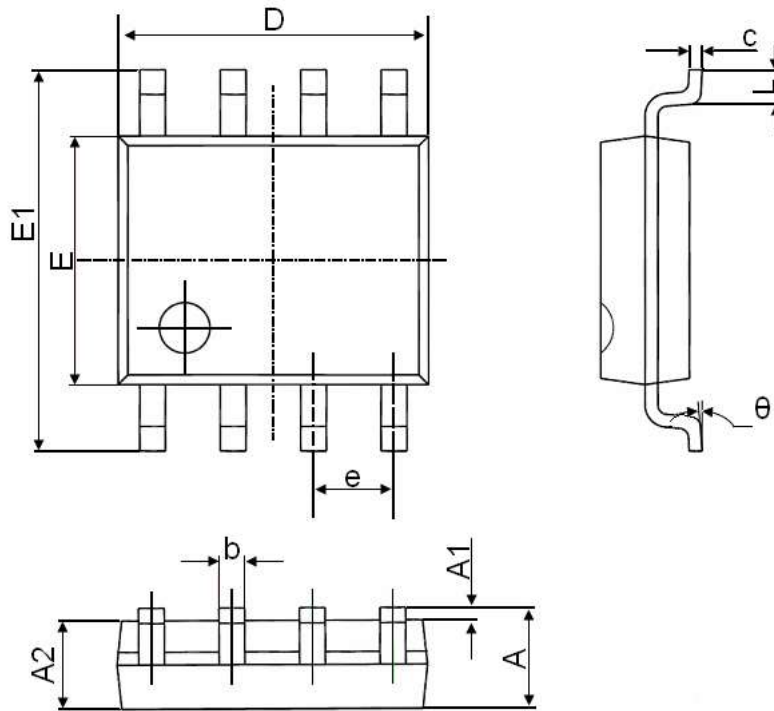


**Figure 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case**

# AP12N10S

N-Channel Enhancement Mosfet

### SOP-8 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
$\theta$	0°	8°	0°	8°

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