

AP2317SD

P-Channel Power MOSFET

Description

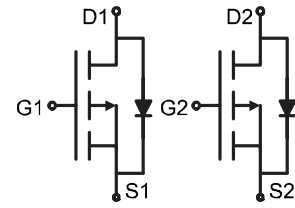
The AP2317SD uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a load switch or in PWM applications.

General Features

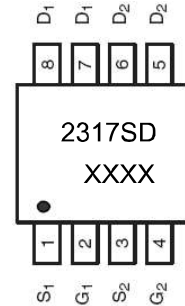
- $V_{DS} = -20V, I_D = -8A$
 $R_{DS(ON)} < 28m\Omega(max) @ V_{GS} = -2.5V$
 $R_{DS(ON)} < 20m\Omega(max) @ V_{GS} = -4.5V$
- High power and current handling capability
- Lead free product is acquired
- Surface mount package

Application

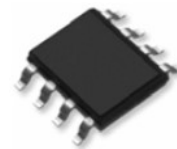
- PWM applications
- Load switch
- Power management
- Halogen-free



Schematic diagram



Marking and pin assignment



SOP-8 top view

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
2317SD	AP2317SD	SOP-8	Ø330mm	12 mm	4000 units

Absolute Maximum Ratings (TA=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	±12	V
Drain Current -Continuous	I_D	-8	A
Drain Current -Pulsed ^(Note 1)	I_{DM}	-45	A
Maximum Power Dissipation	P_D	3.0	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	°C

Thermal Characteristic

Thermal Resistance, Junction-to-Ambient ^(Note 2)	$R_{\theta JA}$	42	°C/W
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Electrical Characteristics (TA=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=-250\mu A$	-20	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-12V, V_{GS}=0V$	-	-	-1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 12V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.4	-0.65	-1.0	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=-4.5V, I_D=-6A$	-	17	20	m Ω
		$V_{GS}=-2.5V, I_D=-5A$	-	22	28	
Forward Transconductance	g_{FS}	$V_{DS}=-5V, I_D=-6A$		20	-	S
Dynamic Characteristics (Note 4)						
Input Capacitance	C_{iss}	$V_{DS}=-6V, V_{GS}=0V,$ $F=1.0MHz$	-	1730	-	PF
Output Capacitance	C_{oss}		-	320	-	PF
Reverse Transfer Capacitance	C_{rss}		-	210	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=-6V, I_D=-1A,$ $R_L=6\Omega, V_{GEN}=-4.5V, R_g=6\Omega$	-	20	-	nS
Turn-on Rise Time	t_r		-	35	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	90	-	nS
Turn-Off Fall Time	t_f		-	70	-	nS
Total Gate Charge	Q_g	$V_{DS}=-6V, I_D=-6A, V_{GS}=-4.5V$	-	19.5	-	nC
Gate-Source Charge	Q_{gs}		-	4.1	-	nC
Gate-Drain Charge	Q_{gd}		-	5.2	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	$V_{GS}=0V, I_S=-1.0A$	-	-	-1.2	V
Diode Forward Current (Note 2)	I_S		-	-	-8	A

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production

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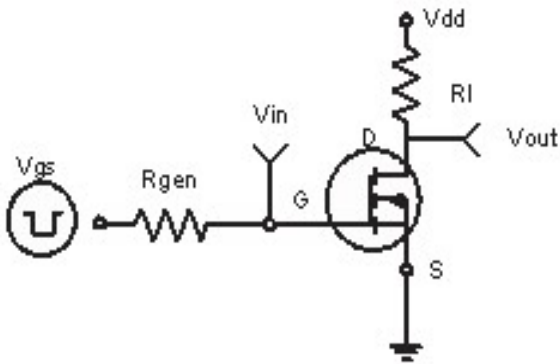


Figure 1: Switching Test Circuit

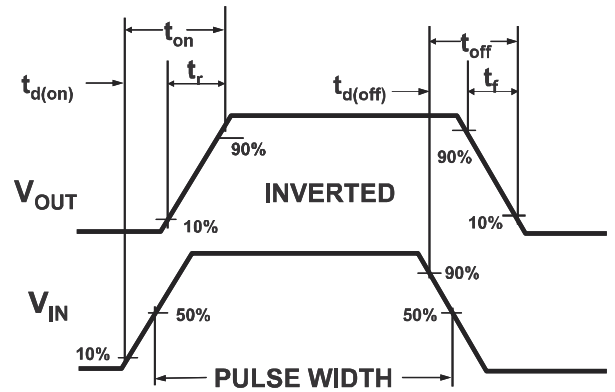


Figure 2: Switching Waveforms

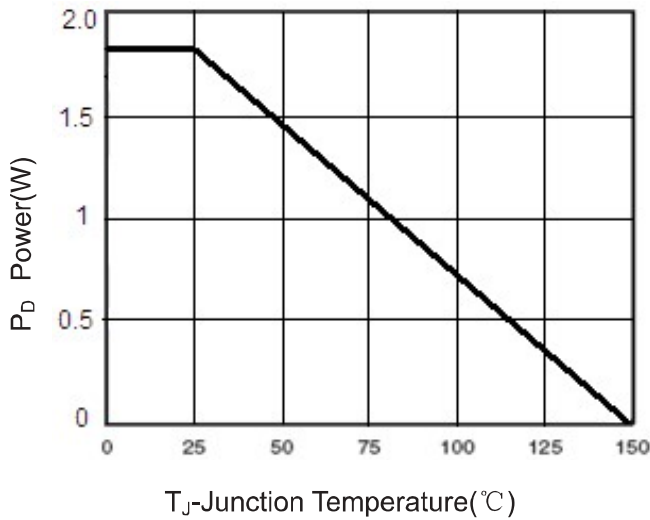


Figure 3 Power Dissipation

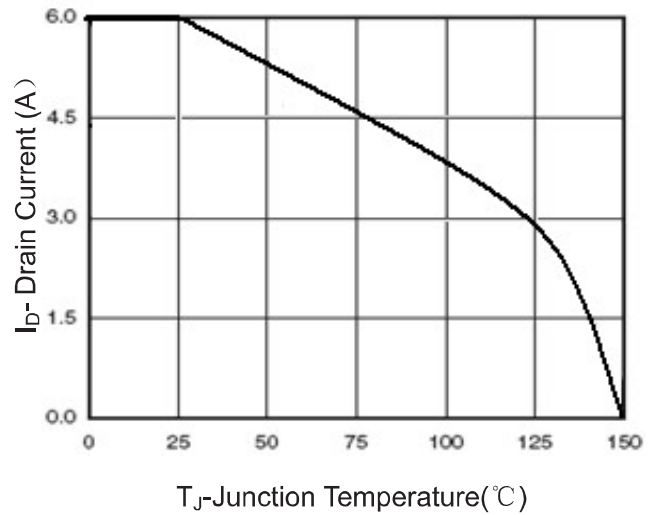


Figure 4 Drain Current

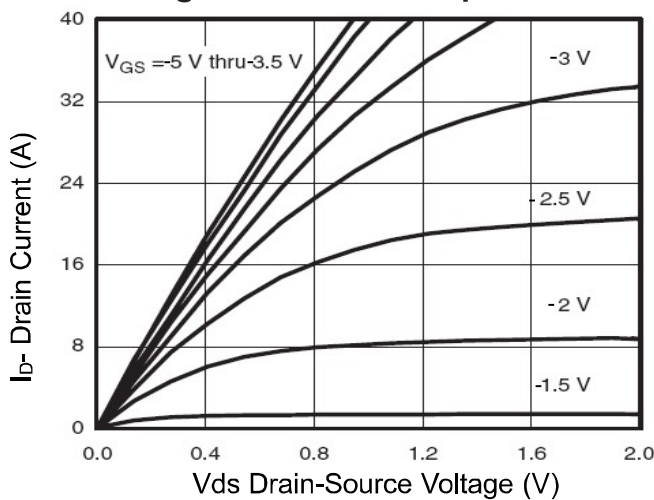


Figure 5 Output Characteristics

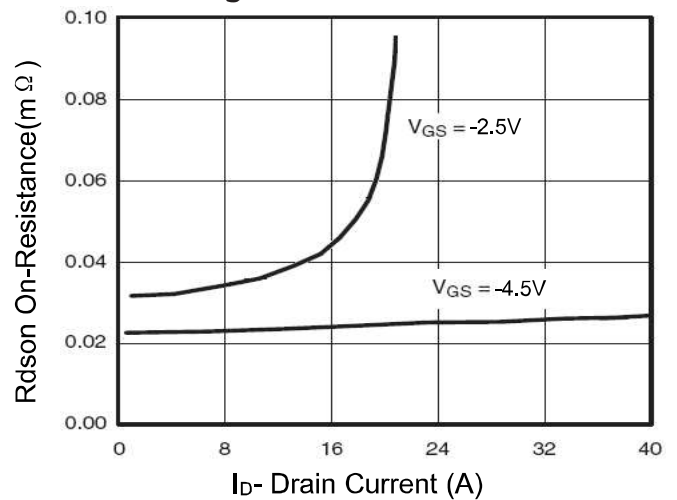


Figure 6 Drain-Source On-Resistance

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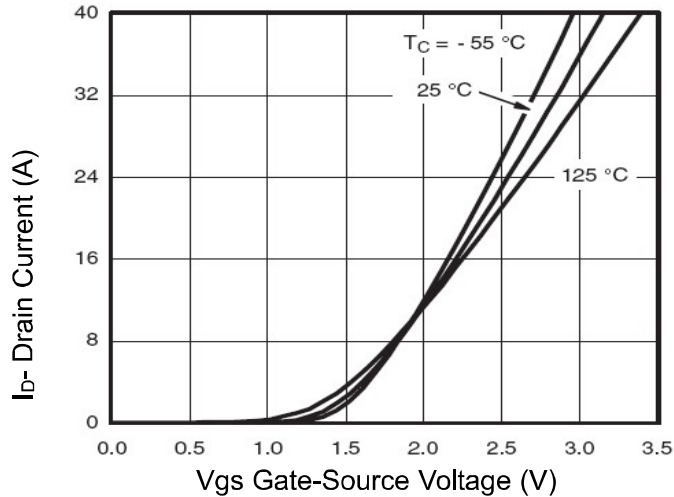


Figure 7 Transfer Characteristics

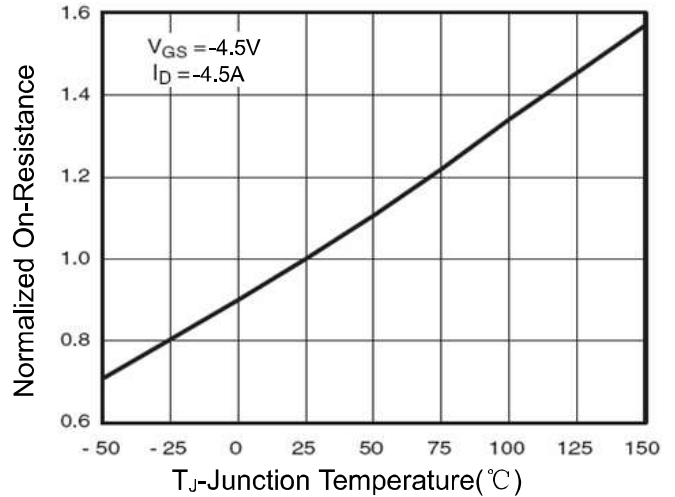


Figure 8 Drain-Source On-Resistance

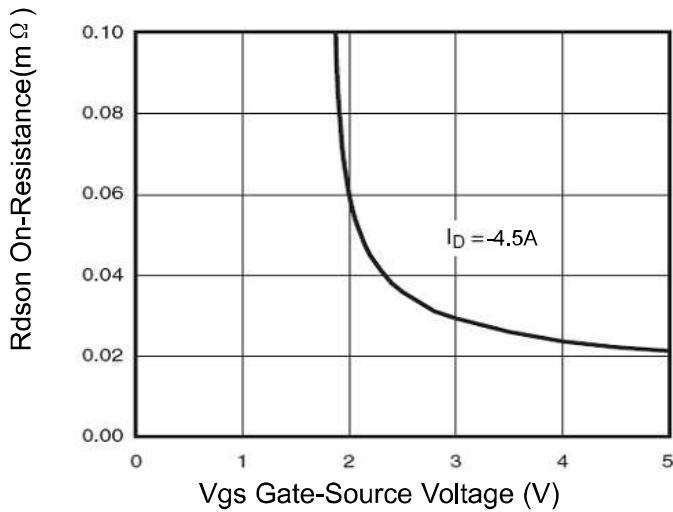


Figure 9 Rdson vs Vgs

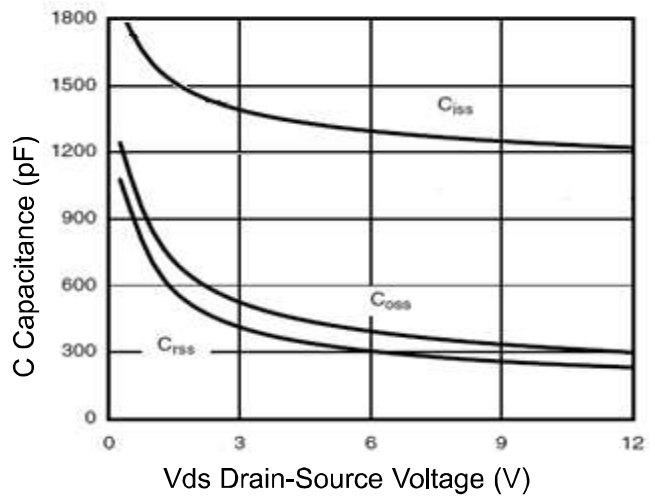


Figure 10 Capacitance vs Vds

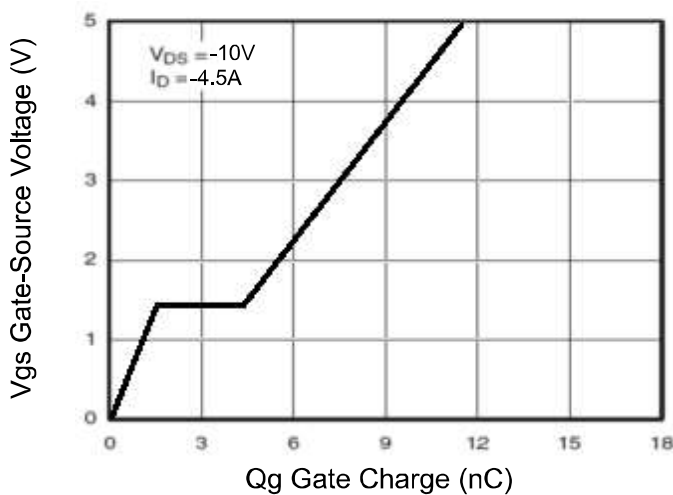


Figure 11 Gate Charge

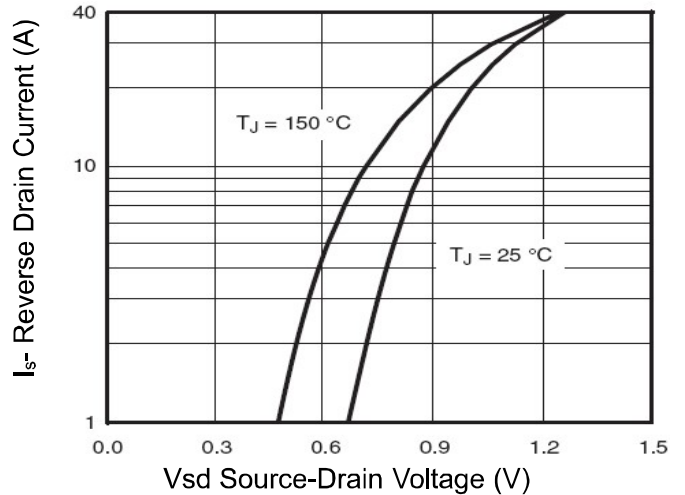


Figure 12 Source- Drain Diode Forward

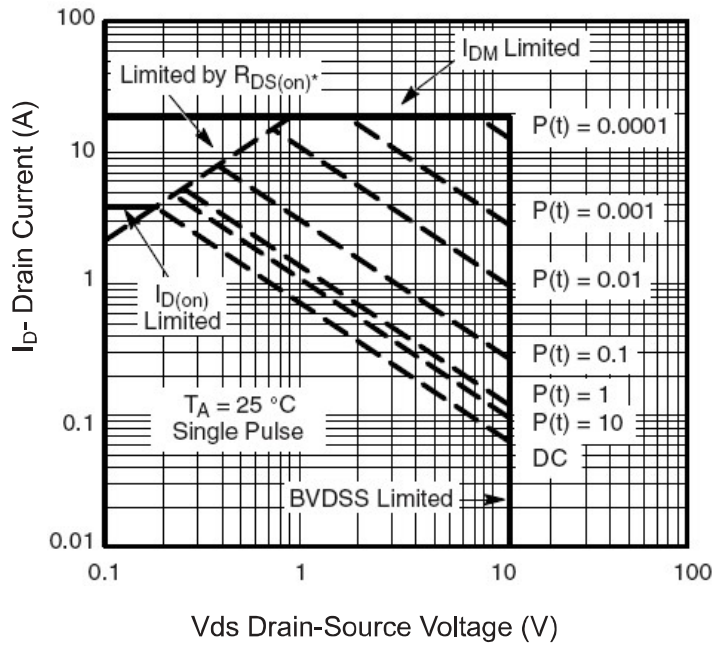


Figure 13 Safe Operation Area

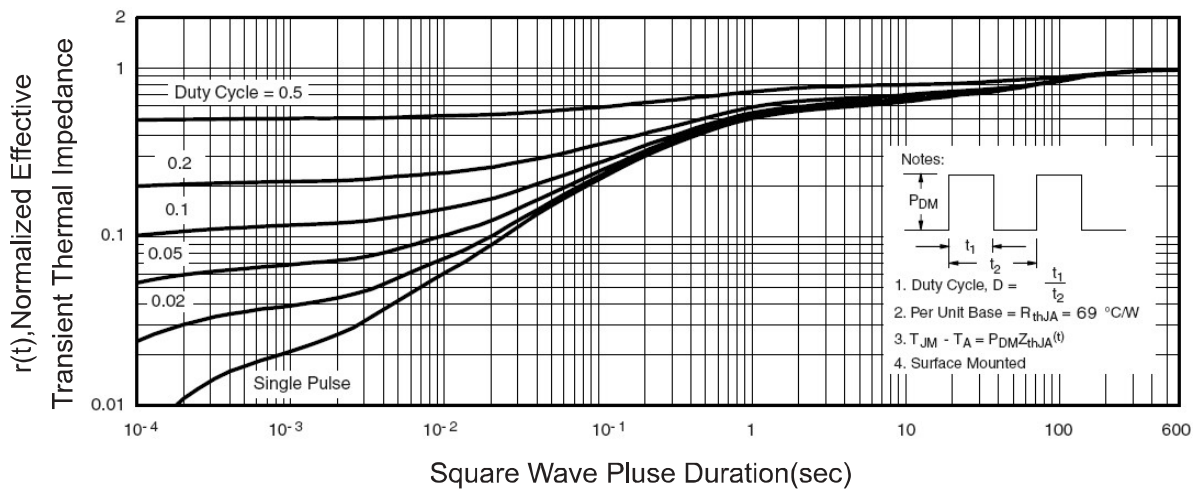
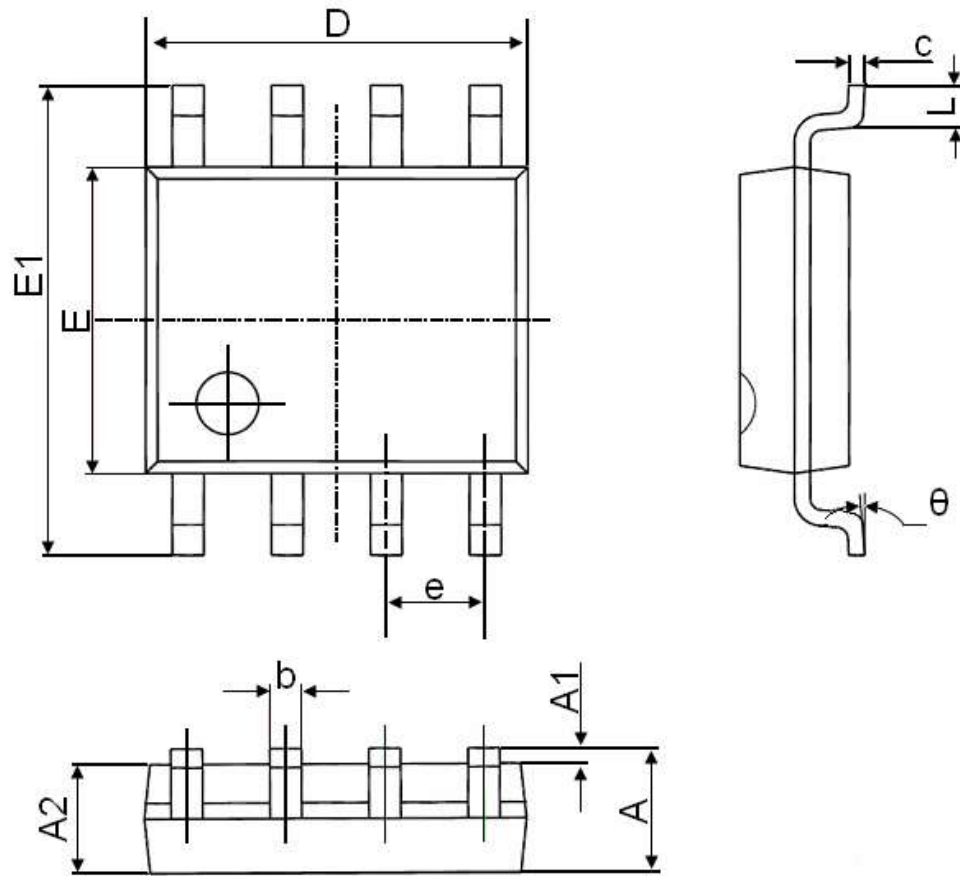


Figure 14 Normalized Maximum Transient Thermal Impedance

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SOP-8 Package Information



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