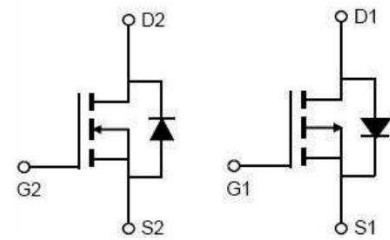


# AP2714QD

## N and P-Channel Enhancement Mosfet

### Feature

- N-Channel**  
 $V_{DD}=40V, I_D=16A$   
 $R_{DS(ON)} < 22m\Omega @ V_{GS}=10V$   
 $R_{DS(ON)} < 30m\Omega @ V_{GS}=4.5V$
- P-Channel**  
 $V_{DD}=-40V, I_D=-18A$   
 $R_{DS(ON)} < 35m\Omega @ V_{GS}=-10V$   
 $R_{DS(ON)} < 50m\Omega @ V_{GS}=-4.5V$
- Lead free product is acquired
- High power and current handling capability
- Surface mount package



N-channel P-channel

Schematic diagram



Marking and pin assignment

### Application

- PWM applications
- Load Switch
- Power management

### Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity (PCS)
2714QD	AP2714QD	PDFN3X3	13 inch	-	5000

### ABSOLUTE MAXIMUM RATINGS ( $T_a=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage	$V_{DS}$	40	-40	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	$\pm 20$	V
Continuous Drain Current ( $T_a = 25^\circ\text{C}$ )	$I_D$	16	-18	A
Continuous Drain Current ( $T_a = 100^\circ\text{C}$ )	$I_D$	10.2	-11.2	A
Pulsed Drain Current <sup>(1)</sup>	$I_{DM}$	40	-45	A
Power Dissipation	$P_D$	21		W
Thermal Resistance from Junction to Ambient	$R_{\theta JA}$	6.25		$^\circ\text{C/W}$
Junction Temperature	$T_J$	150		$^\circ\text{C}$
Storage Temperature	$T_{STG}$	-55~ +150		$^\circ\text{C}$

**N-CH ELECTRICAL CHARACTERISTICS(T<sub>a</sub>=25°C unless otherwise noted)**

Parameter	Symbol	Test Condition	Min	Type	Max	Unit
<b>Static Characteristics</b>						
Drain-source breakdown voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = -250μA	40			V
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = 100V, V <sub>GS</sub> = 0V			1	μA
Gate-body leakage current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20V, V <sub>DS</sub> = 0V			±100	nA
Gate threshold voltage <sup>(2)</sup>	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	1	1.6	2.5	V
Drain-source on-resistance <sup>(2)</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 10A		17	22	mΩ
		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 6A		22	30	
<b>Dynamic characteristics</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0V, f = 1MHz		1050		pF
Output Capacitance	C <sub>oss</sub>			84		
Reverse Transfer Capacitance	C <sub>rss</sub>			72		
<b>Switching characteristics</b>						
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = 20V, I <sub>D</sub> = 5A, R <sub>L</sub> = 6Ω V <sub>GS</sub> = 10V, R <sub>G</sub> = 1Ω		11		ns
Turn-on rise time	t <sub>r</sub>			13		
Turn-off delay time	t <sub>d(off)</sub>			36		
Turn-off fall time	t <sub>f</sub>			9		
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 20V, I <sub>D</sub> = 5A, V <sub>GS</sub> = 10V		11		nC
Gate-Source Charge	Q <sub>gs</sub>			1.9		
Gate-Drain Charge	Q <sub>gd</sub>			2.2		
<b>Source-Drain Diode characteristics</b>						
Diode Forward voltage <sup>(2)</sup>	V <sub>DS</sub>	V <sub>GS</sub> = 0V, I <sub>S</sub> = 10A			1.2	V
Diode Forward current <sup>(3)</sup>	I <sub>S</sub>		-	-	10	A

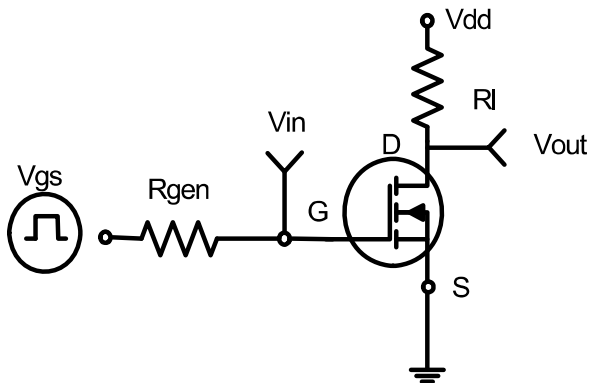
**P-CH ELECTRICAL CHARACTERISTICS(T<sub>a</sub>=25°C unless otherwise noted)**

Parameter	Symbol	Test Condition	Min	Type	Max	Unit
<b>Static Characteristics</b>						
Drain-source breakdown voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = -250μA	-40			V
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = -40V, V <sub>GS</sub> = 0V			1	μA
Gate-body leakage current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20V, V <sub>DS</sub> = 0V			±100	nA
Gate threshold voltage <sup>(2)</sup>	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250μA	-1	-1.6	-2.5	V
Drain-source on-resistance <sup>(2)</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = -10V, I <sub>D</sub> = -8A		27	35	mΩ
		V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -5A		35	50	
<b>Dynamic characteristics</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = -20V, V <sub>GS</sub> = 0V, f = 1MHz		1415		pF
Output Capacitance	C <sub>oss</sub>			134		
Reverse Transfer Capacitance	C <sub>rss</sub>			102		
<b>Switching characteristics</b>						
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = -20V, I <sub>D</sub> = -5A, R <sub>L</sub> = 6Ω V <sub>GS</sub> = -10V, R <sub>G</sub> = 1Ω		22		ns
Turn-on rise time	t <sub>r</sub>			16		
Turn-off delay time	t <sub>d(off)</sub>			59		
Turn-off fall time	t <sub>f</sub>			6		
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = -20V, I <sub>D</sub> = -5A, V <sub>GS</sub> = -10V		11.5		nC
Gate-Source Charge	Q <sub>gs</sub>			3.5		
Gate-Drain Charge	Q <sub>gd</sub>			3.2		
<b>Source-Drain Diode characteristics</b>						
Diode Forward voltage <sup>(2)</sup>	V <sub>DS</sub>	V <sub>GS</sub> = 0V, I <sub>S</sub> = -12A			1.2	V
Diode Forward current <sup>(3)</sup>	I <sub>S</sub>		-	-	-12	A

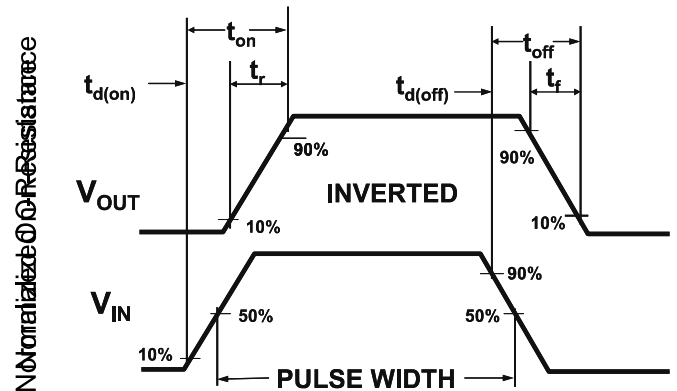
**Notes:**

1. Repetitive Rating: pulse width limited by maximum junction temperature
2. Pulse Test: pulse width ≤ 300μs, duty cycle ≤ 2%
3. Surface Mounted on FR4 Board, t ≤ 10 sec

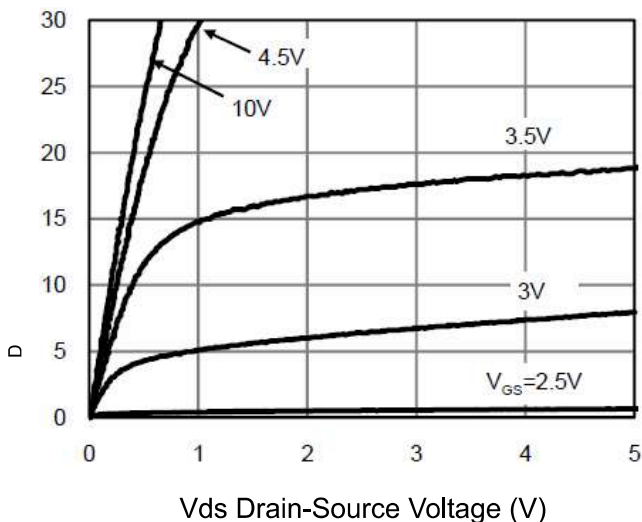
N-Channel



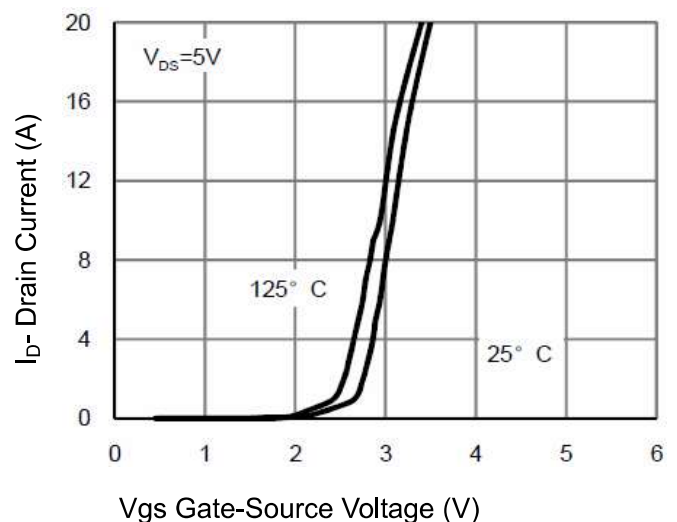
**Figure 1: Switching Test Circuit**



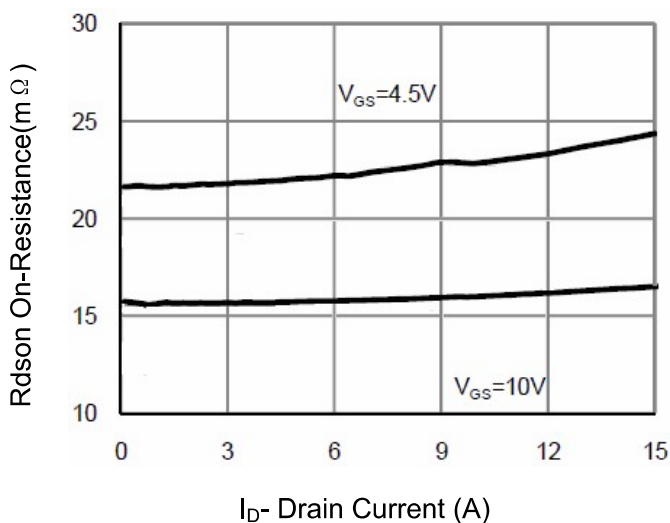
**Figure 2: Switching Waveforms**



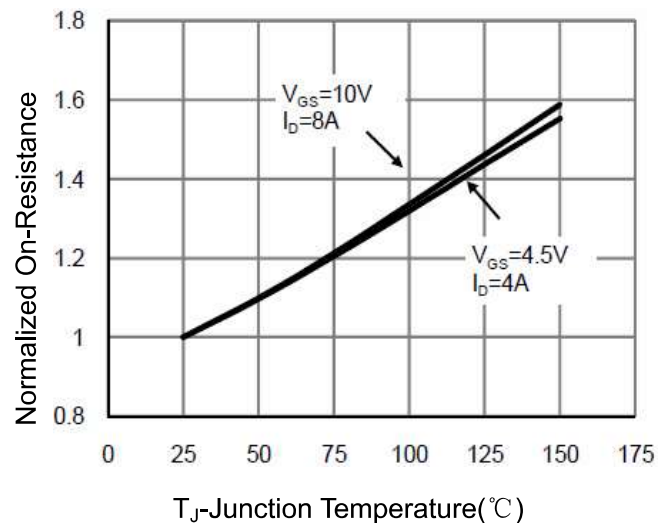
**Figure 3 Output Characteristics**



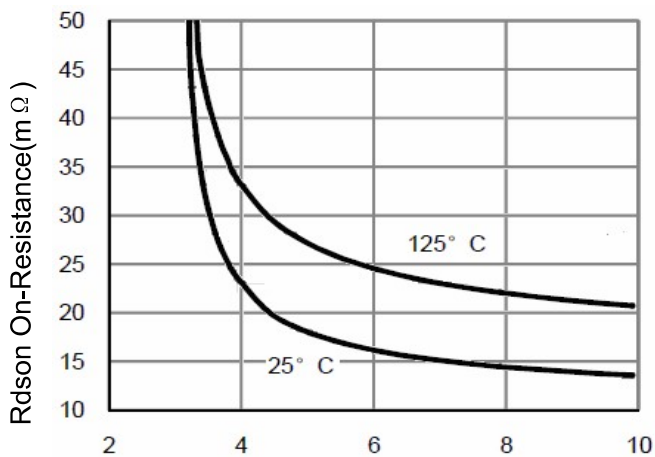
**Figure 4 Transfer Characteristics**



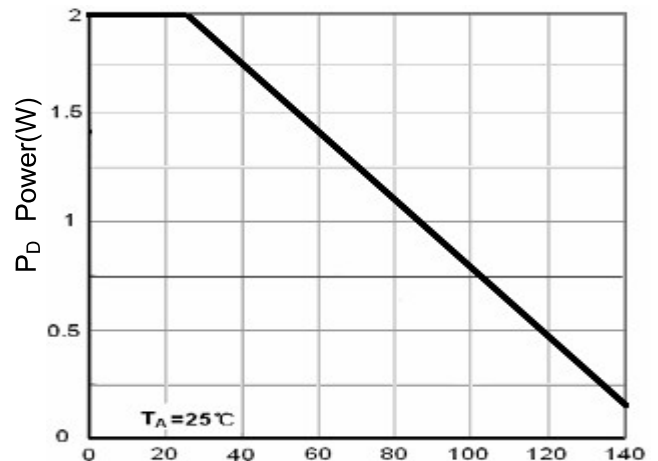
**Figure 5 Drain-Source On-Resistance**



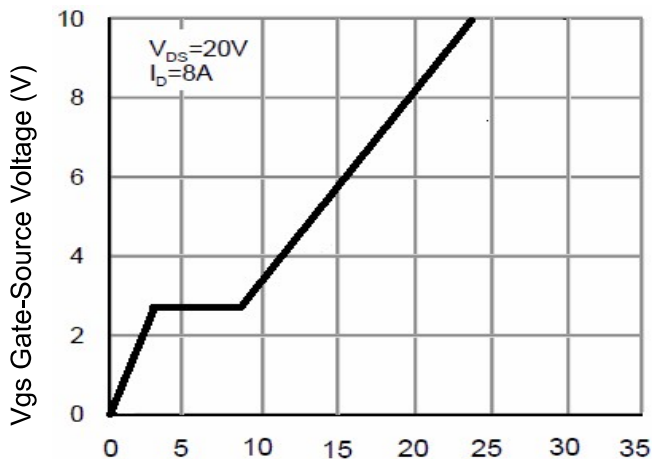
**Figure 6 Drain-Source On-Resistance**



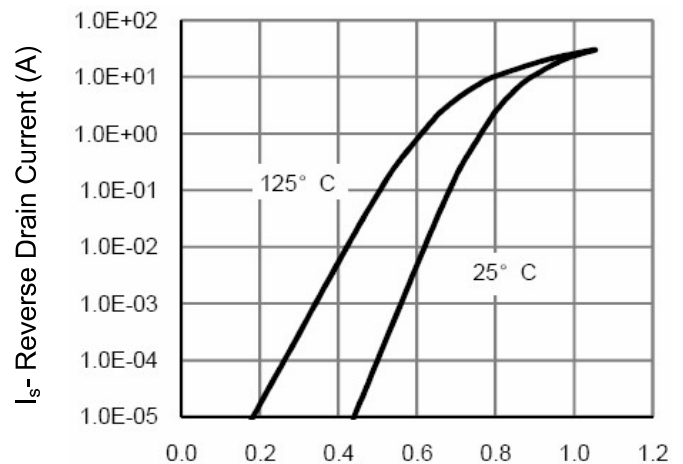
Vgs Gate-Source Voltage (V)  
**Figure 7 Rdson vs Vgs**



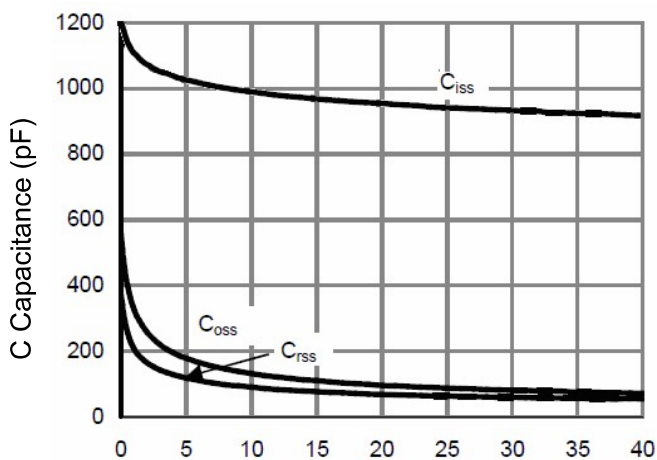
T<sub>J</sub>-Junction Temperature(°C)  
**Figure 8 Power Dissipation**



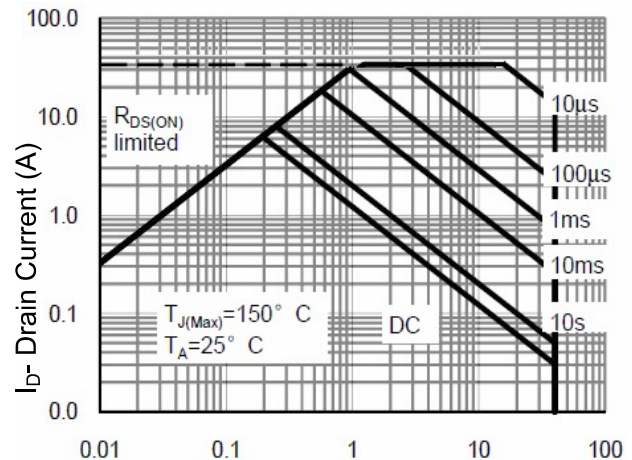
Qg Gate Charge (nC)  
**Figure 9 Gate Charge**



Vds Drain-Source Voltage (V)  
**Figure 10 Source- Drain Diode Forward**

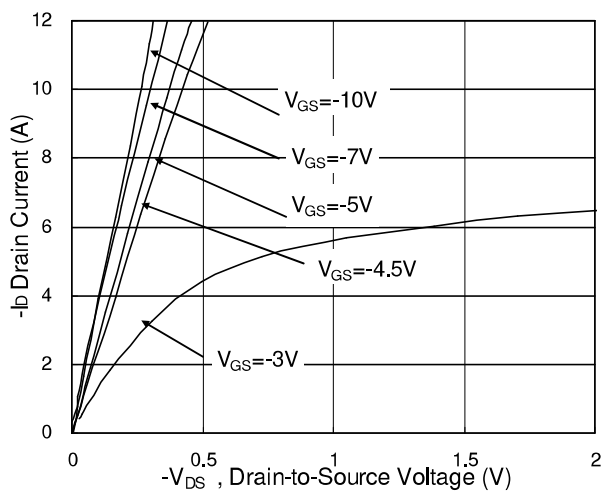


Vds Drain-Source Voltage (V)  
**Figure 11 Capacitance vs Vds**

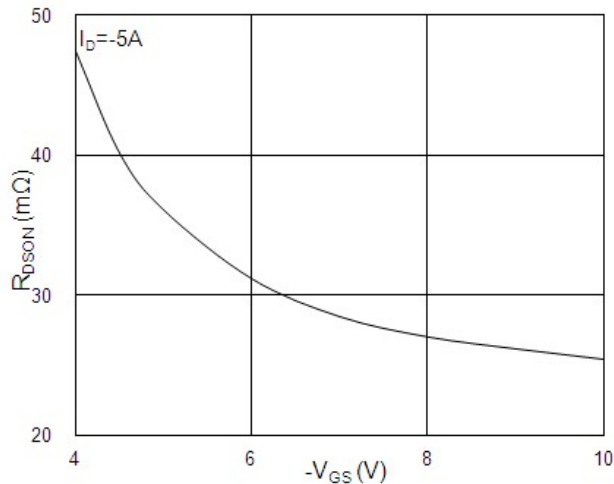


Vds Drain-Source Voltage (V)  
**Figure 12 Safe Operation Area**

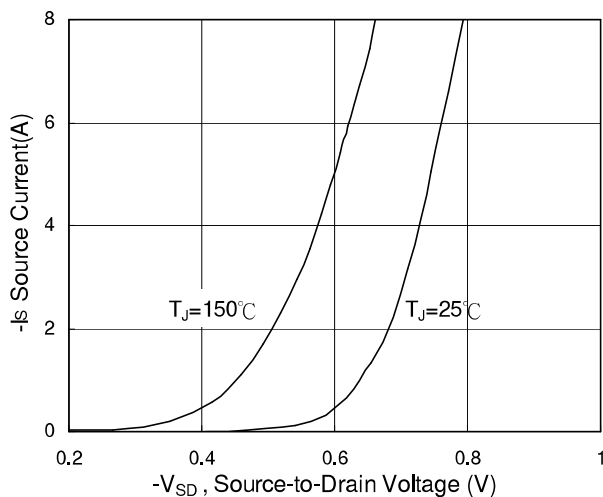
P-Channel



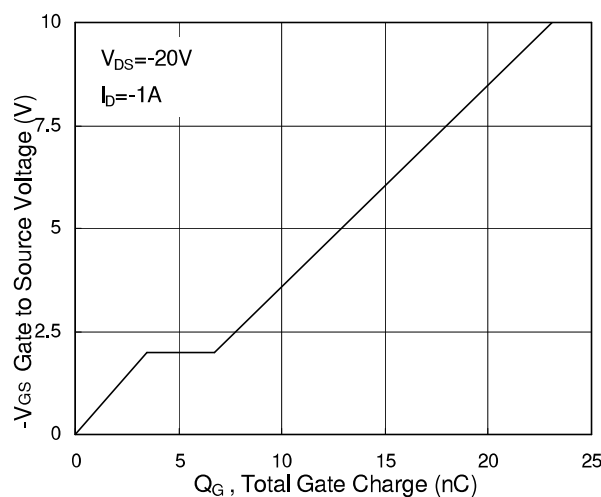
**Fig.1 Typical Output Characteristics**



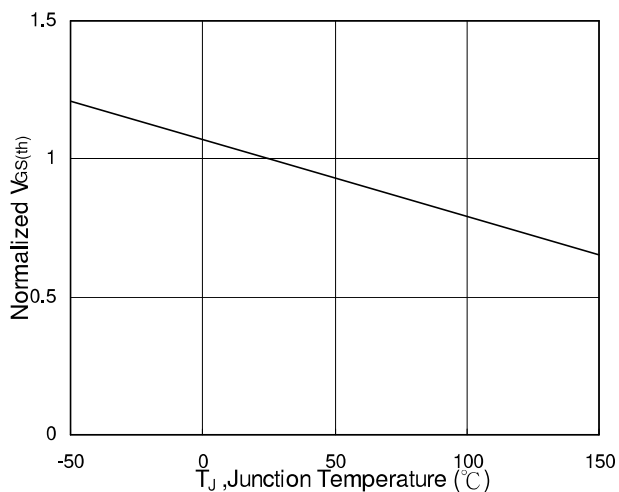
**Fig.2 On-Resistance v.s Gate-Source**



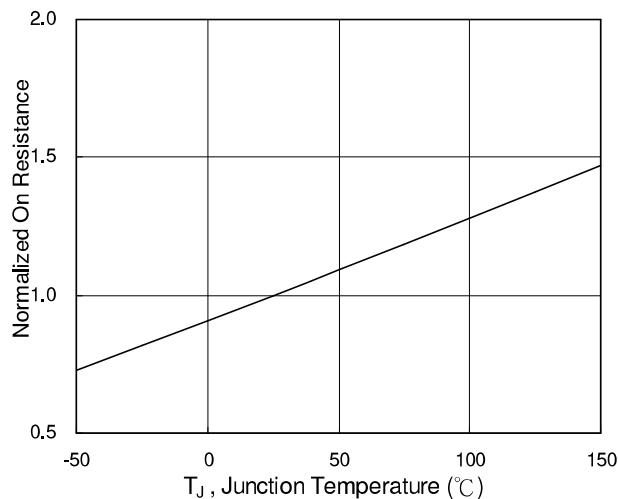
**Fig.3 Forward Characteristics Of Reverse**



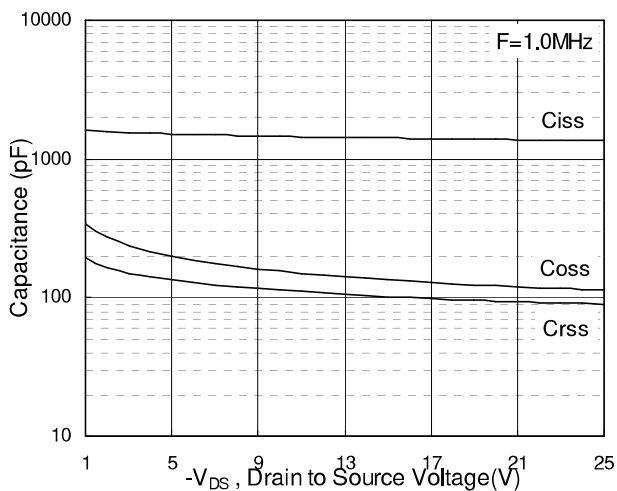
**Fig.4 Gate Charge Characteristics**



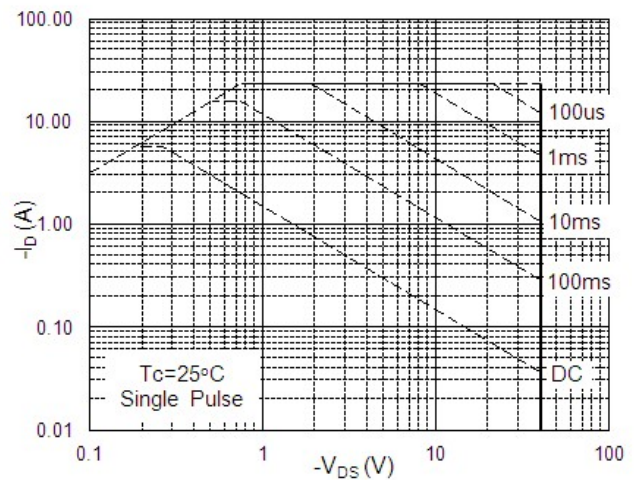
**Fig.5 Normalized  $V_{GS(th)}$  vs.  $T_J$**



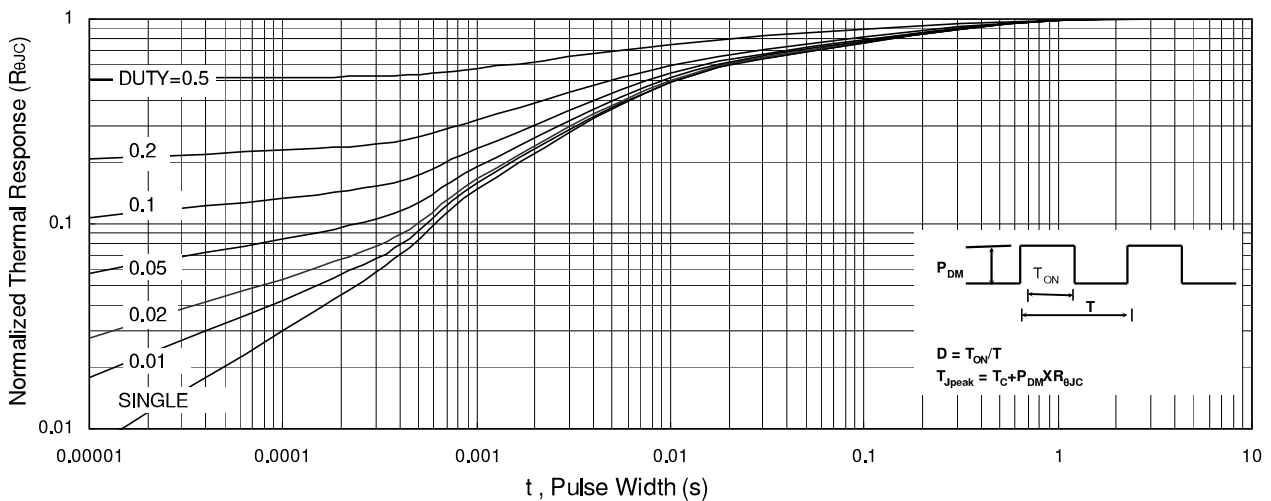
**Fig.6 Normalized  $R_{DS(on)}$  vs.  $T_J$**



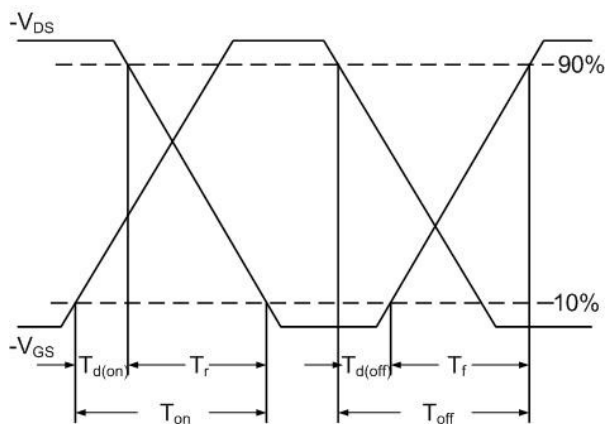
**Fig.7 Capacitance**



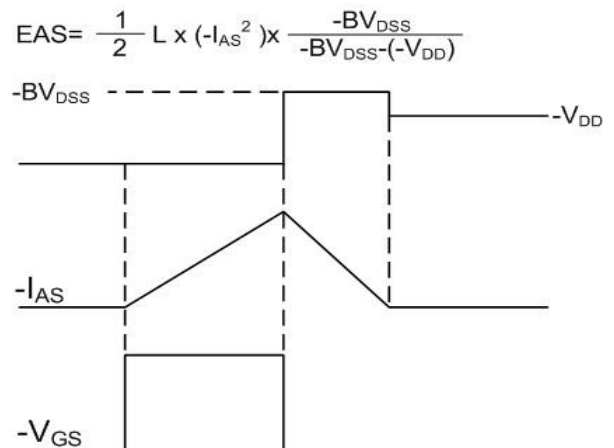
**Fig.8 Safe Operating Area**



**Fig.9 Normalized Maximum Transient Thermal Impedance**

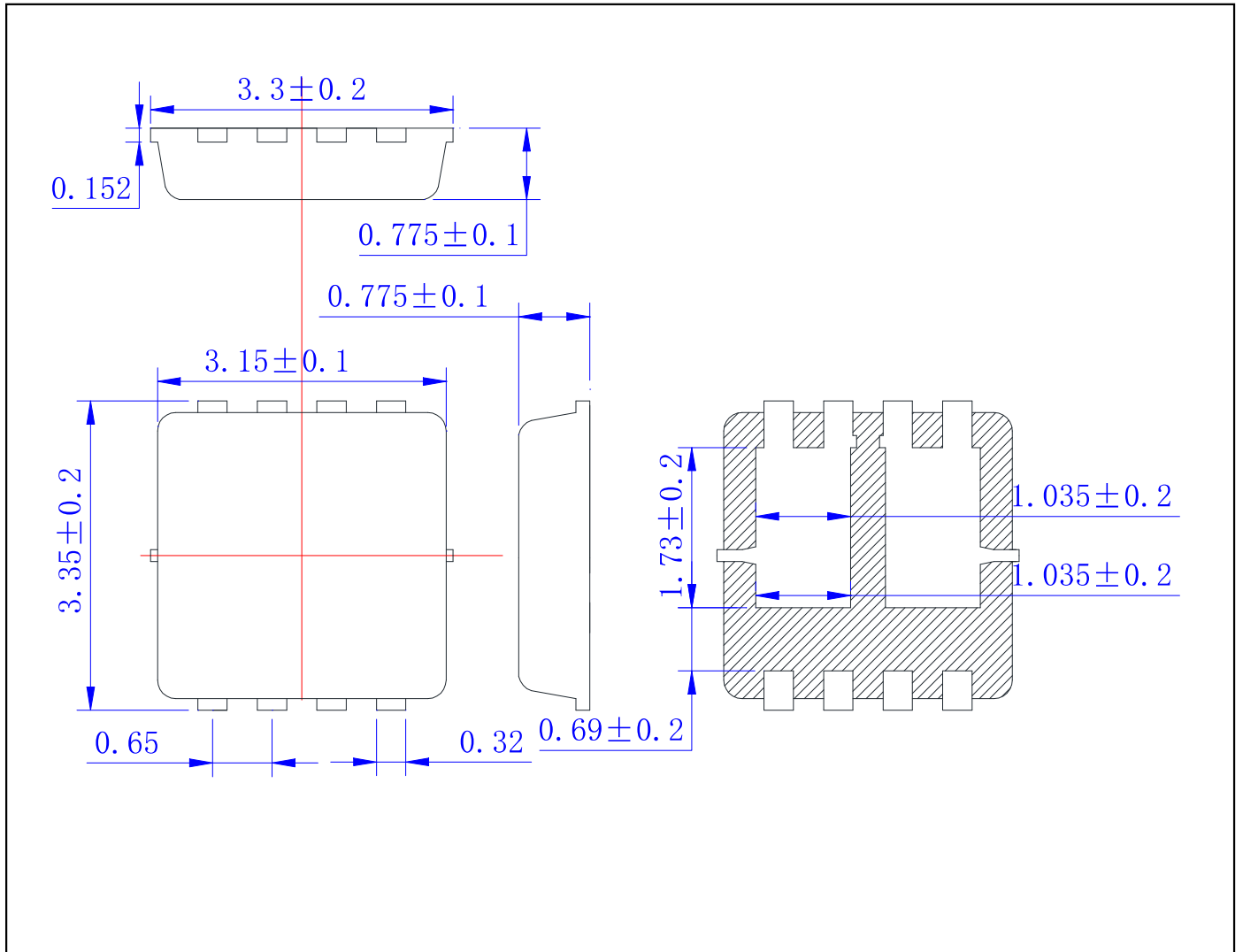


**Fig.10 Switching Time Waveform**



**Fig.11 Unclamped Inductive Switching**

**PACKAGE OUTLINE DIMENSIONS**





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