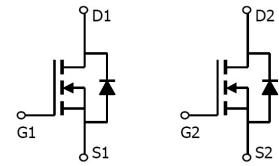


Feature

- 40V,20A
 $R_{DS(ON)} < 15m\Omega @ V_{GS}=10V$ TYP:13 m Ω
 $R_{DS(ON)} < 20m\Omega @ V_{GS}=4.5V$ TYP:17 m Ω
- Advanced Trench Technology
- Lead free product is acquired
- Excellent $R_{DS(ON)}$ and Low Gate Charge



Schematic diagram

Application

- PWM applications
- Load Switch
- Power management



Marking and pin assignment

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity (PCS)
50N04QD	AP50N04QD	PDFN3X3	13 inch	-	5000

ABSOLUTE MAXIMUM RATINGS (T_a=25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V _{DS}	40	V
Gate-Source Voltage	V _{GS}	±20	V
Continuous Drain Current (T _a =25°C)	I _D	20	A
Continuous Drain Current (T _a =100°C)	I _D	14	A
Pulsed Drain Current ⁽¹⁾	I _{DM}	60	A
Singel Pulsed Avalanche Energy ⁽²⁾	E _{AS}	12.25	mJ
Power Dissipation	P _D	35	W
Thermal Resistance from Junction to Case ⁽⁴⁾	R _{θJC}	3.6	°C/W
Junction Temperature	T _J	150	°C
Storage Temperature	T _{STG}	-55~ +150	°C

MOSFET ELECTRICAL CHARACTERISTICS($T_a=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Type	Max	Unit
Static Characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	40	-	-	V
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 40V, V_{GS} = 0V$	-	-	1	μA
Gate-body leakage current	I_{GSS}	$V_{GS} = \pm 20V, V_{DS} = 0V$	-	-	± 100	nA
Gate threshold voltage ⁽³⁾	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	1	1.5	2.5	V
Drain-source on-resistance ⁽³⁾	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 10A$	-	13	15	m Ω
		$V_{GS} = 4.5V, I_D = 8A$	-	17	20	
Dynamic characteristics						
Input Capacitance	C_{iss}	$V_{DS} = 20V, V_{GS} = 0V, f = 1MHz$	-	1250	-	pF
Output Capacitance	C_{oss}		-	114	-	
Reverse Transfer Capacitance	C_{rss}		-	85	-	
Switching characteristics						
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 20V, I_D = 1A, R_L = 6\Omega$ $V_{GS} = 10V, R_G = 1\Omega$	-	10	-	ns
Turn-on rise time	t_r		-	9	-	
Turn-off delay time	$t_{d(off)}$		-	32	-	
Turn-off fall time	t_f		-	16	-	
Total Gate Charge	Q_g	$V_{DS} = 20V, I_D = 10A,$ $V_{GS} = 10V$	-	20	-	nC
Gate-Source Charge	Q_{gs}		-	3.5	-	
Gate-Drain Charge	Q_{gd}		-	4.2	-	
Source-Drain Diode characteristics						
Diode Forward voltage ⁽³⁾	V_{DS}	$V_{GS} = 0V, I_S = 10A$	-	-	1.2	V
Diode Forward current ⁽⁴⁾	I_S		-	-	20	A

Notes:

1. Repetitive Rating: pulse width limited by maximum junction temperature
2. EAS Condition: $T_J = 25^{\circ}\text{C}, V_{DD} = 20V, R_G = 25\Omega, L = 0.5\text{mH}$
3. Pulse Test: pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
4. Surface Mounted on FR4 Board, $t \leq 10\text{ sec}$

Test Circuit

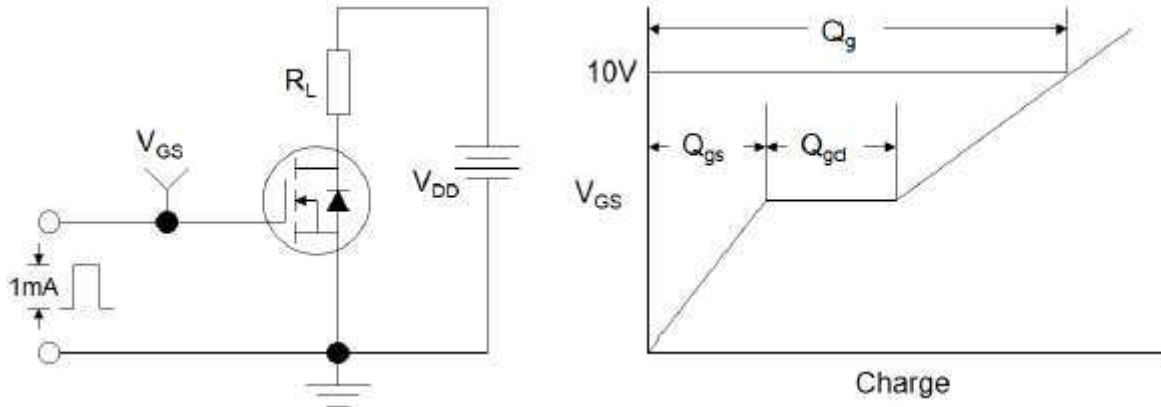


Figure 1: Gate Charge Test Circuit & Waveform

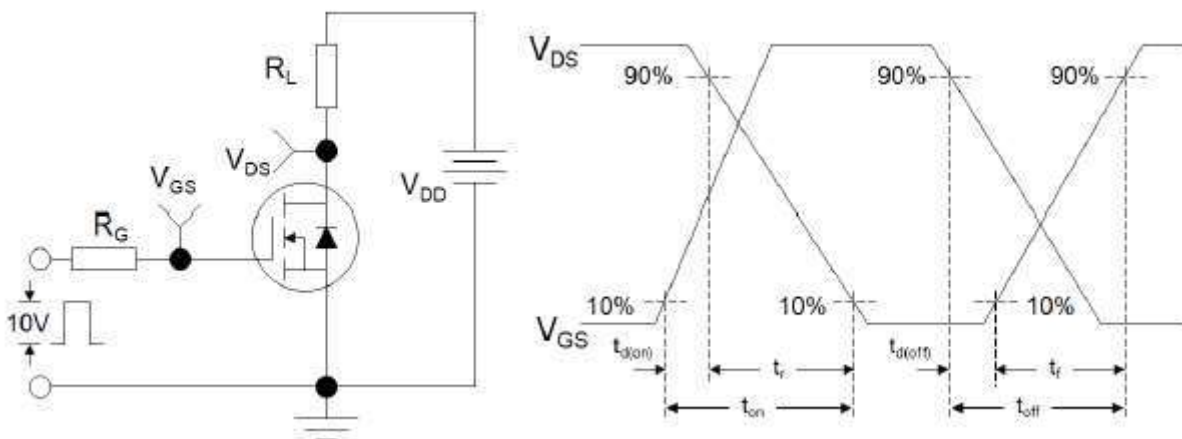


Figure 2: Resistive Switching Test Circuit & Waveforms

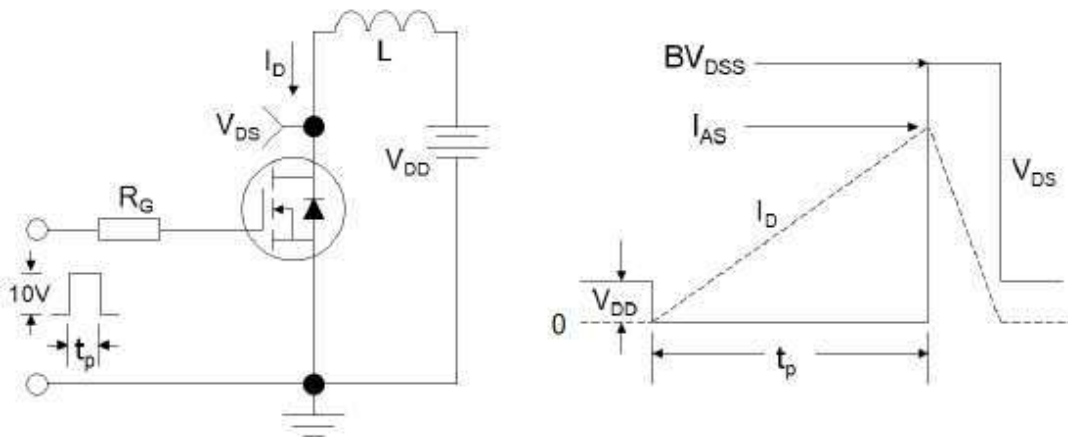


Figure 3: Unclamped Inductive Switching Test Circuit & Waveforms

Typical Performance Characteristics

Figure 1: Output Characteristics

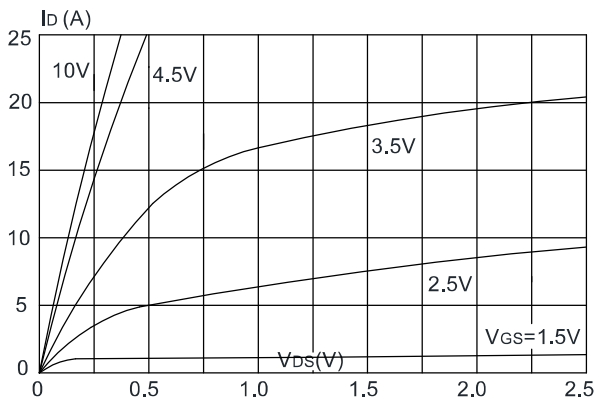


Figure 2: Typical Transfer Characteristics

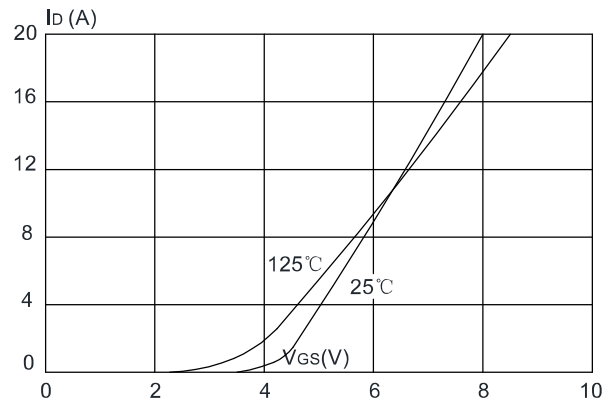


Figure 3: On-resistance vs. Drain Current

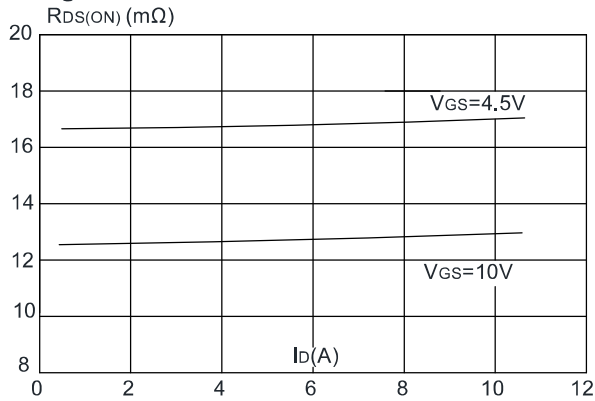


Figure 4: Body Diode Characteristics

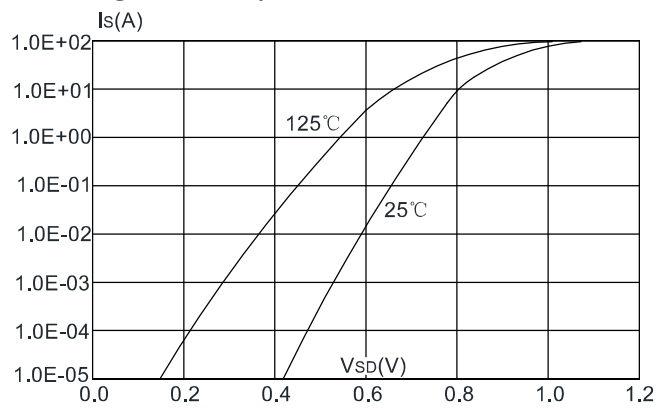


Figure 5: Gate Charge Characteristics

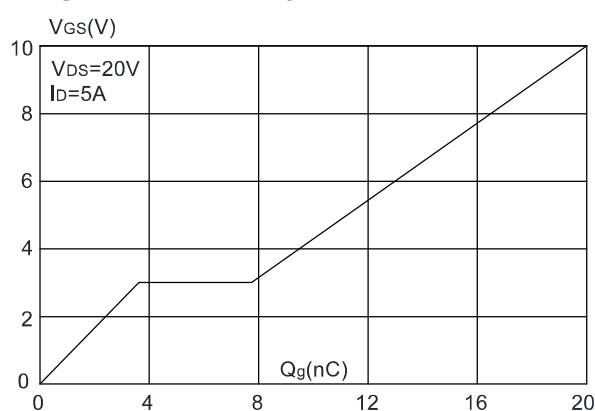


Figure 6: Capacitance Characteristics

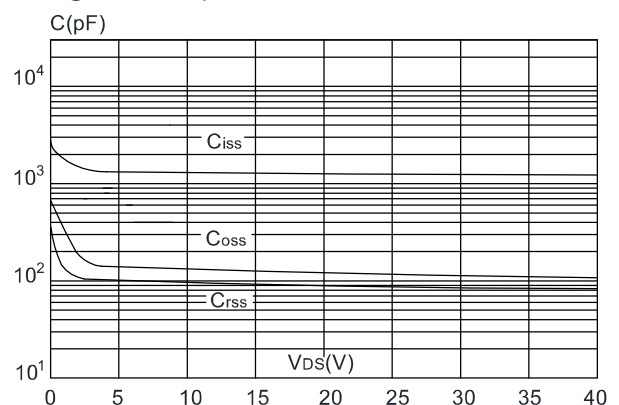


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

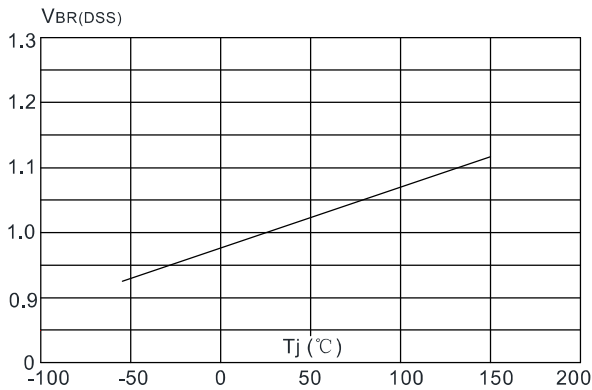


Figure 8: Normalized on Resistance vs. Junction Temperature

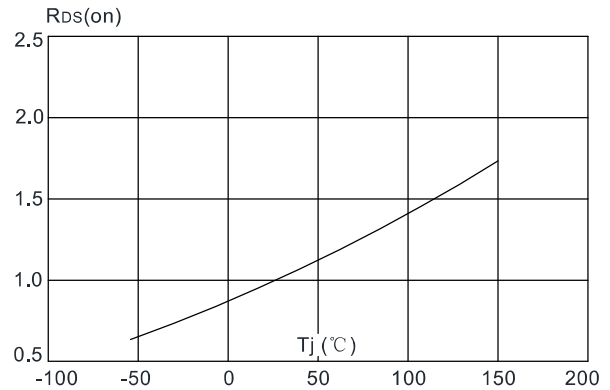


Figure 9: Maximum Safe Operating Area

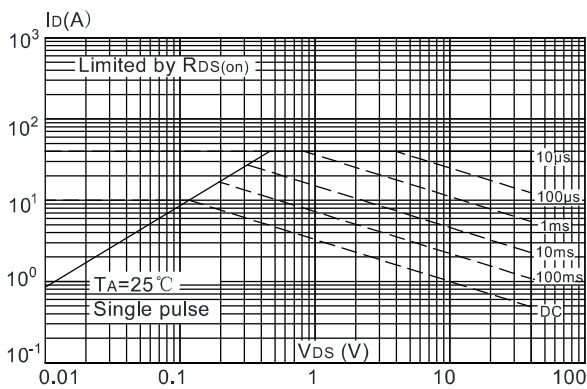


Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature

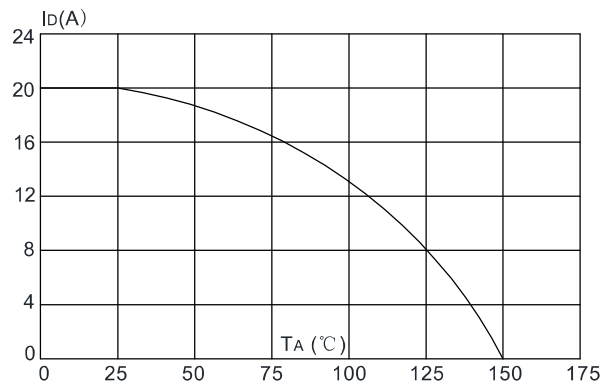
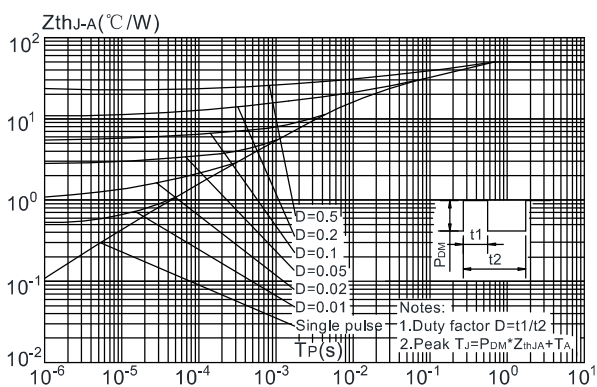
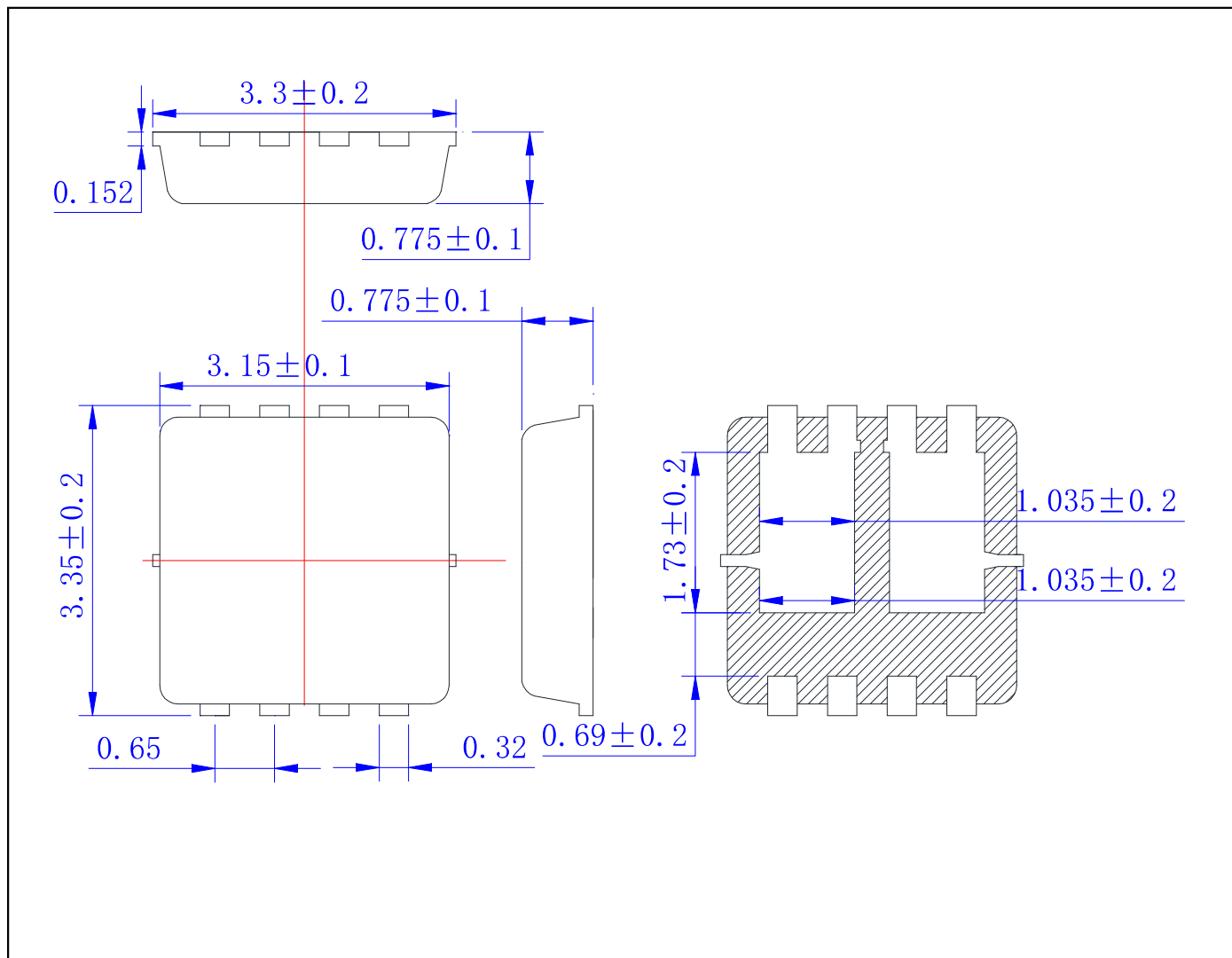


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Ambient



PDFN3X3 Package Information



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[PJMF600N65E1_T0_00201](#) [PJMF900N65E1_T0_00201](#) [PJMF900N60E1_T0_00201](#)