N-Channel Enhancement Mode Power MOSFET

Description

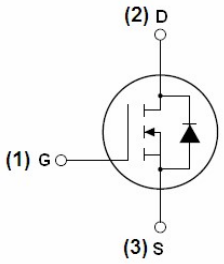
The AP75N04K uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

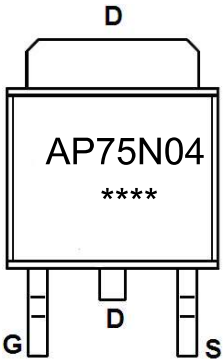
- V_{DS} =40V,I_D =75A
  $R_{DS(ON)}$ <7mΩ @ V_{GS}=10V (Typ:5.8mΩ)
  $R_{DS(ON)}$ <12mΩ @ V_{GS}=4.5V (Typ:9.0mΩ)
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

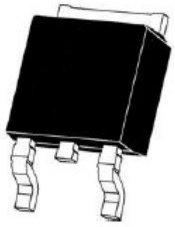
- Power switching application
- Uninterruptible power supply



Schematic diagram



Marking and pin assignment



TO-252-2L top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
AP75N04	AP75N04K	TO-252-2L	-	-	-

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	75	A
Drain Current-Continuous(T_C=100℃)	I_D (100℃)	38	A
Pulsed Drain Current	I_{DM}	160	A
Maximum Power Dissipation	P_D	60	W
Debating factor		0.57	W/℃
Single pulse avalanche energy (Note 5)	E_{AS}	50	mJ
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 175	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Case (Note 2)	$R_{\theta JC}$	1.76	℃/W

Electrical Characteristics (T_C=25℃unless otherwise noted)

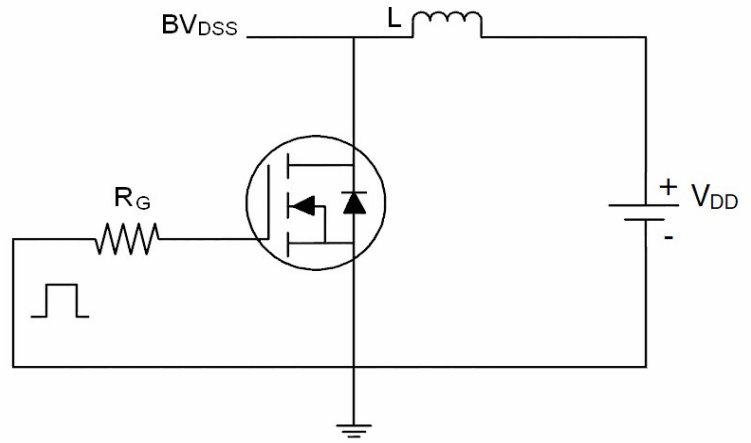
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	40	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=40V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	1	1.6	2.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=30A	-	5.8	7.0	mΩ
			-	9.0	12	mΩ
Forward Transconductance	g_{FS}	V_{DS}=5V,I_D=20A	30	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{lss}	V_{DS}=25V,V_{GS}=0V, F=1.0MHz	-	1540	-	PF
Output Capacitance	C_{oss}		-	171	-	PF
Reverse Transfer Capacitance	C_{rss}		-	115	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=20V,I_D=20A,R_L=1Ω V_{GS}=10V,R_{GEN}=3Ω	-	5.0	-	nS
Turn-on Rise Time	t_r		-	24	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	38	-	nS
Turn-Off Fall Time	t_f		-	12	-	nS
Total Gate Charge	Q_g	V_{DS}=30V,I_D=30A, V_{GS}=10V	-	24	-	nC
Gate-Source Charge	Q_{gs}		-	5.9	-	nC
Gate-Drain Charge	Q_{gd}		-	3.6	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=30A	-	-	1.2	V
Diode Forward Current (Note 2)	I_S		-	-	48	A
Reverse Recovery Time	t_{rr}	TJ = 25°C, IF =30A di/dt = 100A/μs (Note3)	-	9		nS
Reverse Recovery Charge	Qrr		-	15		nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

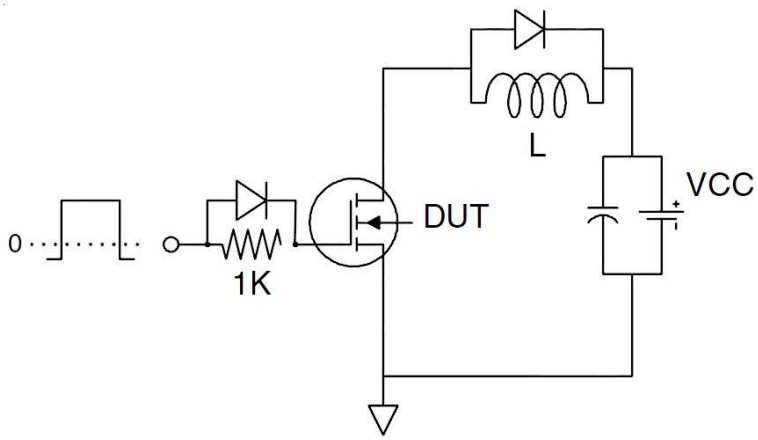
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. E_{AS} condition: Tj=25℃,V_{DD}=30V,V_G=10V,L=0.5mH,Rg=25Ω

Test circuit

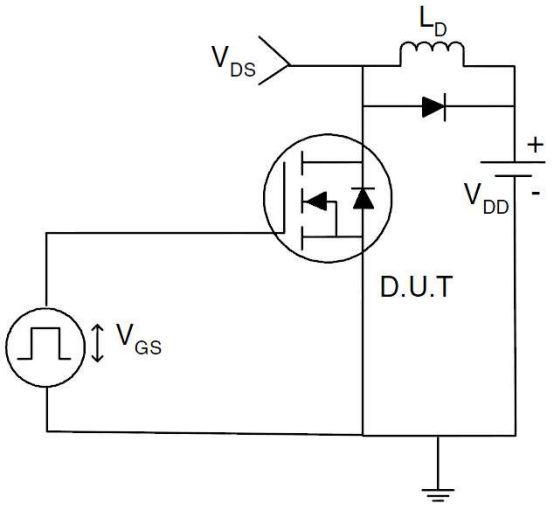
1) E_{AS} test Circuits



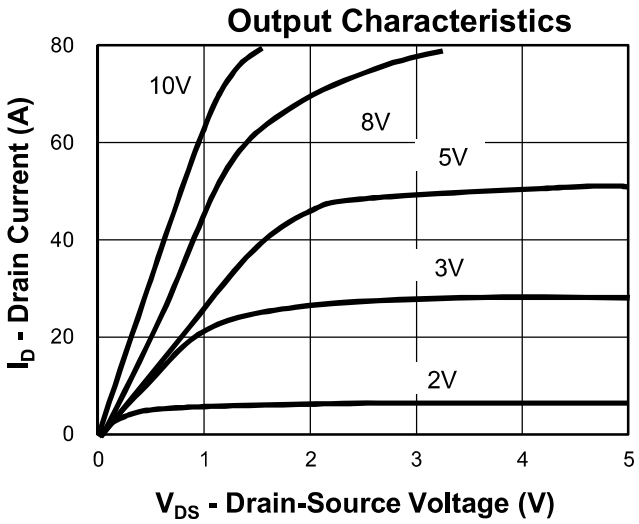
2) Gate charge test Circuit

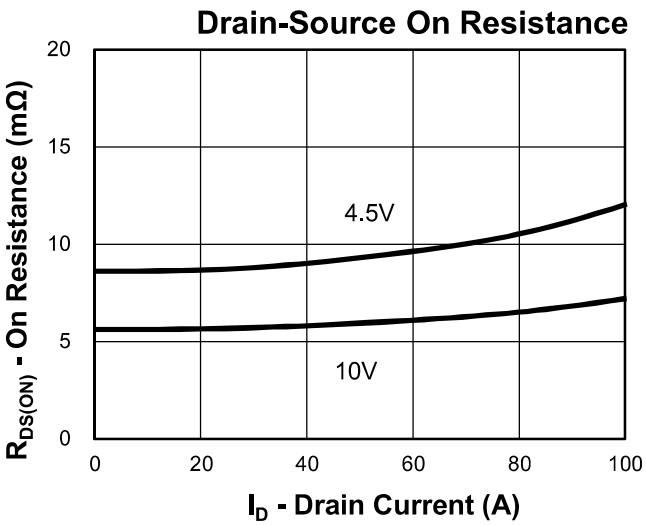


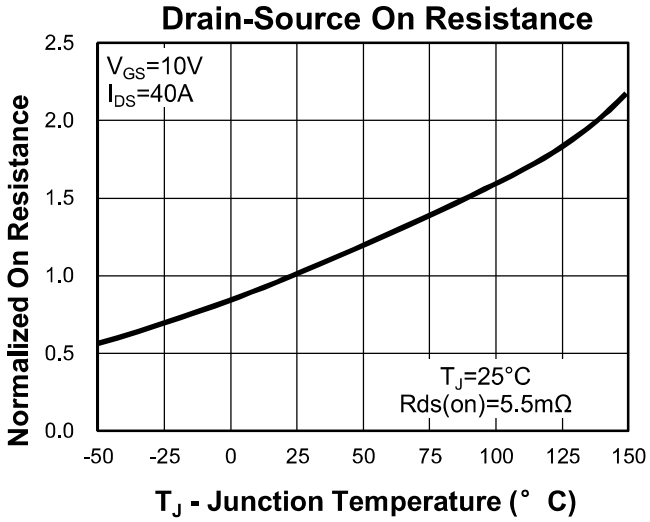
3) Switch Time Test Circuit

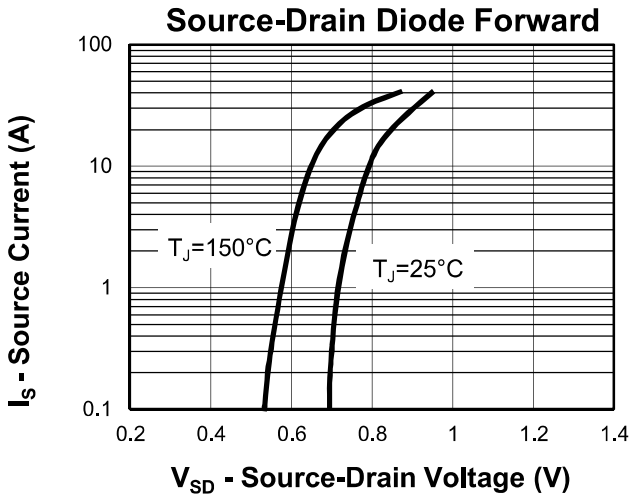


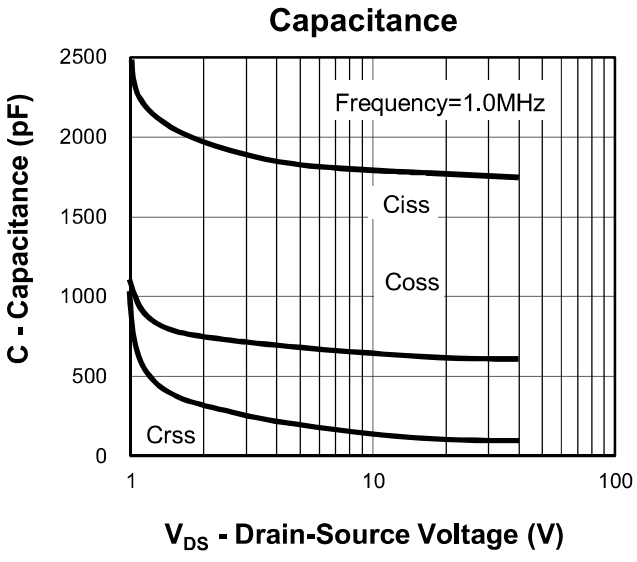
Typical Characteristics

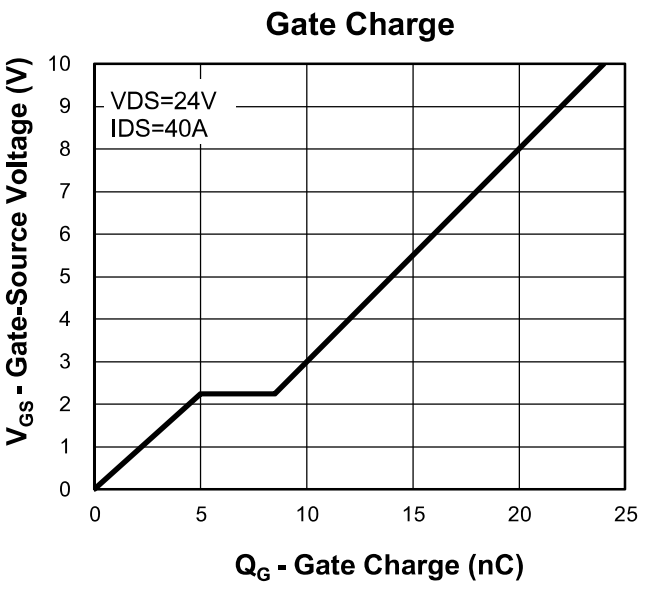












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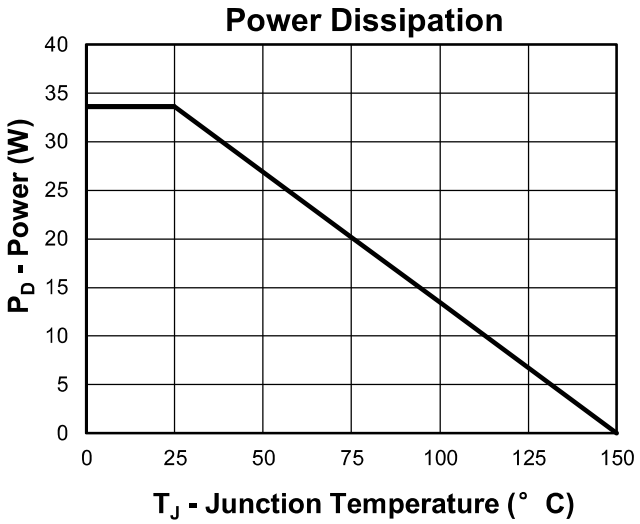
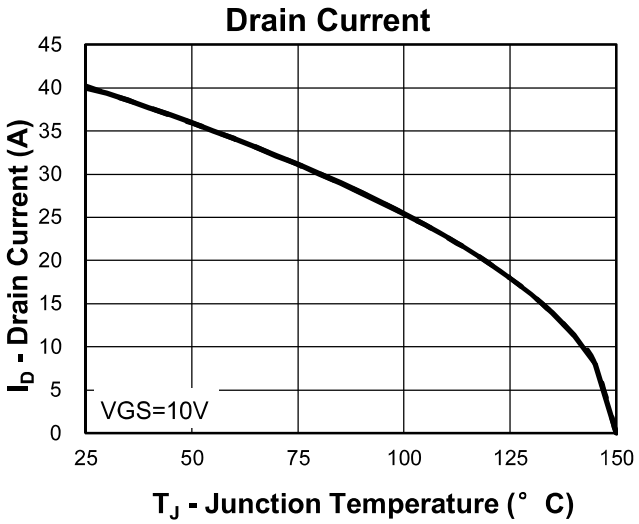
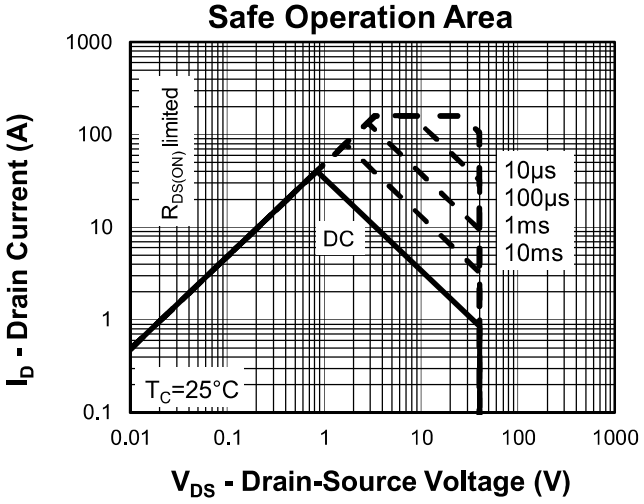
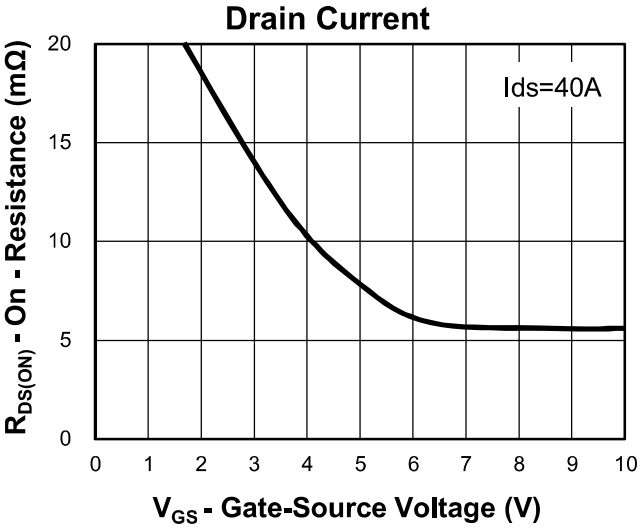
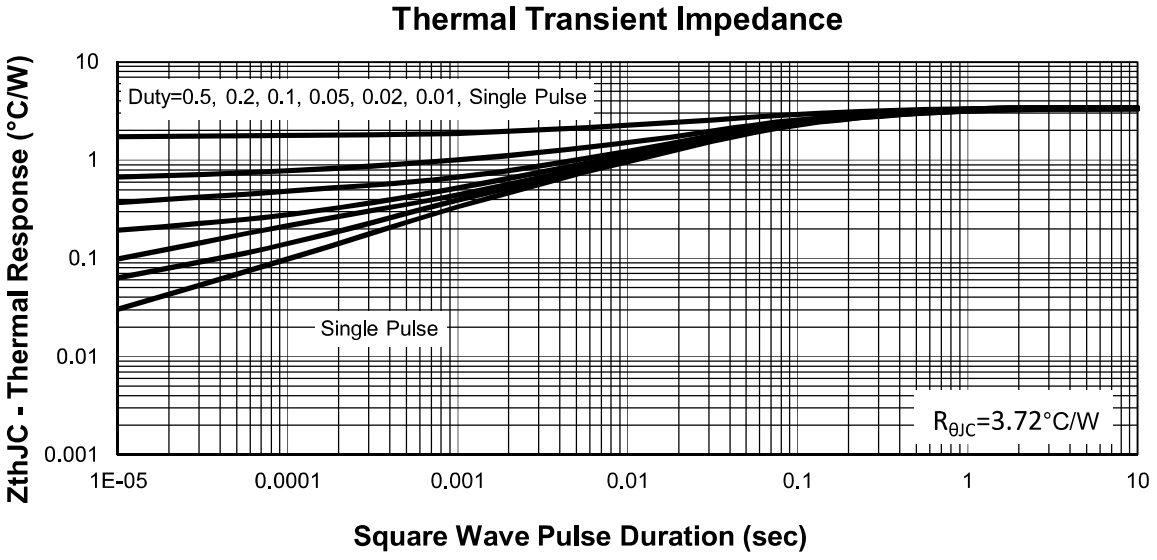


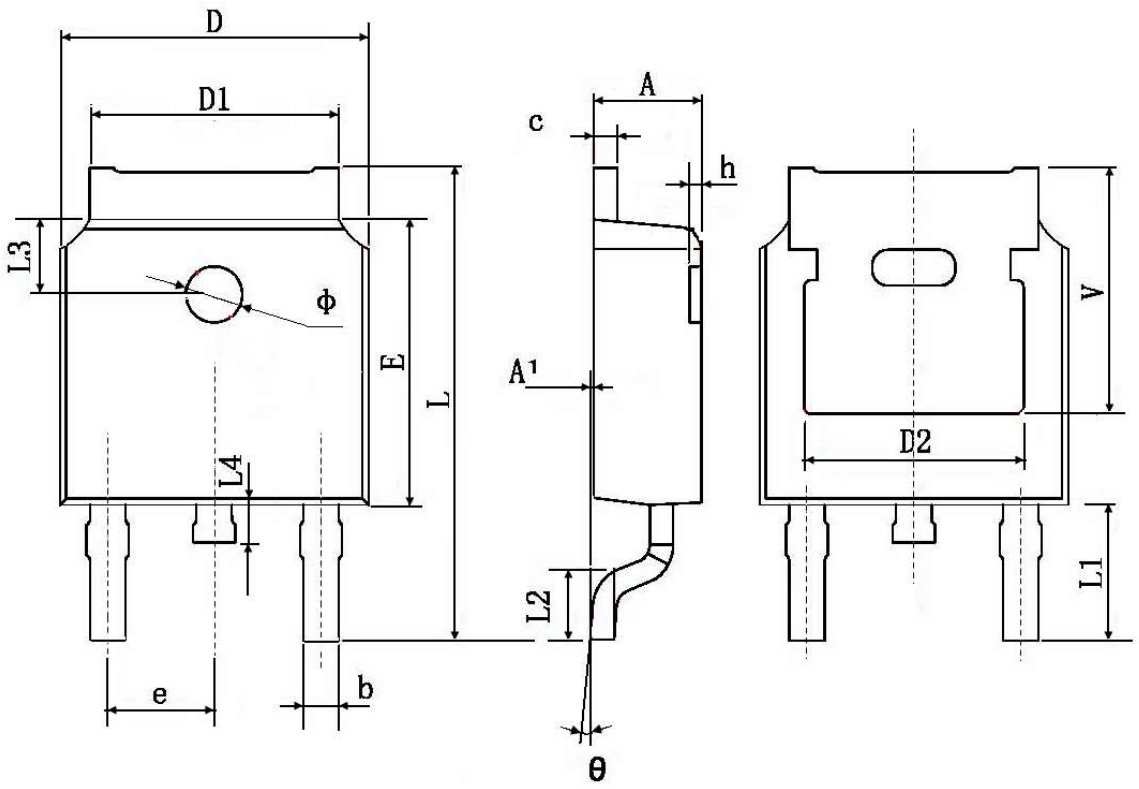








TO-252 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.830 TYP.		0.190 TYP.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 TYP.		0.114 TYP.	
L2	1.400	1.700	0.055	0.067
L3	1.600 TYP.		0.063 TYP.	
L4	0.600	1.000	0.024	0.039
Φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 TYP.		0.211 TYP.	

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