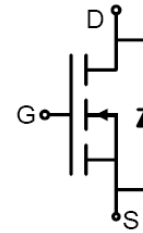


Feature

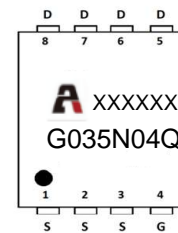
- 40V,100A
 $R_{DS(ON)} < 3.2m\Omega @ V_{GS}=10V$ (TYP:2.8m Ω)
 $R_{DS(ON)} < 5.2m\Omega @ V_{GS}=4.5V$ (TYP:4.3m Ω)
- Split Gate Trench Technology
- Lead free product is acquired
- Excellent $R_{DS(ON)}$ and Low Gate Charge



Schematic Diagram

Application

- PWM applications
- Load Switch
- Power management



Marking and pin Assignment

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity (PCS)
G035N04	APG035N04Q	PDFN3*3-8L	13 inch	-	5000

ABSOLUTE MAXIMUM RATINGS (T_a=25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V _{DS}	40	V
Gate-Source Voltage	V _{GS}	±20	V
Continuous Drain Current (T _a =25°C)	I _D	100	A
Continuous Drain Current (T _a =100°C)	I _D	56	A
Pulsed Drain Current ⁽¹⁾	I _{DM}	376	A
Singel Pulsed Avalanche Energy ⁽²⁾	E _{AS}	100	mJ
Power Dissipation	P _D	51.6	W
Thermal Resistance from Junction to Case	R _{θJC}	2.42	°C/W
Junction Temperature	T _J	150	°C
Storage Temperature	T _{STG}	-55~ +150	°C

MOSFET ELECTRICAL CHARACTERISTICS($T_a=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Type	Max	Unit
Static Characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	40	-	-	V
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 40V, V_{GS} = 0V$	-	-	1	μA
Gate-body leakage current	I_{GSS}	$V_{GS} = \pm 20V, V_{DS} = 0V$	-	-	± 100	nA
Gate threshold voltage ⁽³⁾	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	1.2	1.7	2.2	V
Drain-source on-resistance ⁽³⁾	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 30A$	-	2.8	3.5	m Ω
		$V_{GS} = 4.5V, I_D = 20A$	-	4.3	5.2	
Gate Resistance	R_g	$V_{DS} = V_{GS} = 0V, f = 1MHz$	-	3.2	-	Ω
Dynamic characteristics						
Input Capacitance	C_{iss}	$V_{DS} = 20V, V_{GS} = 0V, f = 1MHz$	-	1280	-	pF
Output Capacitance	C_{oss}		-	462	-	
Reverse Transfer Capacitance	C_{rss}		-	22	-	
Switching characteristics						
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 20V, I_D = 25A,$ $V_{GS} = 10V, R_G = 4.7\Omega$	-	4	-	ns
Turn-on rise time	t_r		-	25.5	-	
Turn-off delay time	$t_{d(off)}$		-	20.5	-	
Turn-off fall time	t_f		-	9.2	-	
Total Gate Charge	Q_g	$V_{DS} = 20V, I_D = 25A,$ $V_{GS} = 10V$	-	20.3	-	nC
Gate-Source Charge	Q_{gs}		-	4.1	-	
Gate-Drain Charge	Q_{gd}		-	3.5	-	
Reverse Recovery Chrage	Q_{rr}	$I_F = 50A, di/dt = 100A/us$	-	13	-	nC
Reverse Recovery Time	T_{rr}	$I_F = 50A, di/dt = 100A/us$	-	22.1	-	ns
Source-Drain Diode characteristics						
Diode Forward voltage ⁽³⁾	V_{SD}	$V_{GS} = 0V, I_S = 50A$	-	-	1.2	V
Diode Forward current ⁽⁴⁾	I_S		-	-	100	A

Notes:

1. Repetitive Rating: pulse width limited by maximum junction temperature
2. EAS Condition: $T_J = 25^{\circ}\text{C}, V_{DD} = 20V, R_G = 25\Omega, L = 0.5Mh, I_{AS} = 20A$
3. Pulse Test: pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
4. Surface Mounted on FR4 Board, $t \leq 10$ sec

■ Test circuits and waveforms

Figure A: Gate Charge Test Circuit & Waveforms

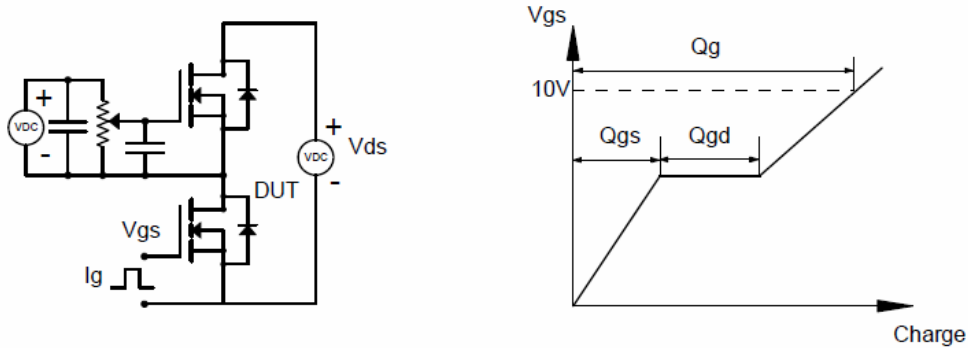


Figure B: Resistive Switching Test Circuit & Waveforms

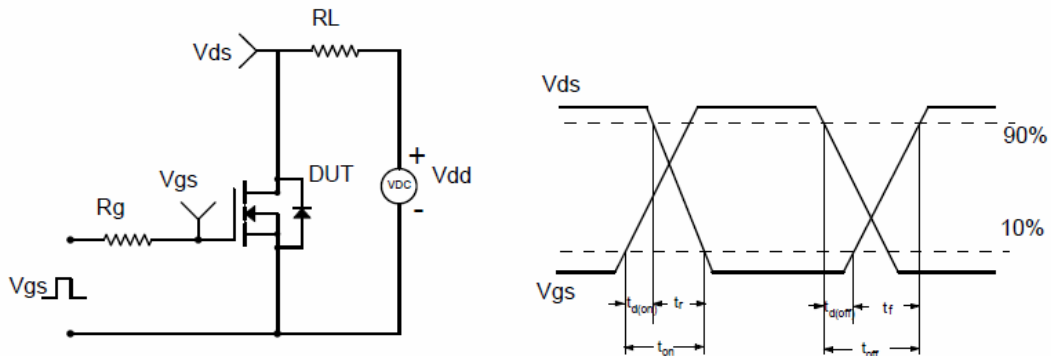


Figure C: Unclamped Inductive Switching (UIS) Test

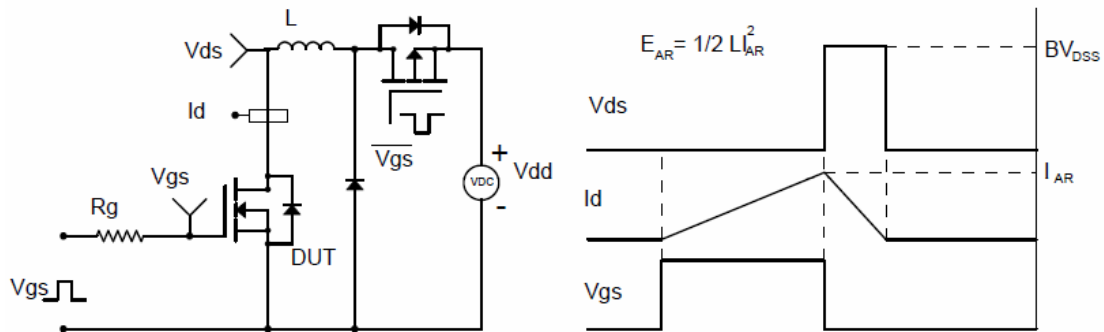
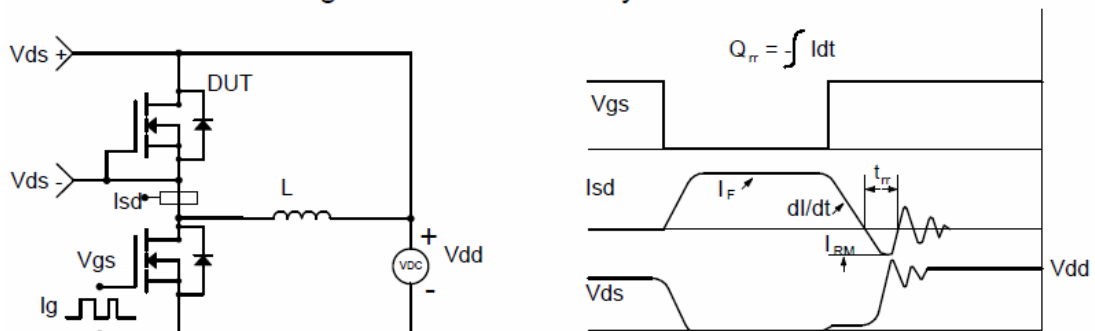
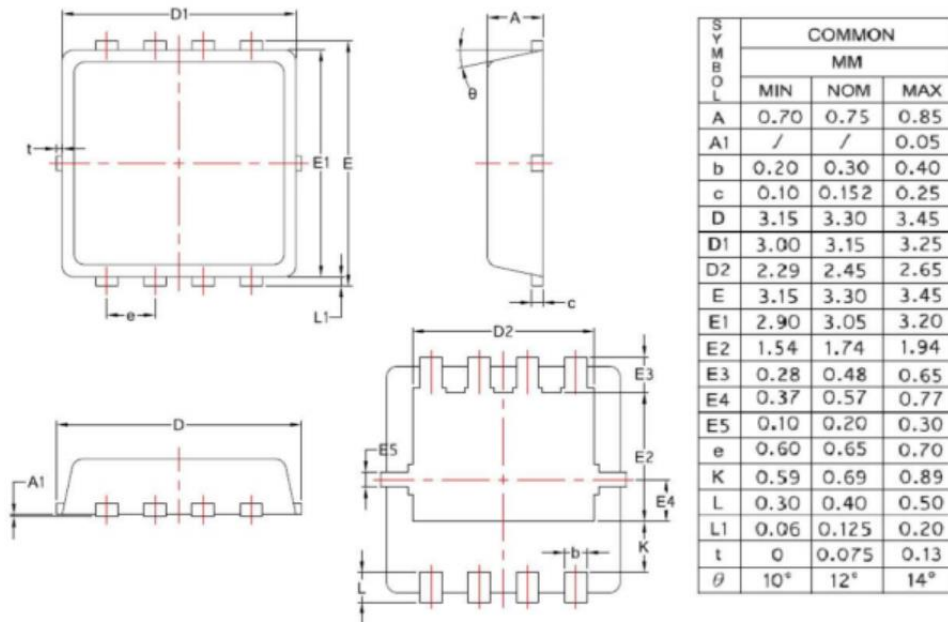


Figure D: Diode Recovery Test Circuit & Waveforms



PDFN3X3-8L Package Information



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