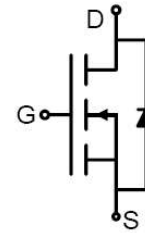


Feature

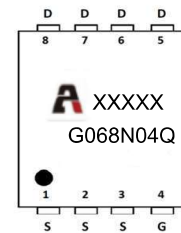
- 40V,54A
 $R_{DS(ON)} < 6.8m\Omega @ V_{GS}=10V$ (TYP:5.7m Ω)
 $R_{DS(ON)} < 11m\Omega @ V_{GS}=4.5V$ (TYP:8.5m Ω)
- Split Gate Trench Technology
- Lead free product is acquired
- Excellent $R_{DS(ON)}$ and Low Gate Charge



Schematic Diagram

Application

- PWM applications
- Load Switch
- Power management



Marking and pin Assignment

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity (PCS)
G068N04Q	APG068N04Q	PDFN3*3-8L	13 inch	-	5000

ABSOLUTE MAXIMUM RATINGS ($T_a=25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ($T_a=25^{\circ}C$)	I_D	54	A
Continuous Drain Current ($T_a=100^{\circ}C$)	I_D	34	A
Pulsed Drain Current ⁽¹⁾	I_{DM}	216	A
Singel Pulsed Avalanche Energy ⁽²⁾	E_{AS}	56	mJ
Power Dissipation	P_D	36.7	W
Thermal Resistance from Junction to Case	$R_{\theta JC}$	3.4	$^{\circ}C/W$
Junction Temperature	T_J	150	$^{\circ}C$
Storage Temperature	T_{STG}	-55~ +150	$^{\circ}C$

MOSFET ELECTRICAL CHARACTERISTICS(T_a=25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Type	Max	Unit
Static Characteristics						
Drain-source breakdown voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D =250μA	40	-	-	V
Zero gate voltage drain current	I _{DSS}	V _{DS} =40V, V _{GS} = 0V	-	-	1	μA
Gate-body leakage current	I _{GSS}	V _{GS} =±20V, V _{DS} = 0V	-	-	±100	nA
Gate threshold voltage ⁽³⁾	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1.0	1.6	2.0	V
Drain-source on-resistance ⁽³⁾	R _{DS(on)}	V _{GS} =10V, I _D =20A	-	5.7	6.8	mΩ
		V _{GS} =4.5V, I _D =15A	-	8.5	11	
Gate Resistance	R _g	V _{DS} =V _{GS} =0V, f =1MHz	-	3.6	-	Ω
Dynamic characteristics						
Input Capacitance	C _{iss}	V _{DS} =20V, V _{GS} =0V, f =1MHz	-	840	-	pF
Output Capacitance	C _{oss}		-	254	-	
Reverse Transfer Capacitance	C _{rss}		-	5	-	
Switching characteristics						
Turn-on delay time	t _{d(on)}	V _{DD} =20V, I _D =20A, V _{GS} =10V, R _G =10Ω	-	4	-	ns
Turn-on rise time	t _r		-	11	-	
Turn-off delay time	t _{d(off)}		-	25	-	
Turn-off fall time	t _f		-	23	-	
Total Gate Charge	Q _g	V _{DS} =20V, I _D =20A, V _{GS} =4.5V	-	13.1	-	nC
Gate-Source Charge	Q _{gs}		-	2.2	-	
Gate-Drain Charge	Q _{gd}		-	2.6	-	
Reverse Recovery Chrage	Q _{rr}	I _F =40A, di/dt=100A/us		5.8		nC
Reverse Recovery Time	T _{rr}	I _F =40A, di/dt=100A/us		18		ns
Source-Drain Diode characteristics						
Diode Forward voltage ⁽³⁾	V _{DS}	V _{GS} =0V, I _S =50A	-	-	1.2	V
Diode Forward current ⁽⁴⁾	I _S		-	-	54	A

Notes:

1. Repetitive Rating: pulse width limited by maximum junction temperature
2. EAS Condition: T_J=25°C, V_{DD}=20V, R_G=25 Ω, L=0.5mH
3. Pulse Test: pulse width≤300μs, duty cycle≤2%
4. Surface Mounted on FR4 Board, t≤10 sec

Test Circuit

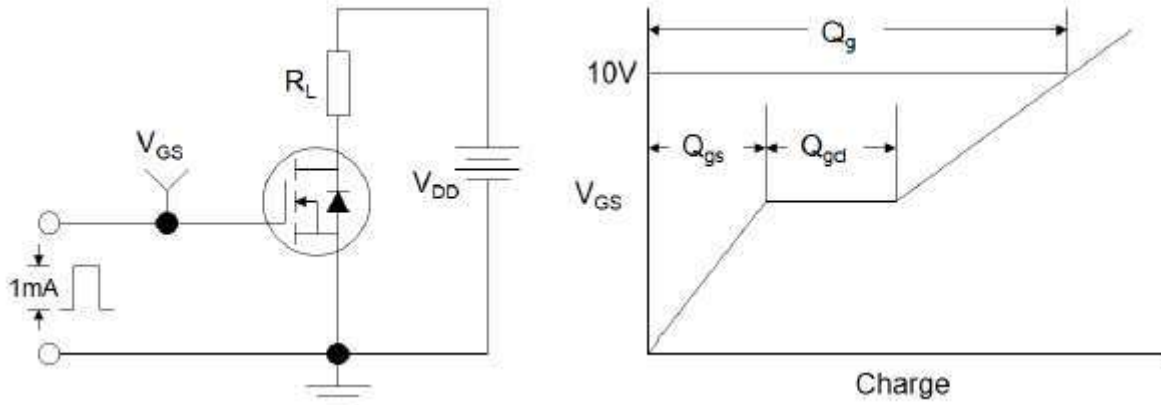


Figure1:Gate Charge Test Circuit & Waveform

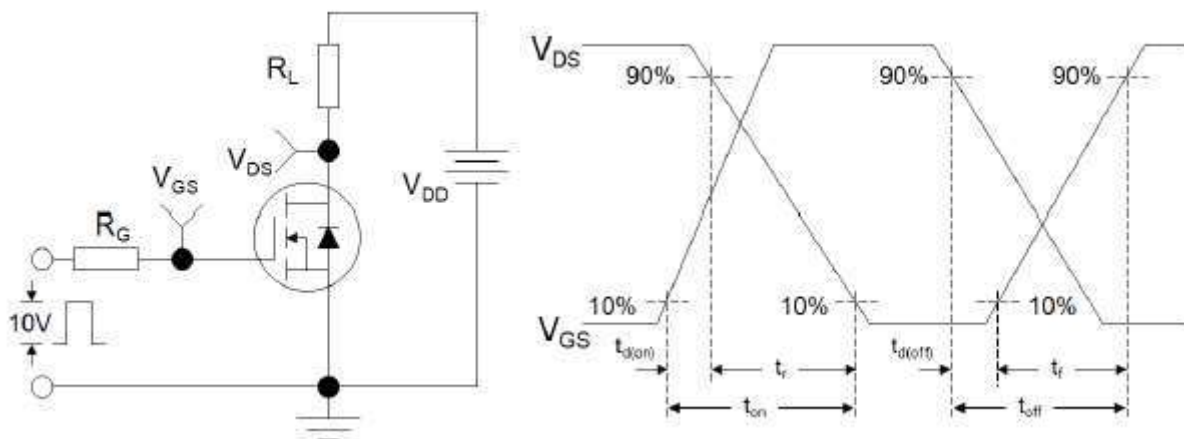


Figure 2: Resistive Switching Test Circuit & Waveforms

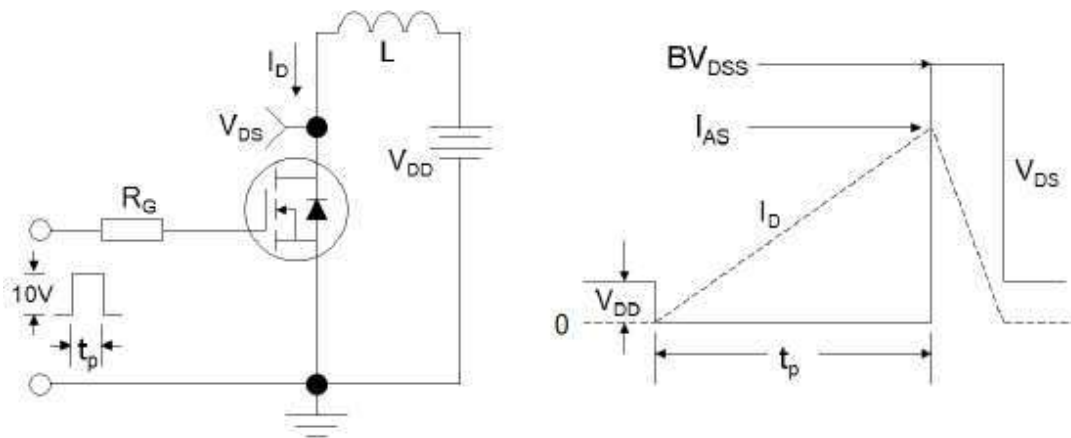
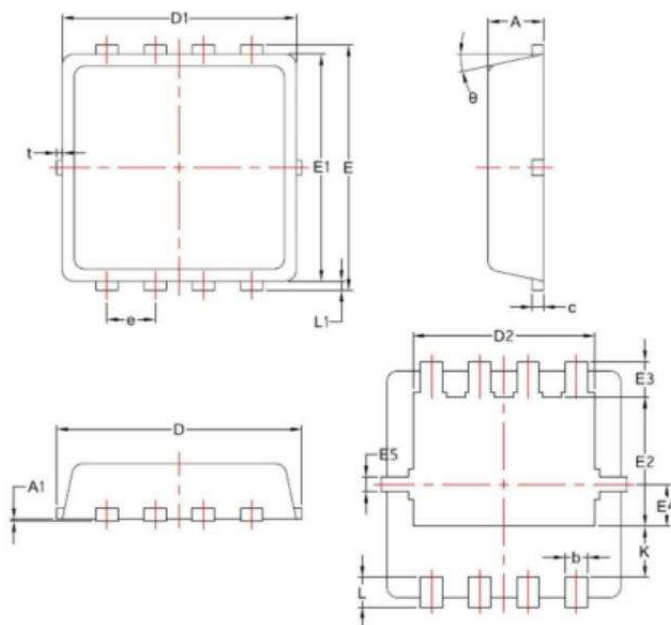


Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms

PDFN3X3-8L Package Information



SYMBOL	COMMON		
	MM		
	MIN	NOM	MAX
A	0.70	0.75	0.85
A1	/	/	0.05
b	0.20	0.30	0.40
c	0.10	0.152	0.25
D	3.15	3.30	3.45
D1	3.00	3.15	3.25
D2	2.29	2.45	2.65
E	3.15	3.30	3.45
E1	2.90	3.05	3.20
E2	1.54	1.74	1.94
E3	0.28	0.48	0.65
E4	0.37	0.57	0.77
E5	0.10	0.20	0.30
e	0.60	0.65	0.70
K	0.59	0.69	0.89
L	0.30	0.40	0.50
L1	0.06	0.125	0.20
t	0	0.075	0.13
θ	10°	12°	14°

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[IRF40H233XTMA1](#) [STU5N65M6](#) [DMN6022SSD-13](#) [DMN13M9UCA6-7](#) [DMTH10H4M6SPS-13](#) [IPS60R360PFD7SAKMA1](#)
[DMN2990UFB-7B](#) [SSM3K35CT,L3F](#) [IPLK60R1K0PFD7ATMA1](#) [2N7002W-G](#) [MCAC30N06Y-TP](#) [IPWS65R035CFD7AXKSA1](#)
[MCQ7328-TP](#) [SSM3J143TU,LXHF](#) [DMN12M3UCA6-7](#) [PJMF280N65E1_T0_00201](#) [PJMF380N65E1_T0_00201](#)
[PJMF280N60E1_T0_00201](#) [PJMF600N65E1_T0_00201](#) [PJMF900N65E1_T0_00201](#) [PJMF900N60E1_T0_00201](#)