QuickLogic® PolarPro® 3 Device Data Sheet

Ultra-Low Power FPGA Combining Efficient Logic Cells with Embedded RAM and FIFO Blocks to Maximize Logic Density in Minimal PCB Space

Device Highlights

Ultra Low Power

- 55 µA static power consumption, suitable for smartphones, tablets, mobile enterprise devices and other power sensitive applications
- Prolongs device battery life

Small Form Factor Packaging

- 640 and 1,019 logic cell packages as small as 2.09 mm x 2.54 mm
- WLCSP, VFBGA, or die options available
- Designed for the most space-sensitive applications

Complete Customizable Solutions

- Allows offloading of computationally intensive applications
- Includes comprehensive software packages along with hardware

Efficient Logic Utilization

- Flexible logic cells, capable of two independent 3-input LUTs or a single 4-input LUT.
- Allows greater functionality in less PCB space

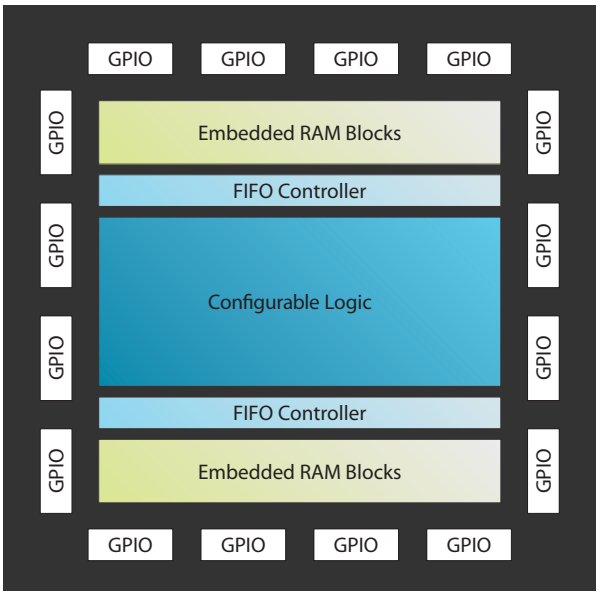
Embedded Standard Blocks

- Built in SRAM and FIFO controllers
- Enables data buffering and autonomous data transfers

Fast Time-to-Market

- QuickLogic designs and delivers complete Customer Specific Standard Product (CSSP) solutions, including hardware and software
- Uses QuickLogic's existing library of Proven System Blocks (PSBs)
- Reduces development time and costs

Figure 1: PolarPro 3 Block Diagram



Flexible Reconfigurable Logic

- 1.2 V core voltage, 1.8/2.5/3.3 V drive capable I/Os
- Up to 64 kilobits of SRAM
- 55 µA standby current
- Up to 46 I/Os available
- 640 and 1,019 logic cell options
- Reconfigurable SRAM technology

Embedded Dual-Port SRAM

- Up to eight dual-port 8-kilobit high performance SRAM blocks
- True dual-port capability
- Embedded synchronous/asynchronous FIFO controllers
- Configurable and cascadable aspect ratio

Configurable I/O

- Configurable dual drive strength per GPIO
- Independent I/O banks capable of supporting multiple I/O standards in one device
- Bank programmable I/O standards: LVTTL, LVCMOS25 and LVCMOS18
- Week pulldown capability and input enables

Advanced Clock Network

- Multiple low skew clock networks
  - 5 programmable global clock networks
- Quadrant-based segmentable clock networks
  - 20 quad clock networks per device

Introduction

PolarPro 3 was specifically architected to meet the increasingly complex needs of mobile device OEMs. With special attention paid to efficient logic cell utilization, smallest size, and lowest power consumption during the design process, PolarPro 3 is the ideal solution for OEMs who require a configurable logic solution for their application. PolarPro 3 operates seamlessly with any processor available on the market today to address emerging connectivity, sensor control, and custom applications. QuickLogic combines PSBs and software drivers, along with customer-specific logic, to deliver CSSPs based on the exact requirements of our customers.

Table 1 summarizes the PolarPro 3 device family features.

Table 1: PolarPro 3 Device Family

Features		1,019 Logic Cells	640 Logic Cells
Max Gates		175,000	90,000
Logic Cells		1019	640
8K RAM Modules (9216 bits)		8	4
FIFO Controllers		8	4
RAM bits		73,728	36,864
Max I/O per Package	30-ball WLCSP (0.4 mm pitch)	18	18
	64-ball VFBGA (0.4 mm pitch)	46	46

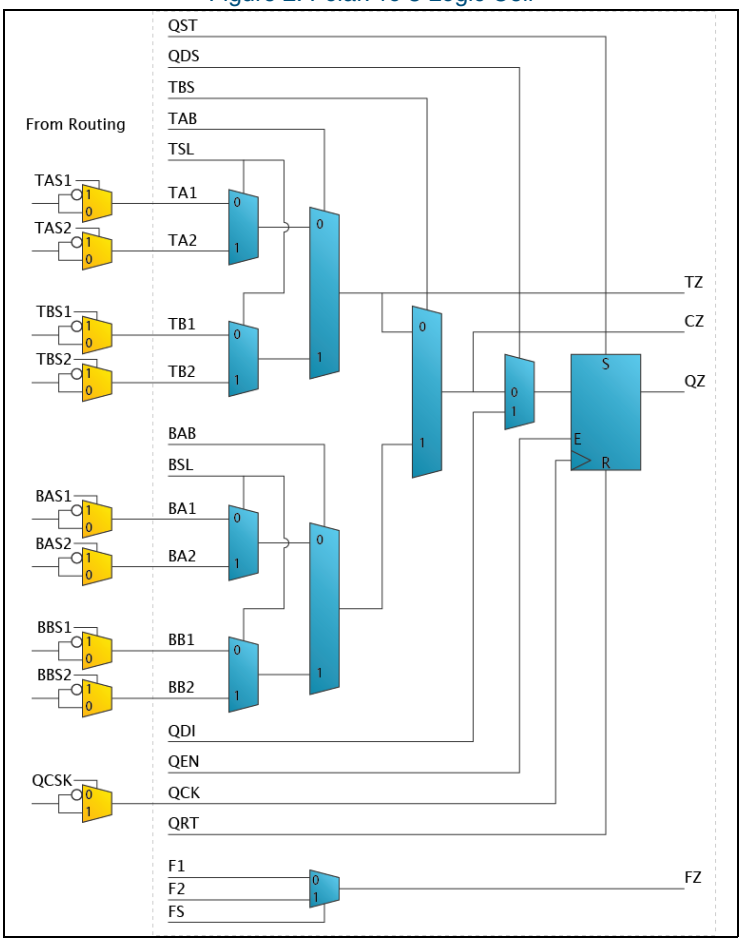
Programmable Logic Architectural Overview

The QuickLogic PolarPro 3 logic cell structure presented in **Figure 2** is a single register, multiplexer-based logic cell. It is designed for wide fan-in and multiple, simultaneous output functions. The cell has a high fan-in, fits a wide range of functions with up to 22 simultaneous inputs (including register control lines), and four outputs (three combinatorial and one registered). The high logic capacity and fan-in of the logic cell accommodates many user functions with a single level of logic delay.

The PolarPro 3 logic cell can implement:

- Two independent 3-input functions
- Any 4-input function
- 8 to 1 mux function
- Independent 2 to 1 mux function
- Inverted or non-inverted clock signal to flip-flop
- Single dedicated register with active high clock enable, set and reset signals
- Direct input selection to the register, which allows combinatorial and register logic to be used separately
- Combinatorial logic can also be configured as an edge-triggered master-slave D flip-flop

Figure 2: PolarPro 3 Logic Cell



RAM Modules

The PolarPro 3 family of devices includes up to eight 8 kilobits (9,216 bits) dual-port RAM modules for implementing RAM and FIFO functions.

RAM features include:

- Independently configurable read and write data bus widths
- Independent read and write clocks
- Inverted or non-inverted clock signals to read and write clock inputs
- Horizontal and vertical concatenation
- Write byte enables
- Selectable pipelined or non-pipelined read data

Figure 3 shows the 8-kilobit Dual-Port RAM block.

Figure 3: 8-Kilobit Dual-Port RAM Block 512 x 18 Configuration

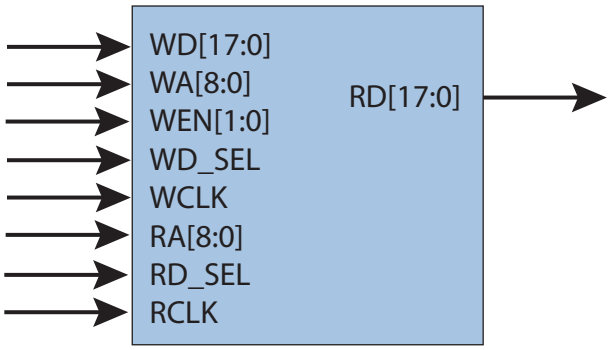


Table 2 describes the RAM interface signals.

Table 2: RAM Interface Signals

Signal Name	Function
Inputs	
WD [17:0]	Write Data
WA [8:0]	Write Address
WEN [1:0]	Write Enable (two 9-bit enables)
WD_SEL	Write Chip Select
WCLK	Write Clock
RA [8:0]	Read Address
RD_SEL	Read Chip Select
RCLK	Read Clock
Output	
RD [17:0]	Read Data Output

The read and write data buses of a RAM block can be arranged to variable bus widths. The bus widths can be configured using the RAM Wizard available in QuickWorks, QuickLogic's development software. The selection of the RAM depth and width determines how the data is addressed.

The RAM blocks also support data concatenation. Designers can cascade multiple RAM modules to increase the depth or width by connecting corresponding address lines together and dividing the words between modules. Generally, this requires the use of additional programmable logic resources. However, when concatenating only two 8-kilobit RAM blocks, they can be concatenated horizontally or vertically without using any additional programmable fabric resources.

For example, two internal dual-port RAM blocks can be concatenated vertically to create a 1024x18 RAM block or horizontally to create a 512x36 RAM block. A block diagram of horizontal and vertical concatenation is displayed in **Figure 4**.

Figure 4: Horizontal and Vertical Concatenation Examples

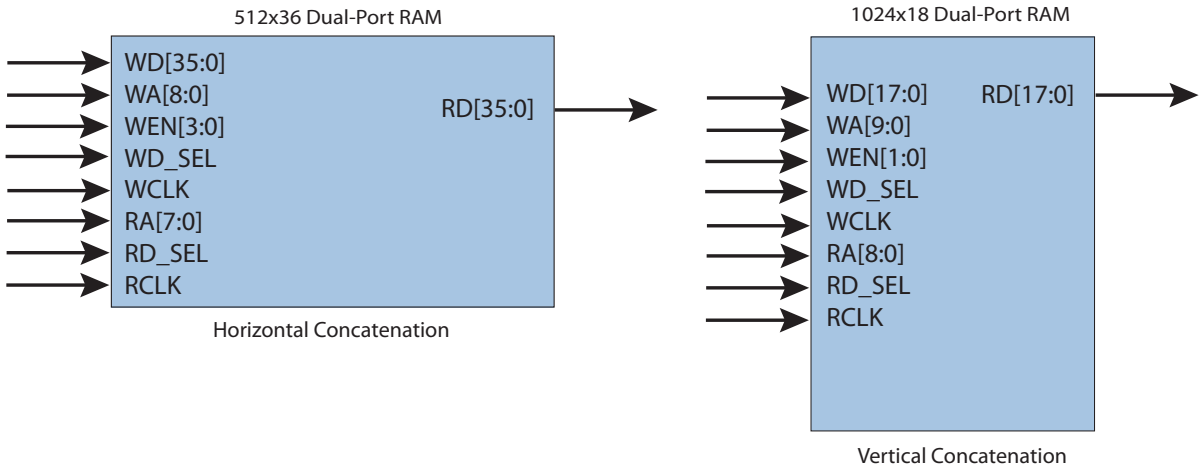


Table 3 shows the various configurations supported by the PolarPro 3 8-kilobit RAM modules.

Table 3: Available Dual-Port Configurations

Number of RAM Blocks	Depth	Supported Widths
1	512	1-18 bits
2	512	1-36 bits
2	1024	1-18 bits
2	2048	1-9 bits

True Dual-Port RAM

PolarPro 3 Dual-Port RAM modules can also be concatenated to generate True Dual-Port RAMs. The True Dual-Port RAM module's Port1 and Port2 have completely independent read and write ports and separate read and write clocks. This allows Port1 and Port2 to have different data widths and clock domains from each other. It is important to note that there is no circuitry preventing a write and read operation to the same address space at the same time. Therefore, the designer must ensure that the same address is not read from and written to simultaneously, otherwise the data is considered invalid. Likewise, the same address should not be written to from both ports at the same time. However, it is possible to read from the same address.

Figure 5 shows an example of a 1024x18 true dual-port RAM.

Figure 5: 1024x18 True Dual-Port RAM Block

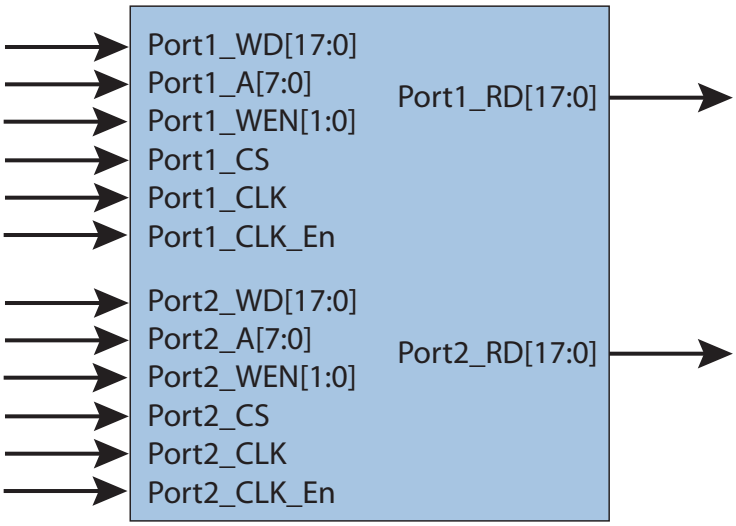


Table 4 describes the true dual-port RAM interface signals.

Table 4: True Dual-Port RAM Interface Signals

Port	Signal Name	Function
Port1	**Inputs**	
	Port1_WD [17:0]	Write Data
	Port1_A [9:0]	Write Address
	Port1_WEN	Write Enable
	Port1_CS	Chip Select
	Port1_CLK	Clock
	Output	
	Port1_RD [17:0]	Read Data
Port2	**Inputs**	
	Port2_WD [17:0]	Write Data
	Port2_A [9:0]	Write Address
	Port2_WEN	Write Enable
	Port2_CS	Chip Select
	Port2_CLK	Clock
	Output	
	Port2_RD [17:0]	Read Data

Table 5 lists the true dual-port configurations that are available.

Table 5: Available True Dual-Port Configurations

Number of RAM Blocks	Depth	Width
2	1024	1-18
2	2048	1-9

Embedded FIFO Controllers

Every 8-kilobit RAM block can be implemented as a synchronous or asynchronous FIFO. There are built-in FIFO controllers that allow for varying depths and widths without requiring programmable fabric resources. During asynchronous operation, the FIFO works in a half-duplex fashion such that PUSH is on one clock domain and POP is on another clock domain. The DIR signal allows the FIFO PUSH and POP signal directions to reverse. Refer to **Table 6** for details on the signal directions. It is important that FIFO pointers are flushed after DIR is switched to reset the FIFO pointers.

The PolarPro 3 FIFO controller features include:

- x9, x18 and x36 data bus widths
- Independent PUSH and POP clocks
- Independent programmable data width on PUSH and POP sides
- Configurable synchronous or asynchronous FIFO operation
- 4-bit PUSH and POP level indicators to provide FIFO status outputs for each port
- Pipelined read data to improve timing
- Option for inverted or non-inverted Async_Flush input

Table 6: FIFO Interface Signals

Signal Name	Width (bits)	Direction	Function
PUSH Signals			
DIN	1 to 36	I	Data bus input.
PUSH	1	I	Initiates a data push.
Fifo_Push_Flush	1	I	Empties the FIFO.
Push_Clk	1	I	Push data clock.
POP Signals			
DOUT	1 to 36	O	Data bus output.
POP	1	I	Initiates a data pop.
Fifo_Pop_Flush	1	I	Empties the FIFO.
Pop_Clk	1	I	Pop data clock.
Status Flags			
Almost_Full	1	O	Asserted when FIFO has one location available.
Almost_Empty	1	O	Asserted when FIFO has one location used.
PUSH_FLAG	4	O	FIFO PUSH level indicator.
POP_FLAG	4	O	FIFO POP level indicator.
Asynchronous Signals			
DIR	1	I	Determines the direction of the PUSH and POP signals: 0 – Signals set as normal. 1 – Reverses the FIFO direction so that the PUSH signals become POP signals and POP signals become PUSH signals.
Async_Flush	1	I	Asynchronous input to flush FIFO. Used to reset FIFO logic asynchronously.

Figure 6 shows an example a FIFO module.

Figure 6: PolarPro 3 FIFO Module

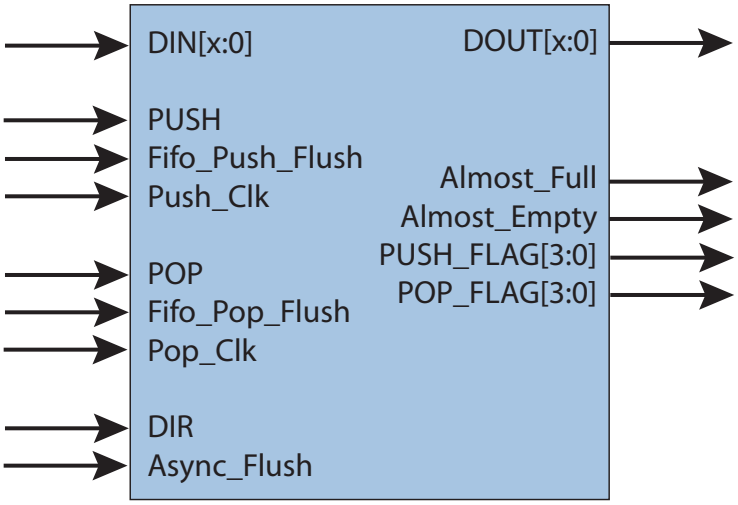


Table 7 lists the FIFO configurations that are available.

Table 7: Available FIFO Configurations

Number of RAM Blocks	Depth	Supported Widths
1	512	1-18 bits
2	512	1-36 bits
2	1024	1-18 bits
2	2048	1-9 bits

Table 8 and **Table 9** highlight the corresponding FIFO level indicator for each 4-bit value of the PUSH_FLAG and POP_FLAG outputs.

Table 8: FIFO PUSH Level Indicator Values

Value	Status
0000	Full
0001	Empty
0010	Room for more than one-half
0011	Room for more than one-forth
0100	Room for less than one-forth full to 64
1010	Room for 32 to 63
1011	Room for 16 to 31
1100	Room for 8 to 15
1101	Room for 4 to 7
1110	Room for at least 2
1111	Room for at least 1
Others	Reserved

Table 9: FIFO POP Level Indicator Signals

Value	Status
0000	Empty
0001	1 entry in FIFO
0010	At least 2 entries in FIFO
0011	At least 4 entries in FIFO
0100	At least 8 entries in FIFO
0101	At least 16 entries in FIFO
0110	At least 32 entries in FIFO
1000	Less than one-forth to 64 full
1101	One-forth or more full
1110	One-half or more full
1111	Full
Others	Reserved

FIFO Synchronous Flush Procedure

Both PUSH and POP domains are provided with a flush input signal synchronized to their respective clocks. When a flush is triggered from one side of the FIFO, the signal propagates and re-synchronizes internally to the other clock domain. During a flush operation, the values of the FIFO flags are invalid for a specific number of cycles (see **Figure 7** and **Figure 8**).

As shown in **Figure 7**, when the **Fifo_Push_Flush** asserts, the **Almost_Full** and **PUSH_FLAG** signals become invalid until the FIFO can flush the data with regards to the Push clock domain as well as the Pop clock domain. After the **Fifo_Push_Flush** is asserted, the next rising edge of the Pop clock starts the Pop flush routine.

Figure 7 illustrates a FIFO Flush operation. After the **Fifo_Push_Flush** is asserted at 2 (**PUSH_Clk**), two POP clock cycles (**11** and **12**) are required to update the **POP_FLAG**, and **PUSH_FLAG** signals. The **Almost_Empty** signal is asserted to indicate that the push flush operation has been completed. On the following rising edge of the **PUSH_Clk** (7), the **PUSH_FLAG** is accordingly updated to reflect the successful flush operation.

Figure 7: FIFO Flush from PUSH Side

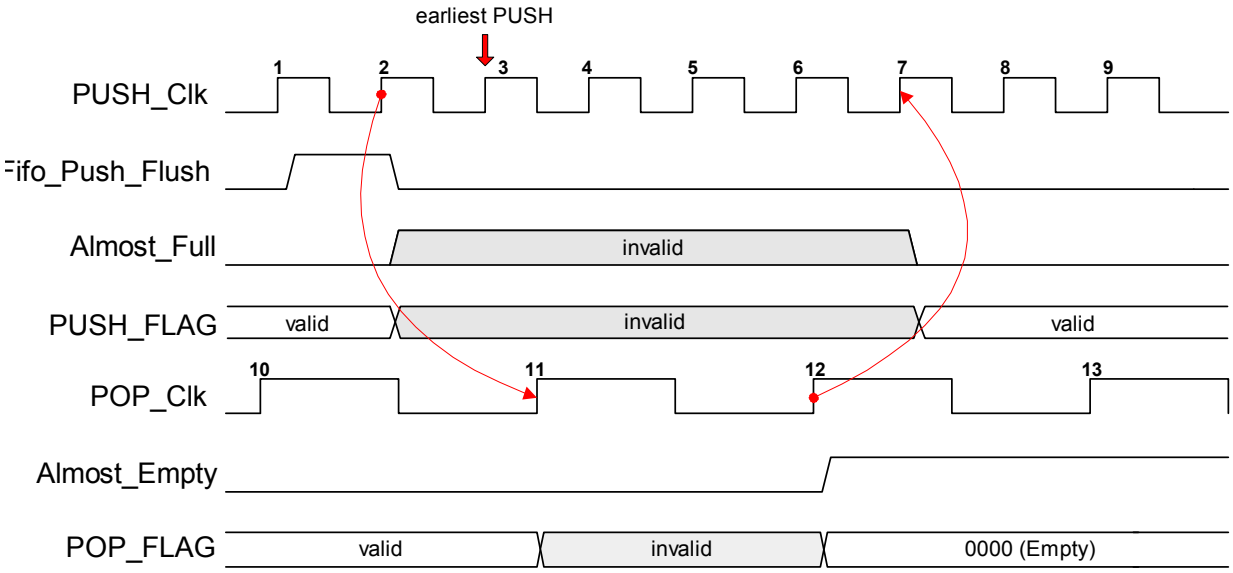


Figure 8 illustrates a POP flush operation. After the **Fifo_Pop_Flush** is asserted at 2 (**POP_Clk**), two PUSH clock cycles (**11** and **12**) are required to update the **POP_FLAG** and **PUSH_FLAG** signals. The **Almost_Empty** signal is asserted to indicate that the pop flush operation has been completed. On the following rising edge of the **POP_Clk** (7), the **POP_FLAG** is updated accordingly to reflect the successful flush operation.

Figure 8: FIFO Flush from POP Side

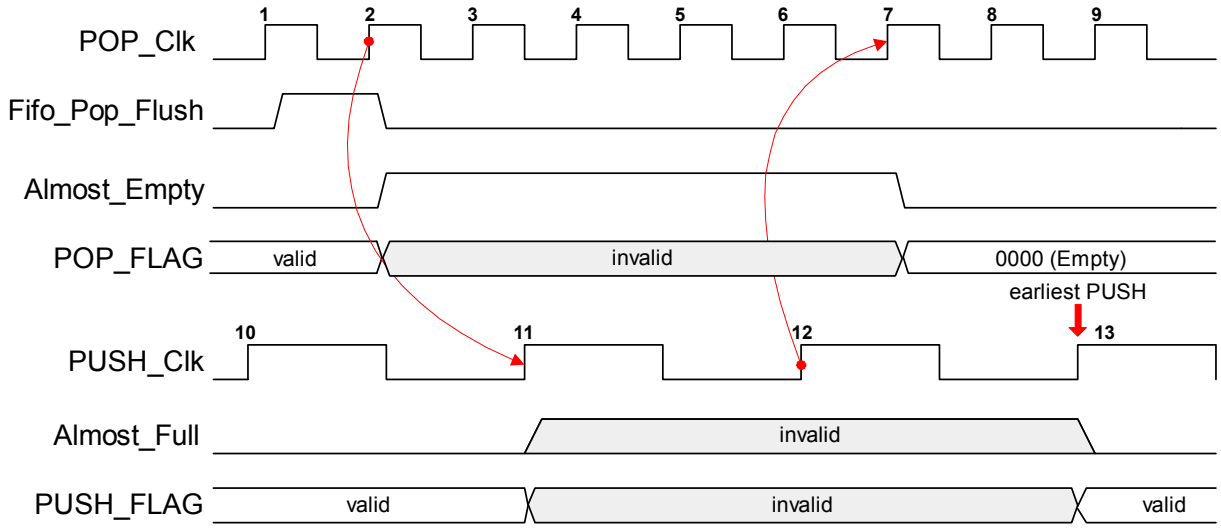


Figure 7 and **Figure 8** are only true for this particular PUSH-POP clock frequency combination. The clock frequency and phase difference between POP_Clk and PUSH_Clk can cause an additional flush delay of one clock cycle in either domain because of the asynchronous relationship between the two clocks.

FIFO Asynchronous Flush

Aside from the synchronous flush controls, there is an asynchronous flush signal named ASYNC_FLUSH. This signal is tied directly to the PUSH and POP pointers without any deglitching circuitry. The designer can add deglitching circuitry if desired.

Distributed Clock Networks

Global Clocks

The PolarPro 3 clock network architecture consists of a 2-level H-tree network as shown in **Figure 9**. The first level of each clock tree (high-lighted in red) spans from the clock input pad to the global clock network and to the center of each quadrant of the chip. The second level spans from the quadrant clock network to the column clock network, and then to every logic cell inside that quadrant. There are five global clocks in the global clock network, and five quadrant clocks in each quadrant clock network. All global clocks drive the quadrant clock network inputs.

The quadrant clocks output to column clock buffers, which can be dynamically disabled at the column level. Column clock buffers can be implemented in Verilog, VHDL, and schematic designs by instantiating the column clock buffer macro, CAND. **Figure 10** shows the schematic representation of the CAND macro. The global clocks can drive RAM block clock inputs and reset, set, enable, and clock inputs to I/O registers. Furthermore, the quadrant clock outputs can be routed to all logic cell inputs.

Figure 9: PolarPro 3 Clock Architecture

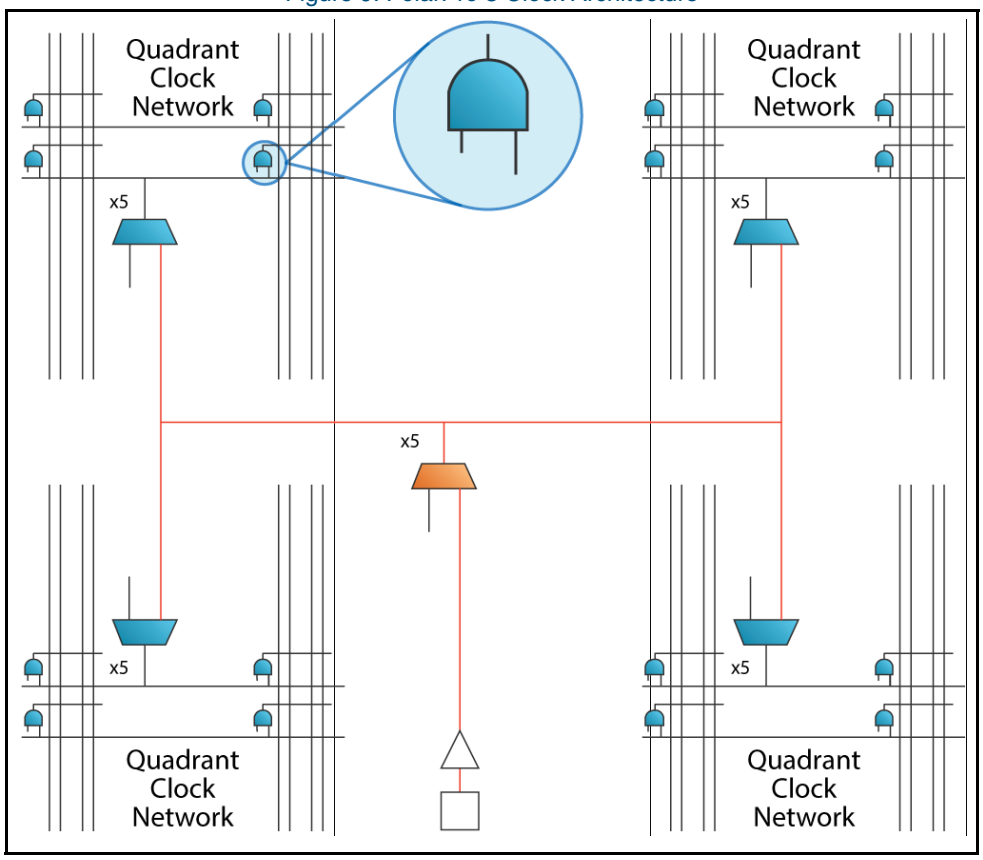
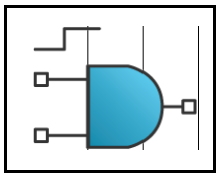


Figure 10: CAND Macro



The five global clock networks can either be driven directly by clock pads or internally generated signals. These global clocks go through 2-input global clock muxes located in the middle of the die. A diagram of a 2-input global clock mux is shown in **Figure 11**.

Figure 11: Global Clock Structure

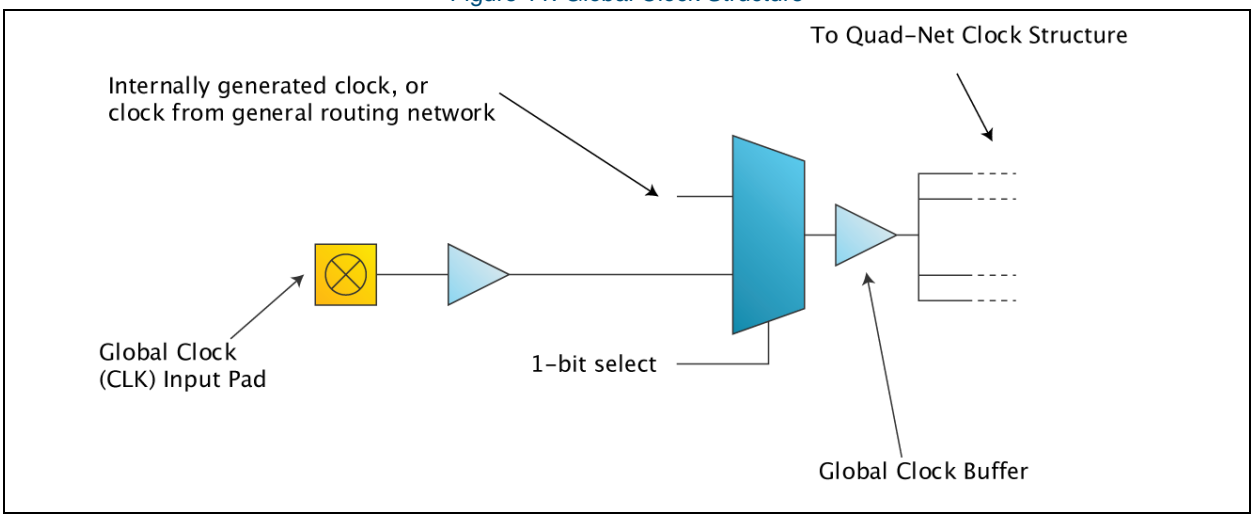
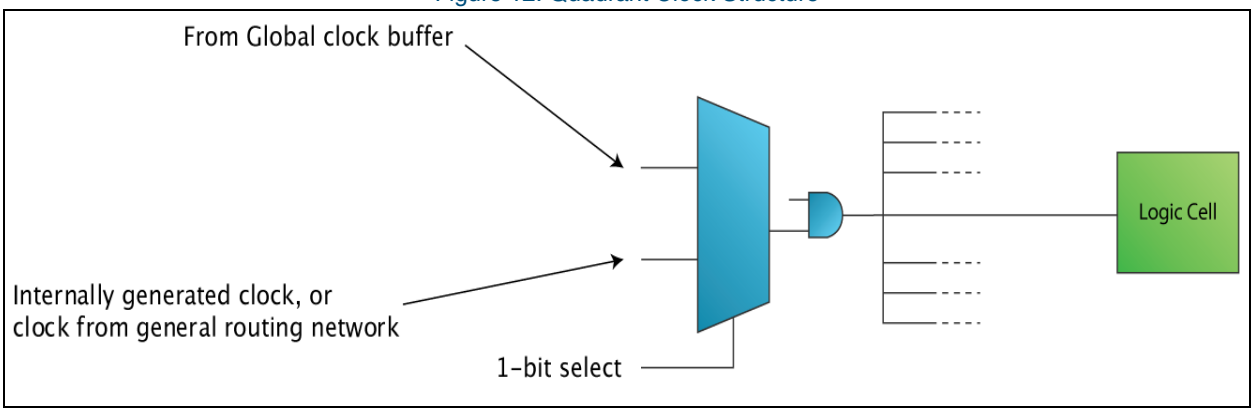


Figure 12 illustrates the quadrant clock 2-input mux.

Figure 12: Quadrant Clock Structure



NOTE: Select lines for the global clock and quadrant clock muxes are static signals and cannot be changed dynamically during device operation.

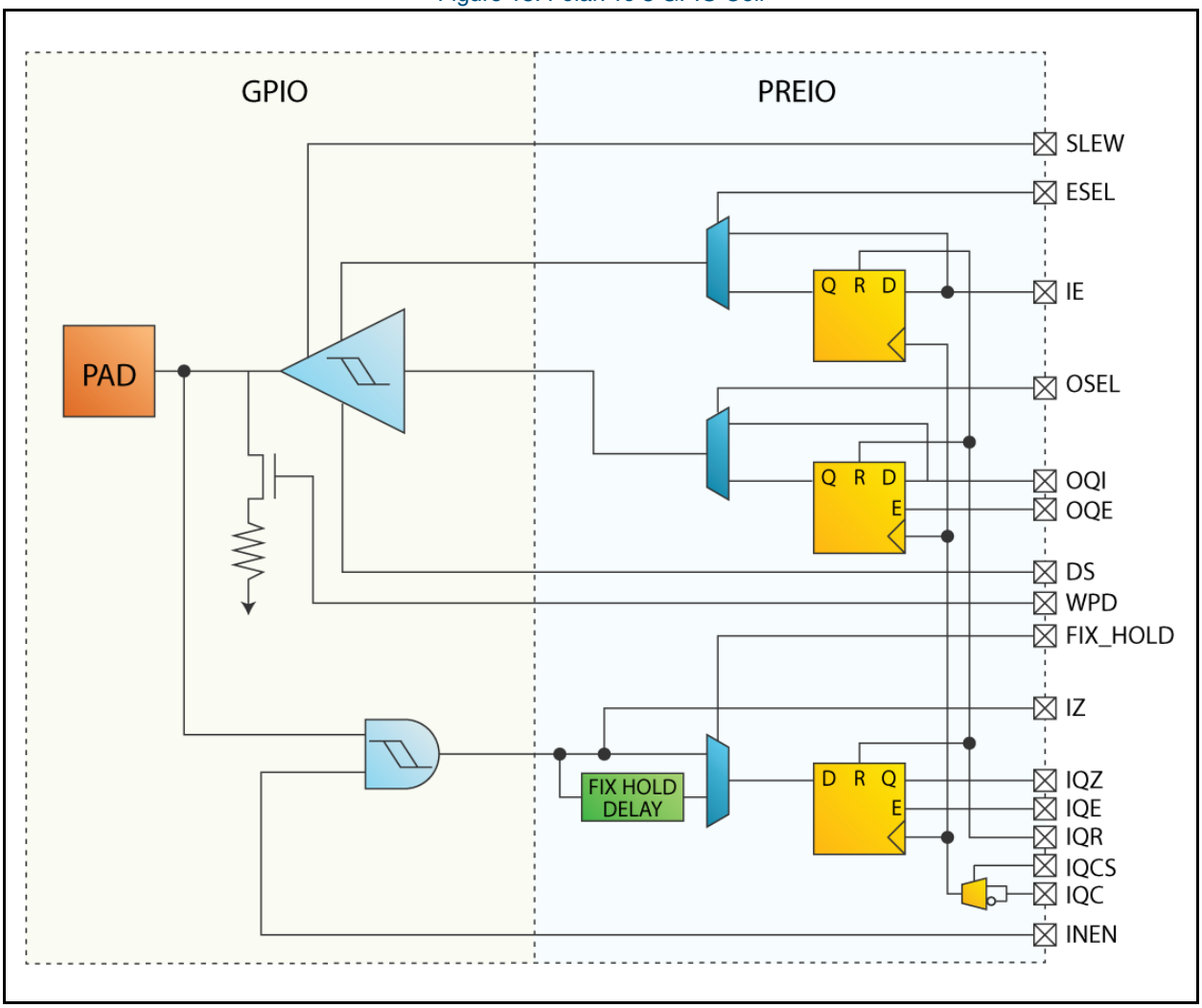
GPIO Cell Structure

The GPIO features include:

- Direct or registered input with input path select
- Direct or registered output with output path select
- Direct or registered output enable with OE path select
- Input buffer enable to reduce power
- Configurable pull-down control
- Inverted or non-inverted clock signal to flip-flops
- Two drive strength options

Figure 13 is a diagram of the PolarPro 3 GPIO cell.

Figure 13: PolarPro 3 GPIO Cell



With bi-directional I/O pins and global clock input pins, the PolarPro 3 device maximizes I/O performance, functionality, and flexibility. All input and I/O pins are 1.8 V, 2.5 V, and 3.3 V tolerant and comply with the specific I/O standard selected. For single ended I/O standards, the corresponding VCCIO bank input specifies the input tolerance and the output drive voltage.

Table 10 describes the GPIO interface signals.

Table 10: GPIO Interface Signals

Signal Name	Direction	Function
Routable Signals		
ESEL	I	Select signal for registered or non-registered output enable.
IE	I	Output enable signal.
OSEL	I	Select signal for registered or non-registered output signal.
OQI	I	Output signal.
OQE	I	Enable signal for output stage flip-flop.
IZ	O	Input data from pad.
IQZ	O	Registered input data from pad.
IQE	I	Enable signal for input stage flip-flop.
IQCS	I	Select signal for clock (inverted or non-inverted). This signal can only be tied high or low.
IQC	I	Clock signal to PREIO flip-flops.
IQR	I	Reset signal to all flip-flops within the GPIO cell.
INEN	I	Input enable signal.
Static Signals		
DS	I	Drive strength control.
WPD	I	Weak pull-down control signal.
FIX_HOLD	I	Additional delay module select signal.

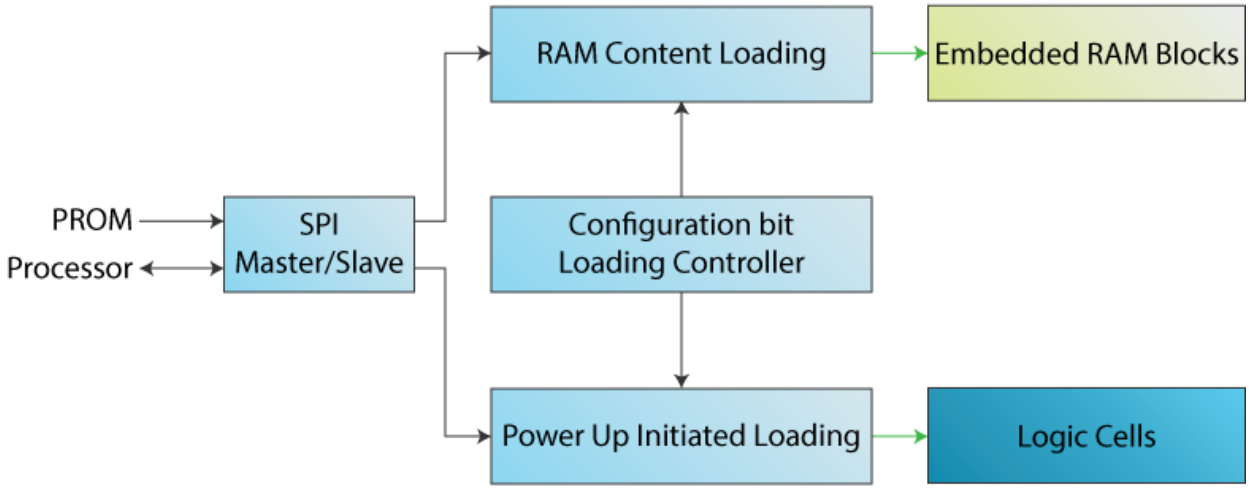
Programmable Weak Pull-Down

A programmable weak pull-down controller is also available on each GPIO. The I/O pull-down eliminates the need for external resistors.

PolarPro 3 Configuration Loading

The PolarPro 3 family of devices are reconfigurable. The configuration of a PolarPro 3 must be loaded each time the device is powered on. As shown in **Figure 14**, the PolarPro 3 provides two interfaces for configuring the logic cells and RAM blocks within the device. These two interfaces are SPI Master and SPI Slave.

Figure 14: Configuration Loading Block Diagram



SPI Modes of Operation

The configuration controller of the PolarPro 3 device can operate as a SPI Master or SPI Slave. When operating in SPI Master mode, PolarPro 3 devices read data from a Programmable Read-Only Memory (PROM). When operating in SPI Slave mode, PolarPro 3 receives data from a processor.

Operation in SPI Master mode or SPI Slave mode is determined by detecting either a logical high or low voltage on the SPI_CS_N pin upon de-assertion of SPI_RST_N.

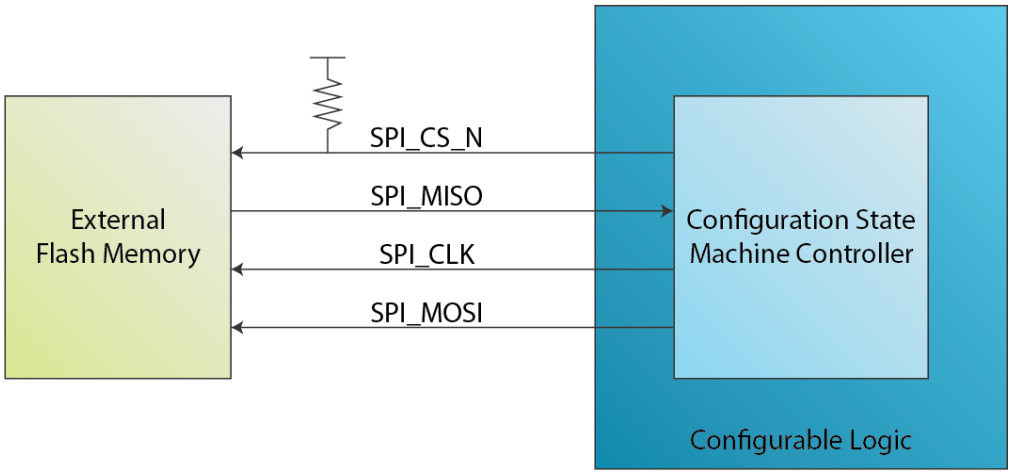
- When SPI_CS_N is high, the PolarPro 3 SPI controller enters SPI Master mode.
- When SPI_CS_N is low, the PolarPro 3 SPI controller enters SPI Slave mode.

Once configuration is completed, the SPI_CS_N, SPI_MOSI, SPI_MISO, and SPI_CLK signals will become normal GPIO.

SPI Master Mode

In SPI Master mode (shown in **Figure 15**), SPI_RST_N must be asserted to hold the PolarPro 3 in a reset state until the PROM is fully powered up and ready to be read. Upon de-assertion of SPI_RST_N, the PolarPro 3 is set to SPI Master mode and will then take control of the SPI pins, and start initiating the required SPI commands.

Figure 15: SPI Master Mode



Configuration loading of the PolarPro 3 requires a PROM of adequate size (at lease 1 Mbit). The PolarPro 3 SPI Master SPI clock frequency can operate at 4 MHz or 16 MHz during configuration. Once configuration is complete, the dual purpose SPI I/O pins can be used as normal GPIO. It is important to note that the VCCIO of the SPI pins for programming and normal operation must match the VCCIO of the PROM.

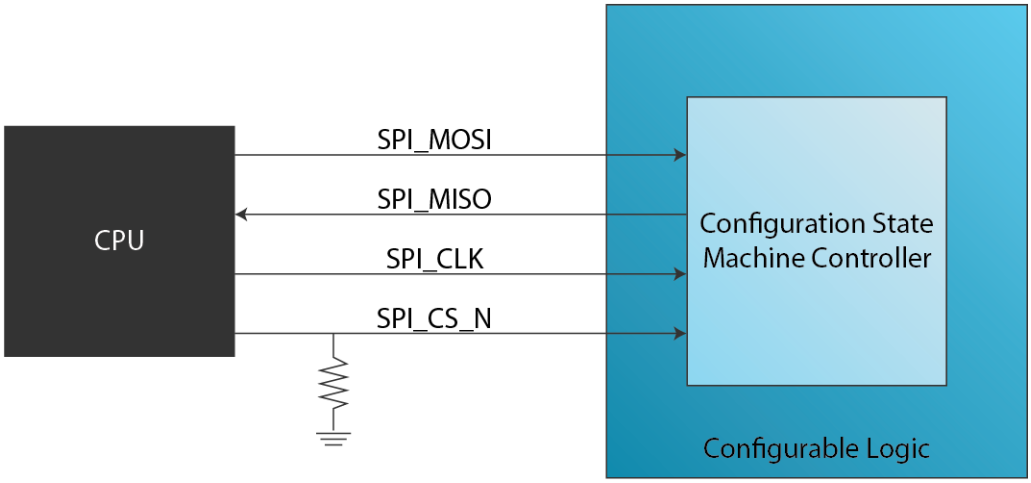
Upon completion of the loading, the PROM can be placed in a deep power down mode. To put the PROM into deep power down mode, the SPI Master sends a power down command after the last byte of data is received. Once the SPI pins switch to normal GPIO, and the PROM is in a deep power down mode, care must be taken to ensure that the PROM is not woken up unintentionally.

The PROM loading file used to program the external flash is generated by QuickLogic's QuickWorks software tools. The configuration data is constructed to work with the corresponding commands from the PolarPro 3 SPI Master.

SPI Slave Mode

When the PolarPro 3 is powered up in SPI Slave mode (shown in **Figure 16**), the SPI Master takes control of the SPI pins. To initiate the data transfer, the SPI Master must assert the SPI_RST_N signal low for at least 20 ns to ensure the PolarPro 3 state machine is reset.

Figure 16: SPI Slave Mode



The configuration bit file, required for specifying the SPI Master commands, is generated by QuickLogic's QuickWorks software tools. The resulting binary file combined with software drivers supplied by QuickLogic can be used for configuration loading of the PolarPro 3.

Configuration Verification Check Sum

To achieve higher system robustness, PolarPro 3 uses a checksum algorithm to guarantee data integrity. Upon receiving the data from the PROM, a check sum mechanism is used to ensure the PolarPro 3 configuration and embedded RAM data is intact. The final checksum is compared to those in the PROM checksum. If the checksums match, the CFG_DONE pin will go high. If the check sum does not match, the configuration controller retries configuration up to five times.

NOTE: Ensure that the SPI_MOSI and SPI_MISO pins are placed correctly. If these two signals are swapped, the CFG_DONE signal will still assert high and appear as if the device was configured correctly. However, it indicates that the request to configure the device with no information is completed.

More details on programming PolarPro 3 devices are located in the *PolarPro 3 Configuration Loading User Guide*.

Electrical Specifications

DC Characteristics

The DC Specifications are provided in **Table 11** through **Table 17**.

Table 11: Absolute Maximum Ratings

Parameter	Value	Parameter	Value
VCC Voltage	-0.5 V to 1.26 V	ESD Pad Protection	2 kV
VCCIO Voltage	-0.5 V to 3.6 V	Laminate Package (BGA) Storage Temperature	-55° C to + 125° C
Input Voltage	-0.5 V to 3.6 V	Latch-up Immunity	±100 mA

Table 12: Recommended Operating Range

Symbol	Parameter	Commercial		Unit
		Min.	Max.	
VCC	Supply Voltage	1.14	1.26	V
VCCIO	Input Tolerance Voltage	1.71	3.6	V
TJ	Junction Temperature	-20	85.0	°C

Table 13: DC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_I	GPIO Input Leakage Current	V_{input} = VCCIO or GND	-	1	-	µA
I_{OZ}	Tri-State Output Leakage Current	V_{input} = VCCIO or GND	-	1	-	µA
CI	I/O Input Capacitance	VCCIO = 3.6 V	-	5	-	pF
C_{CLK}	Clock Input Capacitance	VCCIO = 3.6 V	-	5	-	pF
I_{PD}	Current on programmable pull-down	VCCIO = 3.6 V	-	90	160	µA

Table 14: DC Input and Output Levels[a]

Symbol	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V_{MIN}	V_{MAX}	V_{MIN}	V_{MAX}	V_{MAX}	V_{MIN}	mA	mA
LVTTL	-0.3	0.8	2.2	VCCIO + 0.3	0.4	2.4	2.0	-2.0
LVCMOS25	-0.3	0.7	1.7	VCCIO + 0.3	0.4	1.8	2.0	-2.0
LVCMOS18	-0.3	0.63	1.17	VCCIO + 0.3	0.45	VCCIO - 0.45	2.0	-2.0

a. The data in this table represents JEDEC specifications. QuickLogic devices either meet or exceed these requirements. Based on weak pull-down I/O termination disabled.

Table 15: Quiescent Current

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{VCC}	Quiescent Current on VCC[a]	-	55	-	µA
I_{VCCIO}	Quiescent Current on VCCIO banks A, B, C, and D combined	-	2	-	µA
I_{VCCIO_E}	Quiescent Current on CFG_DONE and SPI_RST_N pins	-	3	-	µA

a. Based on typical process, single cell usage, all outputs tri-stated, and all inputs held at VCCIO or GND.

Table 16: GPIO Programmable Drive Strength

Drive Strength[a]	IOH (mA)			IOL (mA)		
	1.8 V	2.5 V	3.3 V	1.8 V	2.5 V	3.3 V
0	14	30	41	14	17	20
1	16	35	51	20	21	24

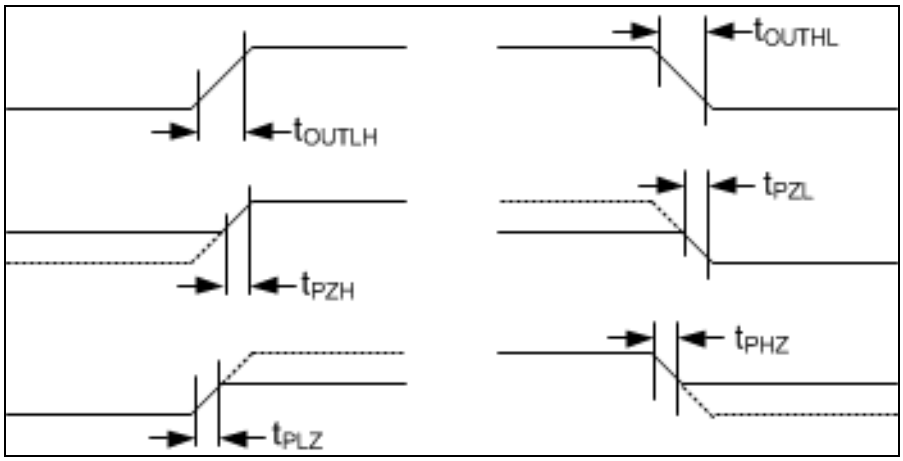
a. Values are based on input and output levels in **Table 14**.

Table 17: Output Slew Rate

Symbol	Parameter[a]	VCCIO (V)	Drive Strength = 1 (ns)	Drive Strength = 0 (ns)
t_{OUTLH}	Output Delay low to high (90% of H)	3.3	5.24	5.92
		2.5	6.48	8.21
		1.8	9.25	11.12
t_{OUTHL}	Output Delay high to low (10% of L)	3.3	5.35	5.98
		2.5	6.25	7.40
		1.8	8.58	11.12
t_{PZH}	Output Delay tri-state to high (90% of H)	3.3	2.13	2.25
		2.5	2.65	2.93
		1.8	2.55	3.01
t_{PZL}	Output Delay tri-state to low (10% of L)	3.3	0.30	0.41
		2.5	2.49	2.51
		1.8	1.95	2.36
t_{PHZ}	Output Delay high to tri-state	3.3V	3.88	4.06
		2.5V	4.42	4.52
		1.8V	3.97	4.31
t_{PLZ}	Output Delay low to tri-state	3.3V	0.60	0.60
		2.5V	3.65	3.81
		1.8V	2.69	2.79

a. Based on 15pF load.

Figure 17: Output Slew Rate



SPI Timing Characteristics

The SPI specifications are provided in **Table 18** through **Table 23**.

Table 18: SPI Master Timing

Symbol	Parameter	Value	
		Slow SPI_CLK	Fast SPI_CLK
t_{MFCMIN}	Minimum time from de-assertion of CFG_RST_N to the first SPI_CLK rising edge.	115 µs	115 µs
t_{MSUMIN}	Minimum setup time that the SPI Master output data will give before a SPI_CLK sampling edge.	105 ns	26 ns

When operating as the SPI Master, the PolarPro 3 initially reads an external SPI flash device using a slow clock (~4 MHz). After reading one byte, it determines whether it will switch over to use the fast clock (~16 MHz) or not. This improves configuration time by a factor of four for SPI flash devices that can support the speed.

Table 19: SPI Master SPI_CLK Timing

SPI Mode	Parameter	Value
SPI Master	Slow Output Frequency Range	4 MHz ±22%
	Fast Output Frequency Range	16 MHz ±22%

Table 20: SPI Slave Timing

Symbol	Parameter	Value	
		Slow SPI_CLK	Fast SPI_CLK
t_{SFCMIN}	Minimum time from de-assertion of CFG_RST_N to when the first SPI_CLK rising edge can be sent to the PolarPro 3.	20 ns	20 ns
t_{SSUMIN}	Minimum setup time that the SPI_MOSI requires for input data.	9 ns	9 ns
t_{SHMIN}	Minimum hold time that the SPI_MOSI signal needs after sampling the data relative to the SPI_CLK edge.	300 ps	300 ps

Table 21: SPI Slave SPI_CLK Timing

SPI Mode	Parameter	Value
SPI Slave	SPI_CLK Input Frequency Range	200 kHz to 25 MHz

Table 22: SPI_RST_N Timing

Symbol	Parameter	Value
$t_{RST\_BGN\_MIN}$	Minimum time, after the VCC and VCCIO rails have reached their voltage, that SPI_RST_N should be high before asserting.	250 µs
$t_{RST\_ASRT\_MIN}$	Minimum time that SPI_RST_N must be asserted to reset the device correctly, and begin configuration.	20 ns

Table 23: CFG_DONE Timing

Symbol	Parameter	Value
t_{CFG_DONE}	Time from when CFG_DONE goes high, to when the device begins operation.	320 ns

Programmable Fabric

Table 24 shows the logic cell delays in the programmable fabric.

Table 24: Logic Cell Delays

Symbol	Parameter	Min.	Max.
t_{PD}	Combinatorial delay of the longest path: time taken by the combinatorial circuit to output	0.34 ns	1.01 ns
t_{SU}	Setup time: time the synchronous input of the flip-flop must be stable before the active clock edge	0.16 ns	0.49 ns
t_{HL}	Hold time: time the synchronous input of the flip-flop must be stable after the active clock edge	0 ns	N/A
t_{ESU}	Enable setup time: time the enable input of the flip-flop must be stable before the active clock edge	0.60 ns	1.8 ns
t_{EHL}	Enable hold time: time the enable input of the flip-flop must be stable after the active clock edge	0 ns	0 ns
t_{CO}	Clock-to-out delay: the amount of time taken by the flip-flop to output after the active clock edge	0.33 ns	1 ns
t_{CWHI}	Clock high time: required minimum time the clock stays high	600 ps	600 ps
t_{CWLO}	Clock low time: required minimum time that the clock stays low	600 ps	600 ps
t_{SET}	Set delay: time between when the flip-flop is “set” (high) and the output is consequently “set” (high)	0.42 ns	1.26 ns
t_{RESET}	Reset delay: time between when the flip-flop is “reset” (low) and the output is consequently “reset” (low)	0.48 ns	1.44 ns
t_{SW}	Set width: time that the SET signal must remain high/low	300 ps	300 ps
t_{RW}	Reset width: time that the RESET signal must remain high/low	300 ps	300 ps

Figure 18 illustrates the logic cell flip-flop timings.

Figure 18: Logic Cell Flip-Flop Timings — First Waveform

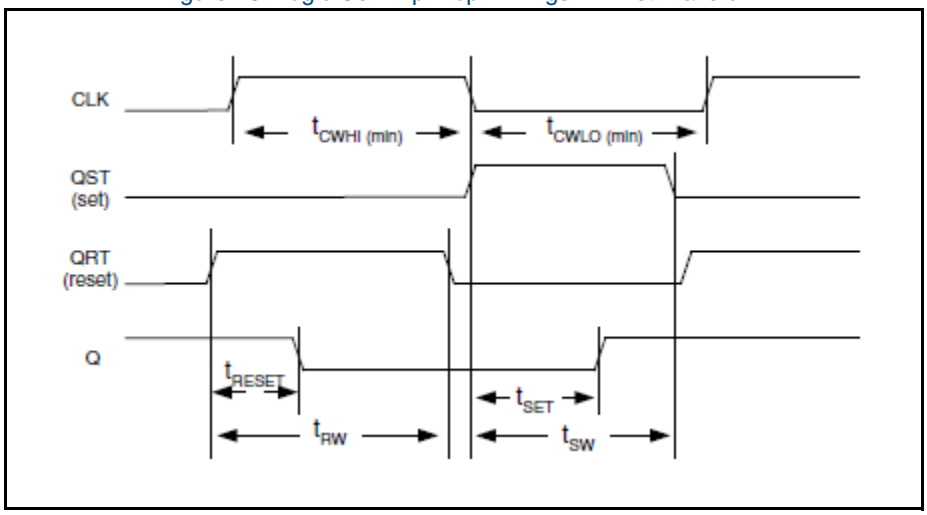


Table 25 shows the tree clock delays in the programmable fabric.

Table 25: Tree Clock Delay

Clock Segment	Parameter	Min.	Max.
t_{PGCK}	Clock pad to flip-flop	1.69 ns	3.9 ns
t_{PGMCK}	Global mux output to flip-flop	0.83 ns	1.96 ns
t_{PQDCK}	Quadrant mux output to flip-flop	0.67 ns	1.59 ns
t_{GSKEW}	Global delay clock skew	1.8 ps	4.1 ps

Power-Up Sequencing

Figure 19: Power-Up Sequencing

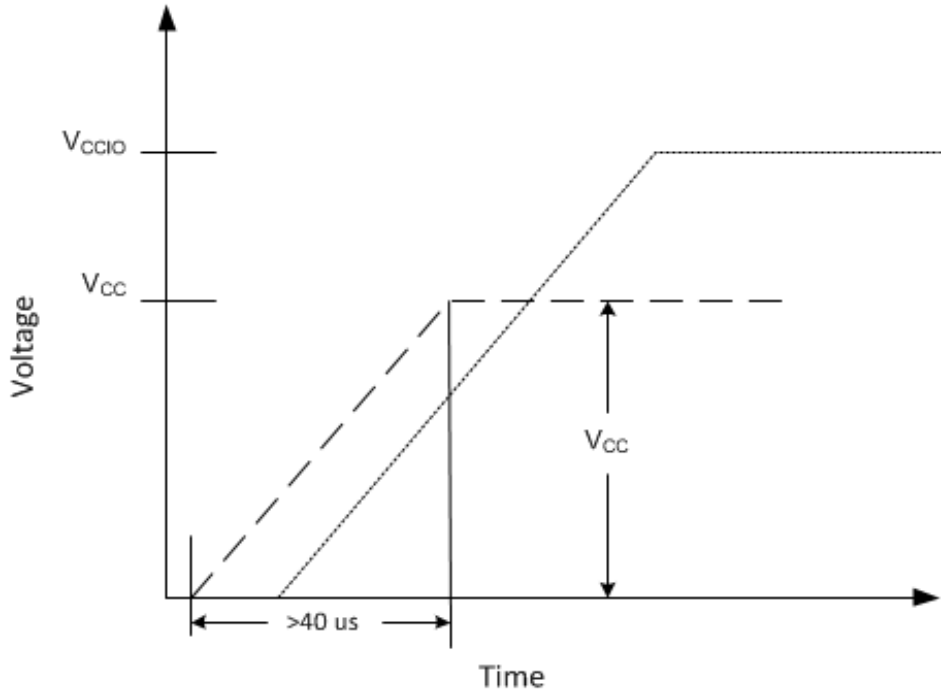


Figure 19 shows an example where all VCCIO = 3.3 V. When powering up a PolarPro 3 device, VCC and VCCIO rails must take 40 µs or longer to reach their maximum values. Ramping VCC and VCCIO faster than 40 µs can cause the device to behave improperly. It is also important to ensure VCC precedes VCCIO. In the case where VCCIO ramps up prior the VCC, additional current will be drawn. SPI_RST_N should not be asserted until 250 µs after VCC reaches its full voltage level.

Power Consumption

QuickLogic's ultra low power reconfigurable logic is ideal for implementing connectivity solutions, custom logic and processor interfaces. The quiescent current can be as low as 55 µA. The dynamic power consumption varies depending on the operating conditions and what functions are used in the logic cells. Contact your QuickLogic Customer Solution Architect (CSA) for specifics related to your use case.

Moisture Sensitivity Level

Table 26 describes the solder composition characteristics.

Table 26: Solder and Lead Finish Composition

Package Type[a]	Ball Count	Lead Type	PB-Free	Moisture Sensitivity Level
WLCSP (2.09 mm x 2.54 mm)	30	BGA Solder	Sn-Ag-Cu	1
VFBGA (3.5 mm x 3.5 mm)	64	BGA Solder	Sn-Ag-CU	3

a. WLCSP = Wafer Level Chip Scale Package
VFBGA = Very-thin Fine-pitch Ball Grid Array

Package Thermal Characteristics

The PolarPro 3 solution platform is available for Commercial (-20°C to 85°C Junction) temperature ranges.

Thermal Resistance Equations:

$\theta_{JC} = (T_J - T_C)/P$
$\theta_{JA} = (TJ - TA)/P$
$P_{MAX} = (T_{JMAX} - T_{AMAX})/\theta_{JA}$

Parameter Description:

θ_{JC}: Junction-to-case thermal resistance

θ_{JA}: Junction-to-ambient thermal resistance

T_J: Junction temperature

T_A: Ambient temperature

P: Power dissipated by the device while operating

P_{MAX}: The maximum power dissipation for the device

T_{JMAX}: Maximum junction temperature

T_{AMAX}: Maximum ambient temperature

NOTE: Maximum junction temperature (T_{JMAX}) is 125°C. To calculate the maximum power dissipation for a device package look up θ_{JA} from **Table 27**, pick an appropriate T_{AMAX} and use: $P_{MAX} = (125°C - T_{AMAX})/ \theta_{JA.}$

Table 27: Package Thermal Characteristics

Device	Package Description			Theta-JC (° C/W)	Air Flow (m/sec)	Theta-JA (° C/W)
	Package Code	Package Type	Pin Count			
PolarPro 3	WDN	WLCSP (2.09 mm x 2.54 mm)	30	5.3	0.0	71.5
					0.5	66.4
					1.0	65.0
					1.5	64.1
	PDN	VFBGA (3.5 mm x 3.5 mm)	64	36.3	0.0	69.9
					0.5	67.6
					1.0	66.7
					1.5	66.1

Reflow Profile

QuickLogic follows IPC/JEDEC J-STD-020 specification for lead-free devices. **Figure 20** shows the Pb-free component preconditioning reflow profile.

Figure 20: Pb-Free Component Preconditioning Reflow Profile

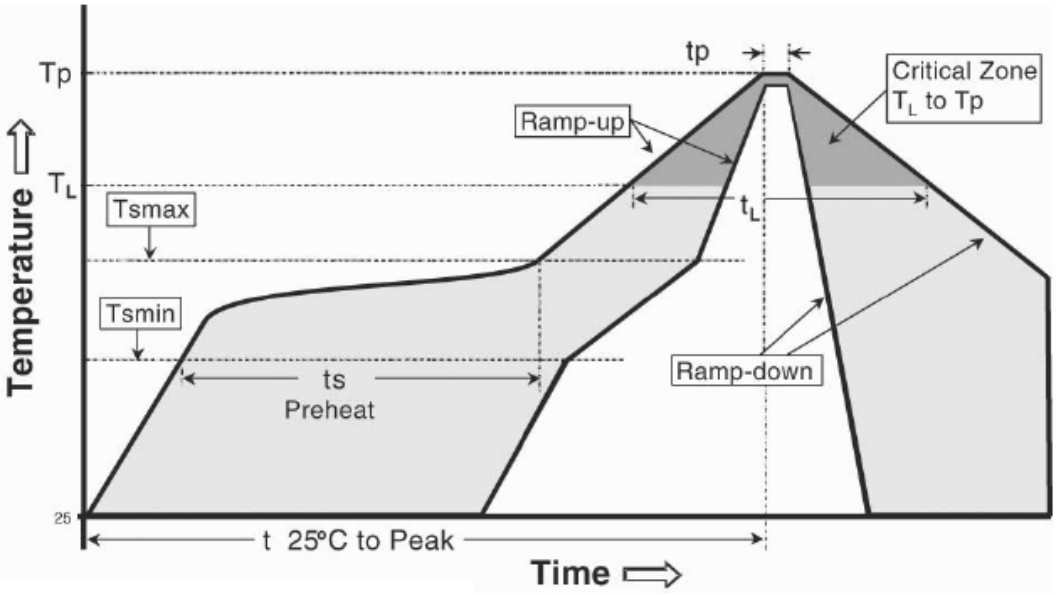


Table 28 shows the Pb-free component preconditioning reflow profile.

Table 28: Pb-Free Component Preconditioning Reflow Profile[a,b]

Profile Feature	Profile Conditions
Average ramp-up rate (Ts_{max}) to Tp)	3° C per sec. max.
Preheat: - Temperature Min (Ts_{min}) - Temperature Max (Ts_{max}) - Time (Ts_{min} to Ts_{max}) (ts)	150°C 200°C 60 sec. to 120 sec.
Time maintained above: - Temperature (T_L) - Time (t_L)	217°C 60 sec. to 150 sec.
Peak Temperature (Tp)	260°C
Time within 5°C of actual Peak Temperature (260°C)	20 sec. to 40 sec.
Ramp-down Rate	6°C per sec. max.
Time 25°C to Peak Temperature	8 min. max.

a. The above conditions are used for component qualifications. This should not be interpreted as the recommended profile for board mounting. Customers should optimize their board mounting reflow profile based on their specific conditions such as board design, solder paste, etc.
b. All temperatures are measured on the package body surface.

Pin Descriptions

Pin descriptions are provided in **Table 29**.

Table 29: Pin Descriptions

Pin	Direction	Function	Description
Dedicated Pin Descriptions			
CLK_1 - CLK_5/ GPIO(D:A)	I	Global clock network pin Low skew global clock	Capable of being a general purpose I/O, or as a clock. When used as a clock, this pin provides access to a distributed network capable of driving the CLOCK, SET, RESET, all inputs to Logic Cells, READ, and WRITE CLOCKS, Read and Write Enables of the Embedded RAM Blocks, and I/O inputs. The letter inside the parenthesis means that the I/O is located in the Bank with that letter.
GPIO(A)	I/O	General Purpose Input/Output pin	The I/O pin is a bi-directional pin, configurable to either an input-only, output-only, or bi-directional pin. Since Bank A is also used by the SPI interface, the I/O voltages of signals on Bank A must match the SPI interface.
GPIO(D:B)	I/O	General Purpose Input/Output pin	The I/O pin is a bi-directional pin, configurable to either an input-only, output-only, or bi-directional pin. The letter inside the parenthesis means that the I/O is located in the Bank with that letter.
VCC	I	Power supply pin	Connect to 1.2V supply.
VCCIO(A)	I	Input voltage tolerance pin	This pin provides the flexibility to interface the device with either a 3.3 V, 2.5 V, or 1.8 V device. VCCIO A is also used by the SPI interface.
VCCIO(E:B)	I	Input voltage tolerance pin	This pin provides the flexibility to interface the device with either a 3.3 V, 2.5 V, or 1.8 V device. The letter inside the parenthesis means that VCCIO is located in the BANK with that letter.
GND	I	Ground pin	Connect to ground
SPI Pin Descriptions			
SPI_RST_N(E)	I	SPI Reset	Reset input (active low). To initiate configuration loading.
CFG_DONE(E)	O	SPI Configuration Done	Configuration done output. Outputs a logic 1 when configuration is successful.
SPI_CS_N(A)	I/O	SPI Chip Select	Selects the SPI mode of operation upon de-assertion of SPI_RST_N. “1” – Master mode “0” – Slave mode
SPI_MISO(A)	I/O	SPI Master Input/Slave Output	Master Input/Slave Output.
SPI_MOSI(A)	I/O	Master Output/Slave Input	Master Output/Slave Input.
SPI_CLK(A)	I/O	SPI Clock	Dual function clock signal. Output in Master mode and input in Slave mode.

Recommended Unused Pin Terminations for PolarPro 3 Devices

All unused, general purpose I/O pins can be tied to their respective VCCIO, GND, weak pull-down resistor, or can be left floating.

Packaging Pinout Tables

PolarPro 3 – 30-Ball (2.09 mm x 2.54 mm) WLCSP Pinout

Table 30: PolarPro 3 – 30-Ball (2.09 mm x 2.54 mm) WLCSP Pinout

Ball	Function	Ball	Function	Ball	Function	Ball	Function
A1	SPI_MOSI/GPIO(A)	B4	GND	D2	VCCIO(C)	E5	GPIO(D)
A2	SPI_MISO/GPIO(A)	B5	VCCIO(E)	D3	VCCIO(D)	F1	GPIO(C)
A3	CLK_5/GPIO(A)	C1	GND	D4	GPIO(D)	F2	CLK_3/GPIO(C)
A4	GND	C2	SPI_CS_N/GPIO(A)	D5	GPIO(D)	F3	CLK_1/GPIO(C)
A5	SPI_CFG_DONE(E)	C3	VCC	E1	GPIO(C)	F4	GPIO(C)
B1	CLK_4/GPIO(A)	C4	GPIO(D)	E2	CLK_2/GPIO(C)	F5	GPIO(D)
B2	VCCIO(A)	C5	SPI_RST_N(E)	E3	GND		
B3	SPI_CLK/GPIO(A)	D1	VCC	E4	GPIO(D)		

PolarPro 3 – 64-Ball (3.5 mm x 3.5 mm) VFBGA Pinout

Table 31: PolarPro 3 – 64-Ball (3.5 mm x 3.5 mm) VFBGA Pinout

Ball	Function	Ball	Function	Ball	Function	Ball	Function
A1	SPI_CFG_DONE(E)	C1	SPI_RST_N(E)	E1	GPIO(D)	G1	GPIO(D)
A2	GPIO(A)	C2	GPIO(D)	E2	GPIO(D)	G2	GPIO(C)
A3	SPI_CS_N/GPIO(A)	C3	GPIO(D)	E3	VCCIO(D)	G3	GPIO(C)
A4	CLK_5/GPIO(A)	C4	GND	E4	GND	G4	VCCIO(C)
A5	CLK_4/GPIO(A)	C5	GND	E5	VCC	G5	CLK_3/GPIO(C)
A6	SPI_MOSI/GPIO(A)	C6	GND	E6	VCC	G6	GPIO(B)
A7	GPIO(A)	C7	GPIO(B)	E7	GPIO(B)	G7	GPIO(B)
A8	GPIO(B)	C8	GPIO(B)	E8	VCCIO(B)	G8	GPIO(B)
B1	VCCIO(E)	D1	GPIO(D)	F1	GPIO(D)	H1	GPIO(D)
B2	GPIO(A)	D2	GPIO(D)	F2	GPIO(C)	H2	GPIO(C)
B3	SPI_CLK/GPIO(A)	D3	GPIO(D)	F3	CLK_1/GPIO(C)	H3	GPIO(C)
B4	VCCIO(A)	D4	GND	F4	GPIO(C)	H4	CLK_2/GPIO(C)
B5	SPI_MISO/GPIO(A)	D5	VCC	F5	GND	H5	GPIO(C)
B6	GPIO(A)	D6	VCC	F6	GND	H6	GPIO(C)
B7	GPIO(A)	D7	GPIO(B)	F7	GPIO(B)	H7	GPIO(C)
B8	GPIO(B)	D8	GPIO(B)	F8	GPIO(B)	H8	GPIO(B)

Package Mechanical Drawings

Figure 21: PolarPro 3 – 30-Ball (2.09 mm x 2.54 mm) WLCSP

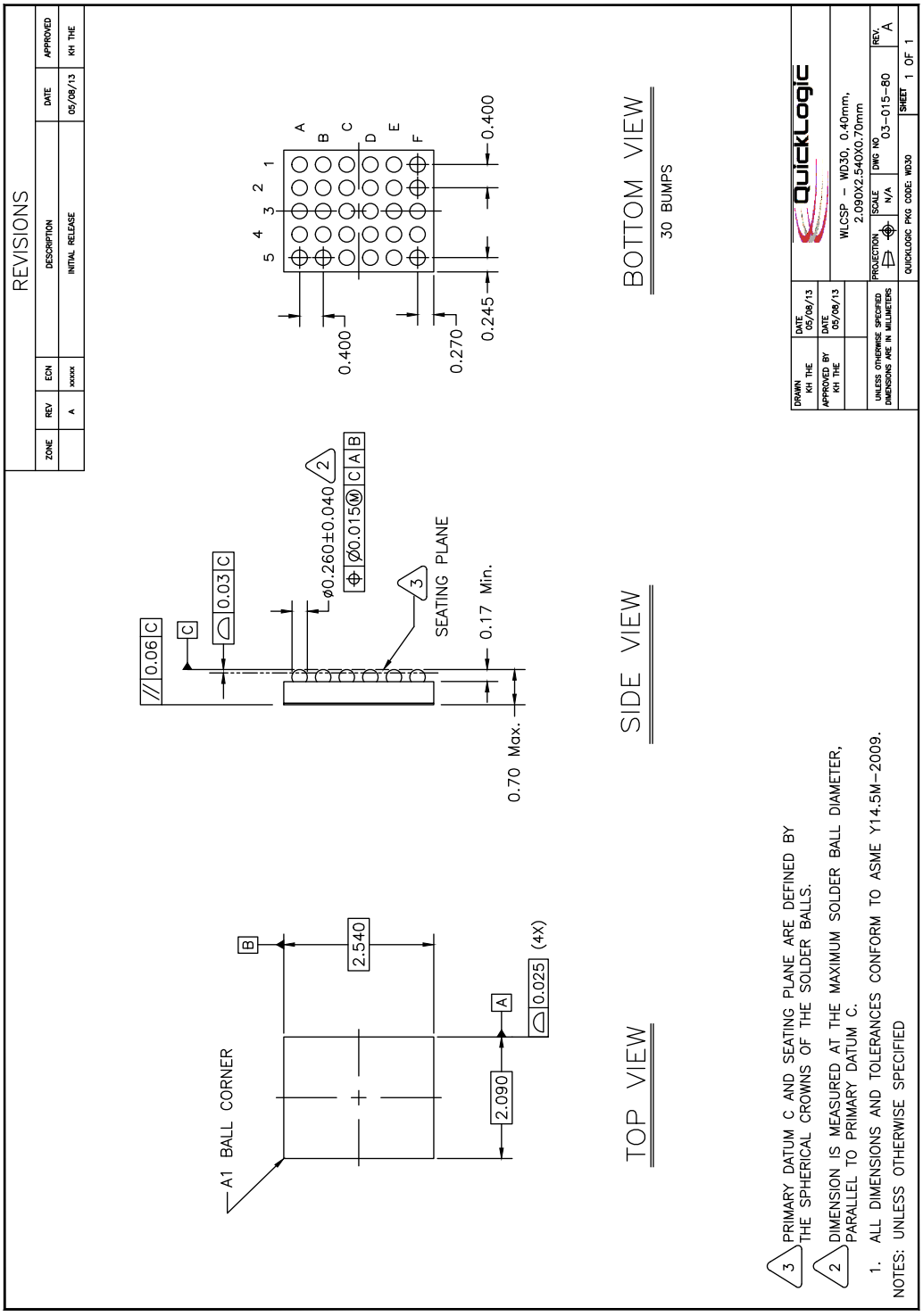
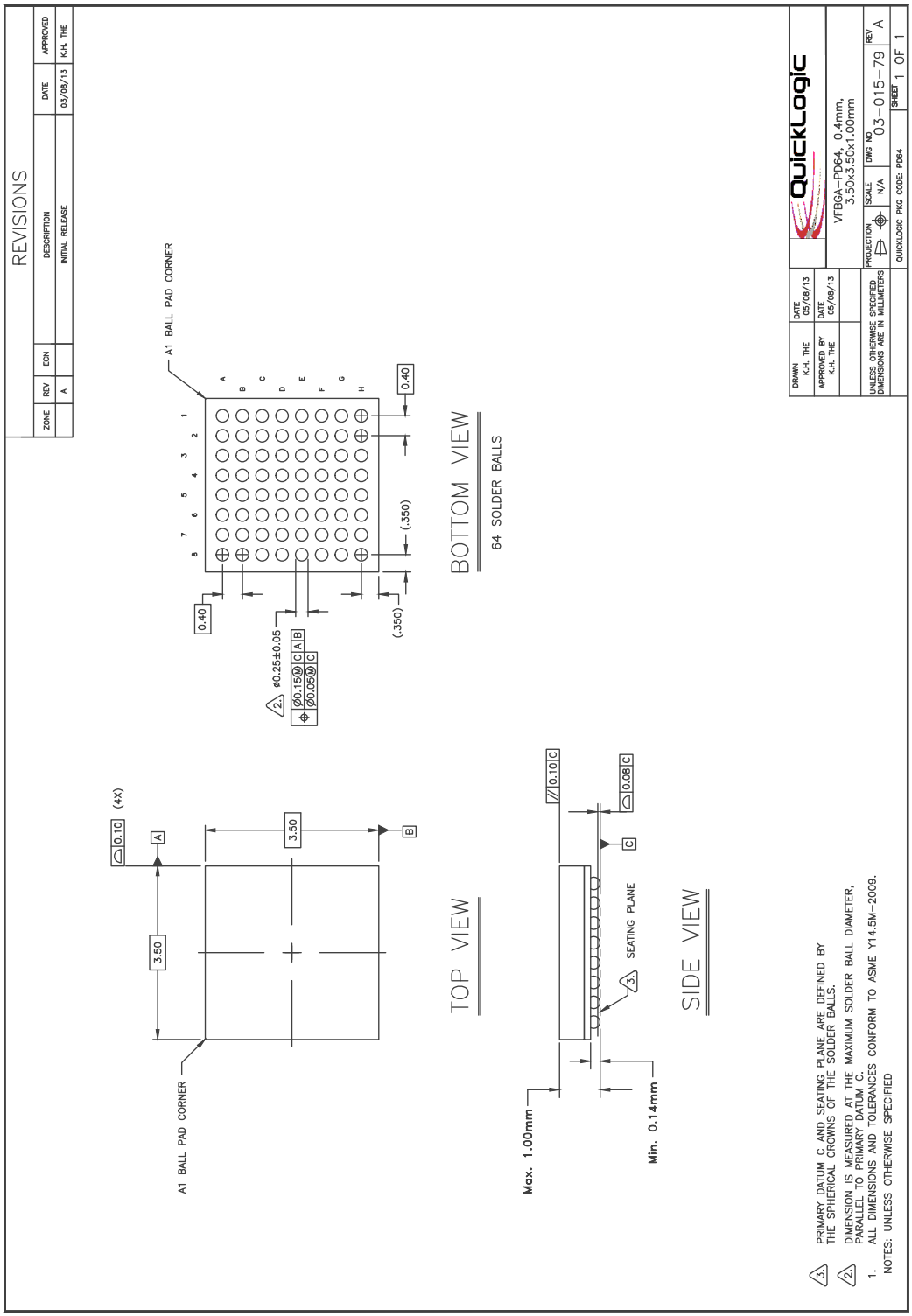


Figure 22: PolarPro 3 – 64-Ball (3.5 mm x 3.5 mm) VFBGA



PCB Design Guidelines

Figure 23: WLCSP – PCB Design Guidelines

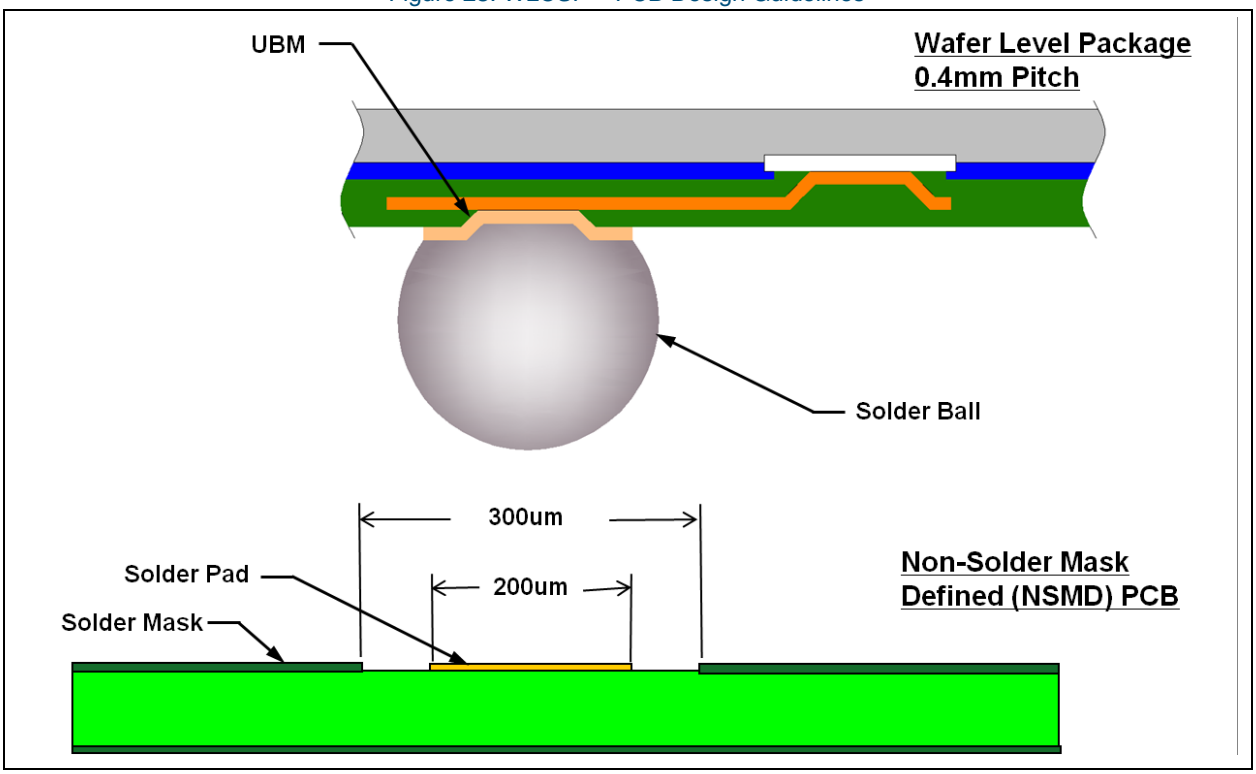
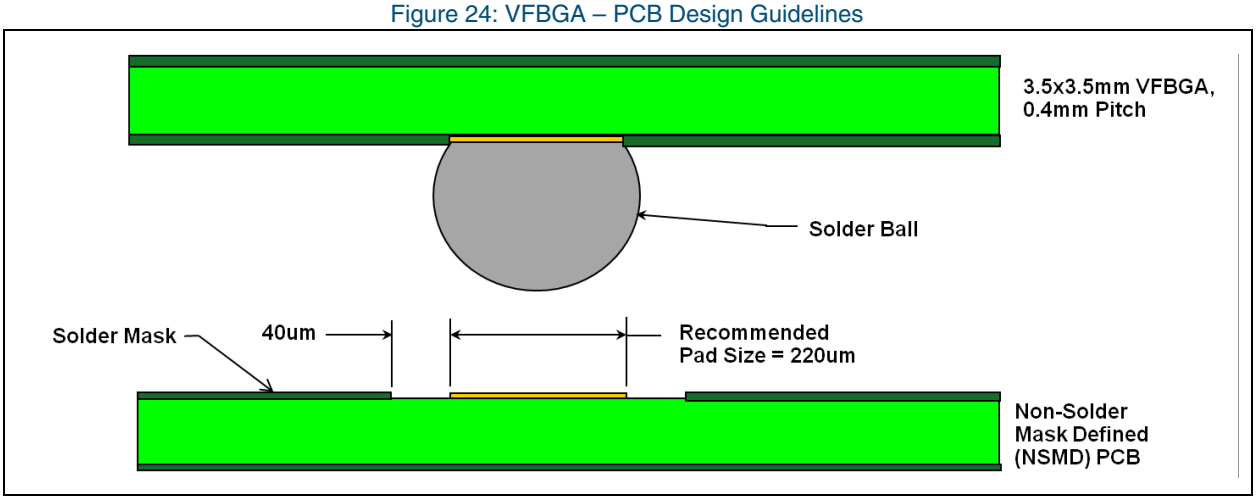


Figure 24: VFBGA – PCB Design Guidelines



PCB Layout Guidelines

When designing a PolarPro 3 PCB, extreme care must be given to the following areas:

- Device interface signals: clock and other data lines that run between devices on the PCB.
- Power going into the device from the connector: the power lines to the PolarPro 3 device must be filtered to pass only low frequency signals of less than 100 kHz. The ground signals must have returned current during data transmission.
- External clock circuit.

Generic Layout Guidelines

The following generic guidelines are from QuickLogic for a board design that contains PolarPro 3 devices. PCB designers should consult internal PCB design rules and recommendations, as well as other device manufacturers, to produce a working PCB.

Important PCB design elements include:

- Type of circuit (analog, digital, etc.)
- Board size
- Number of layers
- Pad stack sizes
- Hole sizes
- Layer thickness
- Board thickness
- External connections
- Mounting holes
- Supply and ground layer thickness
- Component details with specifications

Important design rules are:

- Power distribution and coupling
- Critical signal paths
- IR [Current (I) x Resistance (R)] drops in signal and power traces
- Impedance control
- Pad/land geometries
- Trace width/spacings
- Plated/unplated hole sizes
- Part placement constraints

- Layer assignments and routing constraints
- Heat-removal paths
- Test requirements

Partitioning

The following guidelines are recommended for system partitioning:

- Divide the system into subsystems for placement. The division is used for layout partitioning of circuitries. Group components belonging to a functional block together.
- Isolate sensitive circuits (such as clocks and analog supplies) from noisy sources (such as high transition signals and power regulators).
- Separate analog power supplies from digital power supplies.

Placement

A system with a PolarPro 3 is comprised of a set of interacting elements responding to inputs to produce outputs. Good placement for logical data flow is important to keep the number of layers to a minimum.

The following guidelines are recommended for placement of components:

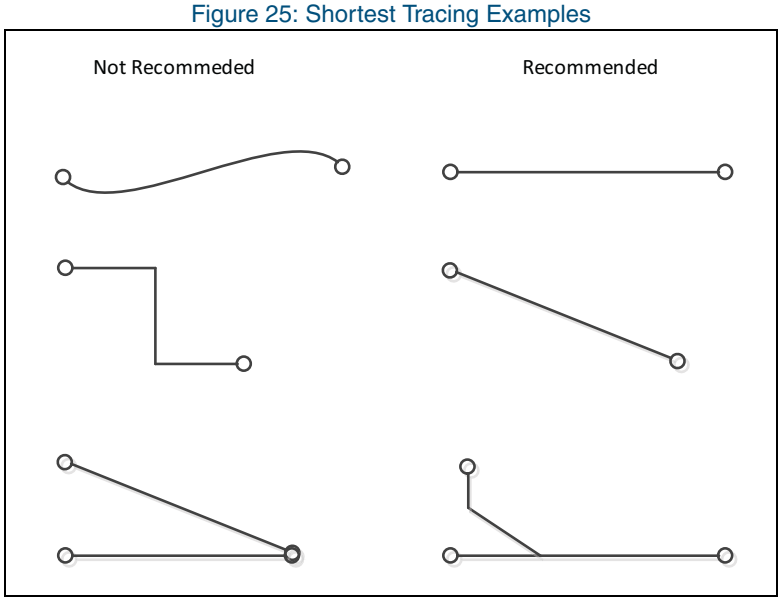
- For highly-sensitive circuits, place the critical components first to produce minimum trace-length.
- For less-critical circuits, arrange the components in the order of the signal flow to minimize the overall connection length.
- For components that have many connecting points, place these components first and group the remaining ones around them.
- For components with a fixed position (such as connectors), place these components first followed by components that are connected to the fixed components.
- Place the larger components (such as main devices) first. Place the smaller components (such as capacitors and resistors) between the larger components.
- Place components in rows or columns for good viewing.
- Place decoupling capacitors as close as possible (preferably adjacent) to the power pins of the device for maximum effectiveness.

Routing

The following guidelines are recommended for routing:

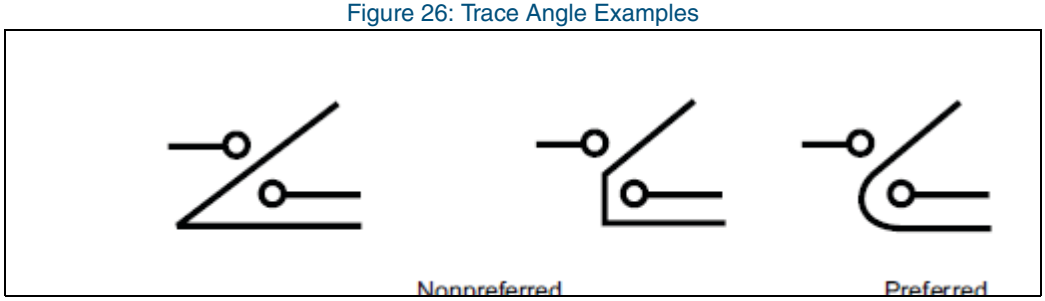
- Select the shortest interconnection length, especially for high frequency circuits (see **Figure 25**).

Figure 25: Shortest Tracing Examples



- Place traces with a minimum angle of 60 degrees (see **Figure 26**).

Figure 26: Trace Angle Examples



- Place parallel traces at the same angle to ensure uniformity, and eliminate the variance in the traces spacing.
- Distribute the spacing equally when one or more traces pass between pads or other conductive areas. To obtain maximum spacing, place traces perpendicular to a narrow passage.
- Distribute traces widely over the available area to avoid issues in manufacturing (i.e., do not space parallel running traces closely).
- Avoid unwanted bunching.
- Match signal impedance for all high-speed signals.
- Ensure that power lines are as thick as possible. Check the current requirements for the line.
- Ensure that the ground traces are always two times wider than the power traces.
- Distribute the routing pattern equally between the various layers of the PCB to achieve uniform plating in the manufacturing process.

- Route adjacent signal layers orthogonally to each other.
- Place ground or power planes to isolate signal layers when possible.
- Route traces directly to a connector pad without line branching to prevent reflections and impedance changes.
- Use curves or two 45° turns to avoid minor line reflections.
- Avoid line-width changes that can affect trace impedance.
- Make pads with soldered signal traces tear-dropped at the pad junction.

Power

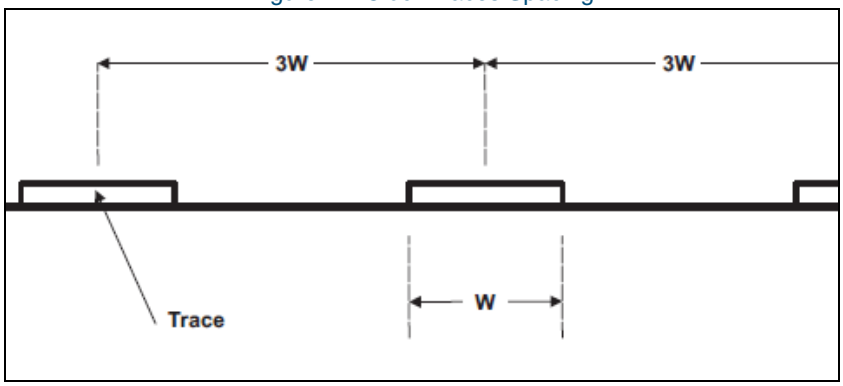
Switching power regulators are noisy and can cause noise-coupling issues if placed close to sensitive areas on the PCB. Keep these circuits away from the sensitive traces, clock circuits and connectors.

Clock Routing

The following guidelines are recommended for clock routing:

- Use series terminator resistors to eliminate reflections. Obtain the final value by looking at the waveform using a high-speed oscilloscope to obtain minimum distortion on the signal.
- Use the 3W spacing rule when routing clock traces from one device to another to minimize cross-talk (see **Figure 27**).

Figure 27: Clock Traces Spacing



- Do not use 90° angles for bending.
- Include guard traces (ground) to surround the clock signal if possible.
- Place clock routing on an internal layer without stubs.

High-Speed Differential Pair

The following guidelines are recommended for high-speed input and output signal layout:

- For low-swing signals (<300 mV), place the device as close to the driving source as possible (such as the flexible printed circuit or processor) to minimize the cross-talk, impedance mismatch, and differential noise pick-up. Keep the total trace-length <4 inches.
- Traces must always be matched lengths.

- Route the pair as close together as possible for noise rejection.
- Trace impedance must be 100 Ohm ± 10% to produce a 50 Ohm ± 10% pair.
- Signals must not have extra components to maintain signal integrity.

Vias

The following guidelines are recommended for via usage:

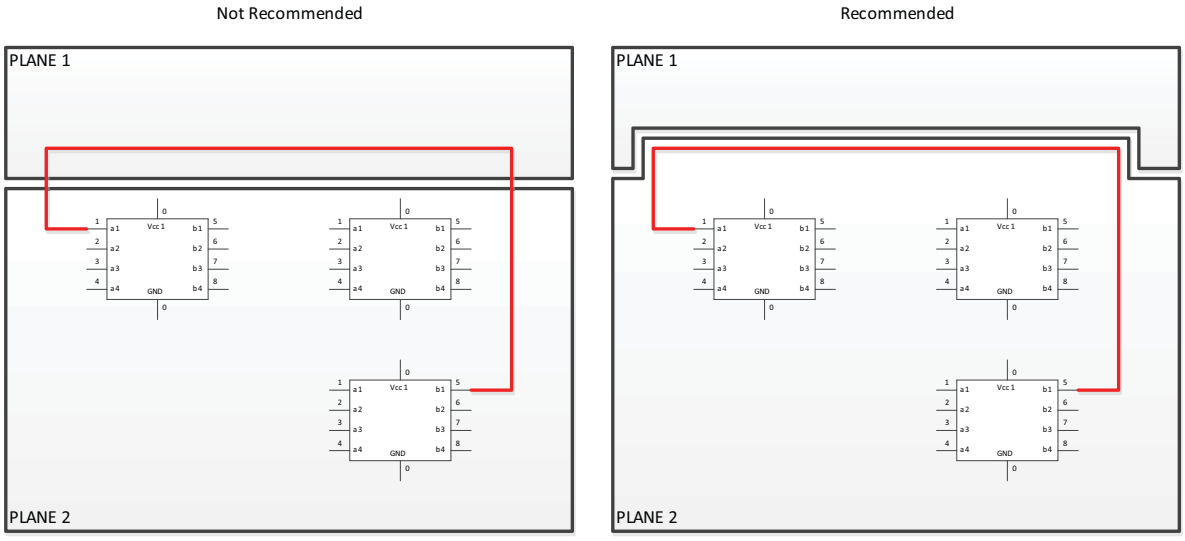
- Increase the clearance around the via to minimize capacitance.
- Minimize the number of vias per signal connection. Each via introduces discontinuities in the signal transmission line and increases the chance to pick up interference from other layers of the PCB.
- Avoid using a through-hole via as a test point if possible.

Isolations

Isolation is referred to as the separation between power and ground planes. The following guidelines are recommended for isolation:

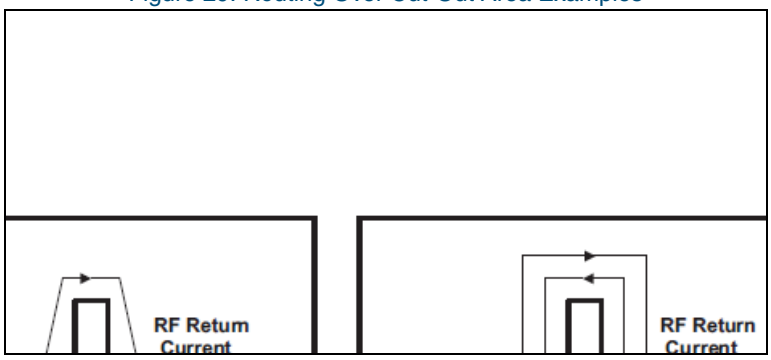
- Isolate between digital and analog power planes.
- Do not route traces across planes (see **Figure 28**). This can cause a broken RF path for the return signal, which can result in severe EMI issues. Route high-speed sensitive signals parallel to solid power or ground planes.

Figure 28: Routing Over Isolation Planes



- Fill unused areas of a layer with copper and connect to ground planes using vias.
- Do not overlap planes between layers. These overlap areas can produce unwanted capacitance that passes RF emissions between the planes.
- Do not route signals over the slot-plane (see **Figure 29**).

Figure 29: Routing Over Cut-Out Area Examples



Electrostatic Discharge (ESD)

The following guidelines are recommended for ESD:

- Provide ESD protection for PCB handling. The typical provision is an ESD strip around the board. The strip must connect to the PCB ground plane.
- Apply ESD protection to all connectors. The ground of the connector body must be connected to the PCB ground plane.

Layout Guidelines Specific to the PolarPro 3

Critical Signals

The following guidelines are recommended for the layout of critical signals:

- Keep the PolarPro 3 reference clock circuits as close to the device as possible.
- Follow the minimum spacing rules for reset lines from adjacent signals on the same and adjacent layers.
- Keep reset lines away from noisy sources (such as long clock traces, high energy signals and fast transition edges signals).
- Keep interrupt lines away from noisy sources (such as long clock traces, high energy signals and fast transition edges signals).

Vias

Use via-in-pad for the layout of vias and device connections.

GPIOs

The following guidelines are recommended for the layout of GPIOs:

- Keep the number of vias as close to minimum (two) as possible.

Power

The following guidelines are recommended for the layout of power:

- Use the power island or plane as much as possible.
- If using a power trace to connect to the PolarPro 3 power pins, make the trace as wide as possible, and follow current requirements to prevent excessive IR drop.
- Since the number of capacitors for the design is at a minimum, place all of the capacitors as close to the power pins as possible.

Reducing the Number of PCB Layers

The cost-reduction requirements common to PCB design and manufacturing requires the PCB designer to look for a solution to produce PCBs at the lowest cost possible. This section discusses areas that a PCB designer needs to consider when using a PolarPro 3 in the system.

There are several factors that contribute to the cost of a bare PCB:

- Volume: the number of PCBs per run.
- PCB size: the smaller, the less costly.
- PCB material: readily available material is less expensive.
- Number of layers: thickness reduction and quicker manufacturing time.
- PCB shapes: odd shape and slots require more processes.
- Copper size and spacing: the dimension of pads and spacing demand better PCB producing equipment.
- Via: current PCB technology is capable to handle more advanced via types: blind, buried, etc. These require more manufacturing time which translates into a more costly PCB.

Work with the PCB manufacturer to understand the trade-offs between PCB cost and these factors before finalizing PCB specifications.

Device Placement

Placement of devices is critical for good flow to nets routing, thus reducing the number of layers required. The placement must follow the flow of data between components. Critical components must be placed first, followed by support components such capacitors. Less critical components are placed last.

Make sure the device orientation is correct. If the device is in the correct location, but with the wrong orientation, the intended result may not be achieved. Always choose the orientation that has the most signals flowing in the same direction. Crossing signals require multiple layers to complete routing.

Via Technology

While advanced via technologies are more expensive that regular thru-hole via, they can be used to improve layers routing. Use blind via and/or buried via for a design that has constraints on PCB size (thus requiring routing of a signal under the PolarPro 3). Using via-in-pad for PolarPro 3 pins that need internal layer connections.

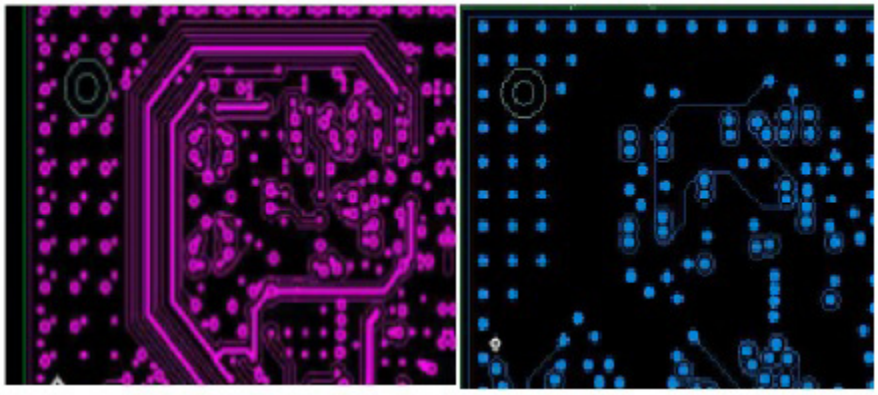
Power and Ground Planes

Dedicated power and ground planes yield the best impedance control and zero IR drop. However, these dedicated planes increases the thickness, and layers count for the PCB.

To reduce the need for a dedicated power plane, use thick traces for power routing. The thickness must meet the current requirements and be as wide as space allows.

To reduce the need for a dedicated ground plane, provide guards around the traces for each layer and fill the rest of the layer with copper (see **Figure 30**). Where possible, provide vias to tie these ground islands on each layer together. While this grounding method is not effective for EMI and trace impedance control, it provides plenty of grounding for the logics.

Figure 30: Fill-In Ground Examples



PCB Size

While increasing the board size can increase the cost of the PCB, this increase can be offset by the reduction of layers. Increasing board size provides additional routing areas and room for parts placement.

Ordering Information

Table 32: Ordering Information

Logic Cells	Ordering Number	Package Type[a]
1,019	CSSP-CDWDN30-xxxx	30-ball WLCSP 2.09 mm x 2.54 mm, 0.4 mm pitch
	CSSP-CDWDN64-xxxx	64-ball VFBGA 3.5 mm x 3.5 mm, 0.4 mm pitch
640	CSSP-CRWDN30-xxxx	30-ball WLCSP 2.09 mm x 2.54 mm, 0.4 mm pitch
	CSSP-CRWDN64-xxxx	64-ball VFBGA 3.5 mm x 3.5 mm, 0.4 mm pitch

a. PolarPro 3 devices are only available in lead-free packaging.

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Revision History

Revision	Date	Originator and Comments
1.0	December 2013	Initial production release.
1.1	May 2014	Paul Karazuba and Kathleen Bylsma Added programmable fabric timing information.
1.2	April 2014	Paul Karazuba and Kathleen Bylsma Added 640 logic cell option and related information.

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