

178ball FBGASpecification

16Gb LPDDR3 (x32)

Document Title

FBGA
16Gb (x32) LPDDR3

Revision History

Revision No.	History	Draft Date	Remark
0.1	- Initial Draft	May. 2019	Preliminary

FEATURES

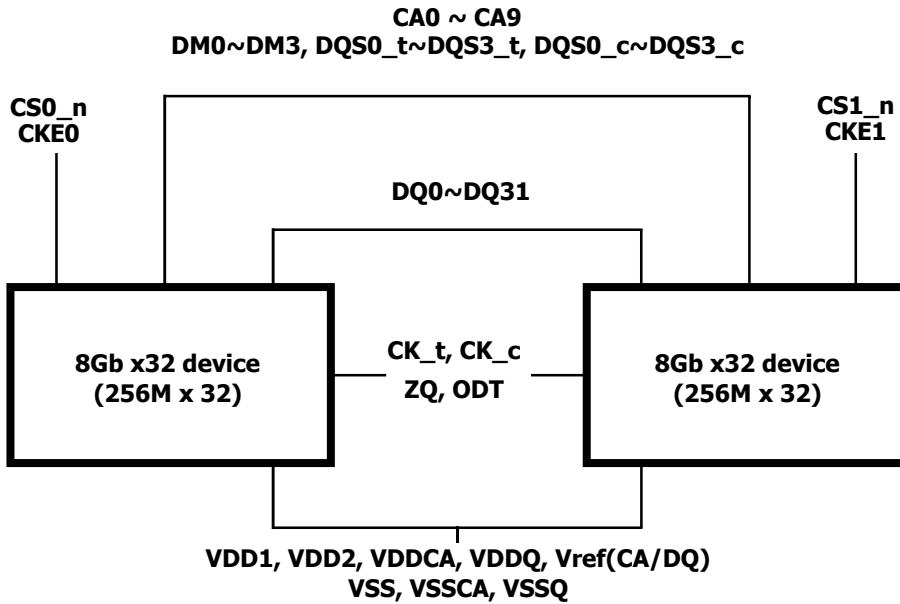
[FBGA]

- Operation Temperature
 - -25°C ~85°C
- Package
 - 178-ball FBGA
 - 11.0x11.5mm², 1.00t, 0.65mm pitch
 - Lead & Halogen Free

[LPDDR3]

- VDD1 = 1.8V (1.7V to 1.95V)
- VDD2, VDDCA and VDDQ = 1.2V (1.14V to 1.30)
- HSUL₁₂ interface (High Speed Unterminated Logic 1.2V)
- Doubled data rate architecture for command, address and data bus;
 - all control and address except CS_n, CKE latched at both rising and falling edge of the clock
 - CS_n, CKE latched at rising edge of the clock
 - two data accesses per clock cycle
- Differential clock inputs (CK_t, CK_c)
- Bi-directional differential data strobe (DQS_t, DQS_c)
 - Source synchronous data transaction aligned to bi-directional differential data strobe (DQS_t, DQS_c)
 - Data outputs aligned to the edge of the data strobe (DQS_t, DQS_c) when READ operation
 - Data inputs aligned to the center of the data strobe (DQS_t, DQS_c) when WRITE operation
- DM masks write data at the both rising and falling edge of the data strobe
- Programmable RL (Read Latency) and WL (Write Latency)
- Programmable burst length: 8
- Auto refresh and self refresh supported
- All bank auto refresh and per bank auto refresh supported
- Auto TCSR (Temperature Compensated Self Refresh)
- PASR (Partial Array Self Refresh) by Bank Mask and Segment Mask
- DS (Drive Strength)
- ZQ (Calibration)
- ODT (On Die Termination)

Functional Block Diagram

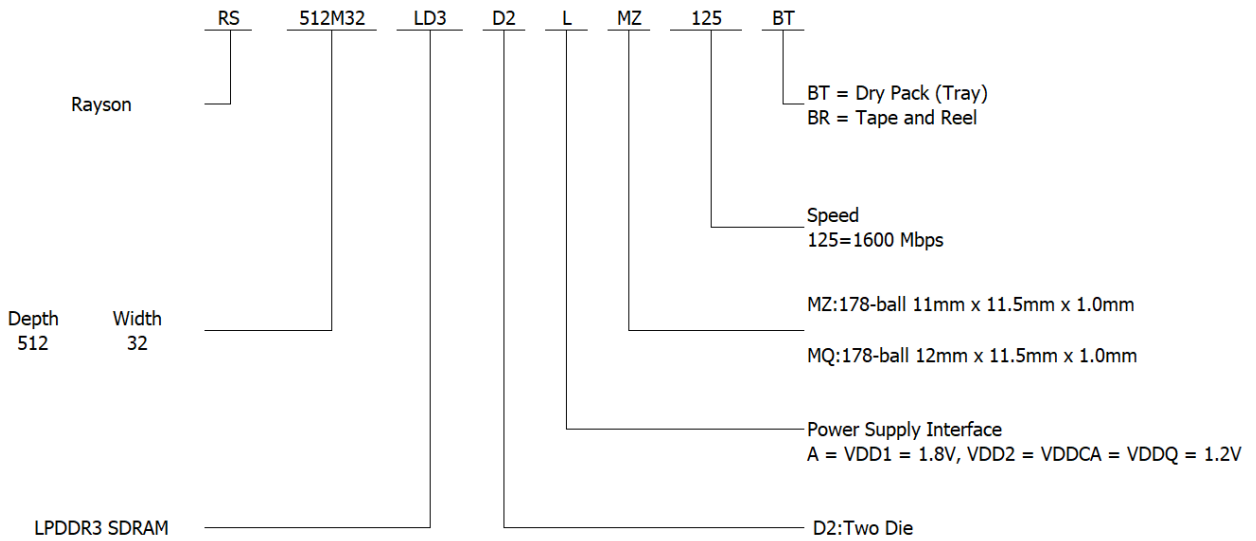


Note

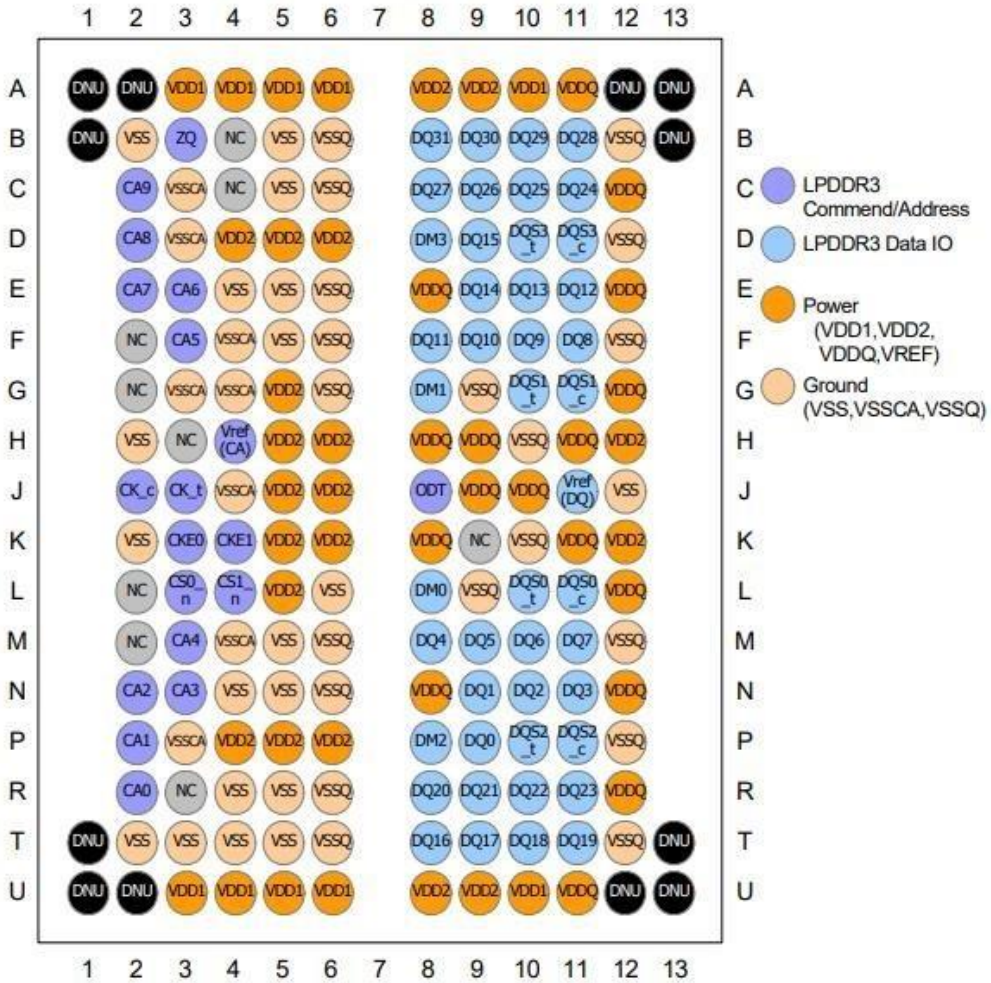
1. Total current consumption is dependent to user operating conditions. AC and DC characteristics shown in this specification are based on a single die. See the section of "DC Parameters and Operating Conditions"

ORDERING INFORMATION

Part Number	Memory Combination	Operation Voltage	Density	Speed	Package
RS512M32LD3D2LMZ-125BT	LPDDR3	1.8V/1.2/1.2/1.2	16Gb(x 32)	DDR3 1600	178Ball FBGA (Lead & Halogen Free)



Ball ASSIGNMENT



Top View

*178ball
x32 LPDDR3*

Note

- 1.1. J8 will be used as "ODT". Users who don't use ODT Function can assign J8 as VSSQ.
2. Inside the chip, VDDCA and VDD2 are tied. F2, G2, H3, L2 and M2 are not connected to the chip. It fully guarantees DRAM operation even there is a VDDCA input voltage.

Pin Description

SYMBOL	DESCRIPTION	Type
CS0	Chip Select	Input
CK_c, CK_t	Differential Clocks	Input
CKE0	Clock Enable	Input
CA0 ~ CA9	Command / Address	Input
DQ0 ~ DQ31	Data I/O	Input/Output
DM0 ~ DM3	Input Data Mask	Input/Output
DQS0_t ~ DQS3_t	Differential Data Strobe (rising edge)	Input/Output
DQS0_c ~ DQS3_c	Differential Data Strobe (falling edge)	Input/Output
ZQ	Drive Strength Calibration	Input/Output
VDD1	Core Power Supply	Power
VDD2	Core Power Supply	Power
VSS	Ground	Ground
VDDQ	I/O Power Supply	Power
VDDCA	CA Power Supply	Power
VSSCA	CA Ground	Ground
VSSQ	I/O Ground	Ground
VREF	Reference Voltage	Power
ODT	On Die Termination Enable	Input

Input/Output Capacitance

Parameter	Symbol	Min	Max	Unit
Input capacitance, CK_t and CK_c	CCK	1.5	3.0	pF
Input capacitance, all other input-only pins	CI	0.5	3.0	pF
Input/output capacitance, DQ, DM, DQS_t, DQS_c	CIO	2.0	3.5	pF
Input/Output Capacitance ZQ	CZQ	1.5	3.0	pF

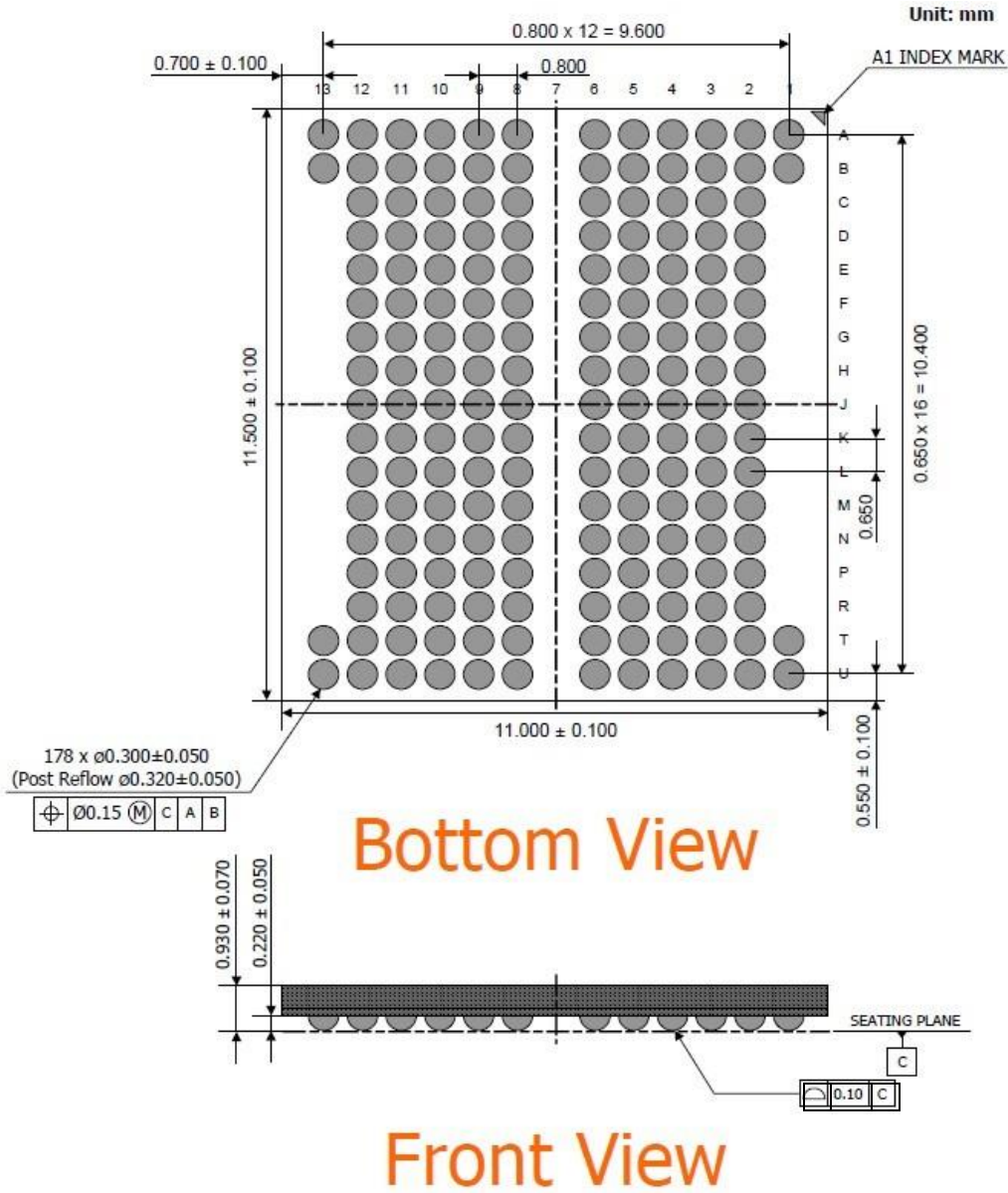
(TOPER; VDDQ = 1.14-1.3V; VDDCA = 1.14-1.3V; VDD1 = 1.7-1.95V, VDD2 = 1.14-1.3V)

Note:

1. This parameter applies to both die and package.
2. This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA) with VDD1, VDD2, VDDQ, VSS, VSSCA, VSSQ applied and all other pins floating).
3. CI applies to CS_n, CKE, CA0-CA9.
4. DM loading matches DQ and DQS.
5. MR3 I/O configuration DS OP3-OP0 = 0001B (34.30ohm typical)
6. Maximum external load capacitance on ZQ pin, including packaging, board, pin, resistor, and other LPDDR3 devices: 5pF.

PACKAGE INFORMATION

178 Ball 0.65mm pitch 11.0mm x 11.5mm [t = 1.00mm max] FBGA



8Gb LPDDR3 SDRAM

Input/Output Functional Description

SYMBOL	TYPE	DESCRIPTION
CK_t, CK_c	Input	Clock: CK_t and CK_c are differential clock inputs. All Double Data Rate (DDR) CA inputs are sampled on both positive and negative edge of CK_t. Single Data Rate (SDR) inputs, CS_n and CKE, are sampled at the positive Clock edge. Clock is defined as the differential pair, CK_t and CK_c. The positive Clock edge is defined by the crosspoint of a rising CK_t and a falling CK_c. The negative Clock edge is defined by the crosspoint of a falling CK_t and a rising CK_c.
CKE	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates internal clock signals and therefore device input buffers and output drivers. Power savings modes are entered and exited through CKE transitions. CKE is considered part of the command code. CKE is sampled at the positive Clock edge.
CS_n	Input	Chip Select: CS_n is considered part of the command code. CS_n is sampled at the positive Clock edge.
CA0 - CA9	Input	DDR Command/Address Inputs: Uni-directional command/address bus inputs. CA is considered part of the command code.
DQ0 - DQ15(x16) DQ0 - DQ31(x32)	I/O	Data Input/Output: Bi-directional data bus
DQS0_t, DQS1_t, DQS0_c, DQS1_c (x16) DQS0_t - DQS3_t, DQS0_c - DQS3_c (x32)	I/O	Data Strobe (Bi-directional, Differential): The data strobe is bi-directional (used for read and write data) and differential (DQS_t and DQS_c). It is output with read data and input with write data. DQS_t is edge-aligned to read data and centered with write data. For x16, DQS0_t and DQS0_c correspond to the data on DQ0 - DQ7; DQS1_t and DQS1_c to the data on DQ8 - DQ15. For x32 DQS0_t and DQS0_c correspond to the data on DQ0 - DQ7, DQS1_t and DQS1_c to the data on DQ8 - DQ15, DQS2_t and DQS2_c to the data on DQ16 - DQ23, DQS3_t and DQS3_c to the data on DQ24 - DQ31.
DM0-DM1 (x16) DM0-DM3 (x32)	Input	Input Data Mask: DM is the input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a write access. DM is sampled on both edges of DQS_t. Although DM is for input only, the DM loadings shall match the DQ and DQS_t (or DQS_c). For x16 and x32 devices, DM0 is the input data mask signal for the data on DQ0-7. DM1 is the input data mask signal for the data on DQ8-15. For x32 devices, DM2 is the input data mask signal for the data on DQ16-23 and DM3 is the input data mask signal for the data on DQ24-31.
ODT	Input	On-Die Termination: This signal enables and disables termination on the DRAM DQ bus according to the specified mode register settings.
VDD1	Supply	Core Power Supply 1
VDD2	Supply	Core Power Supply 2
VDDCA	Supply	Input Receiver Power Supply: Power for CA0-9, CKE, CS_n, CK_t and CK_c input buffers.
VDDQ	Supply	I/O Power Supply: Power supply for data input/output buffers.
VREFCA	Supply	Reference Voltage for CA Command and Control Input Receiver: Reference voltage for all CA0-9, CKE, CS_n, CK_t and CK_c input buffers.
VREFDQ	Supply	Reference Voltage for DQ Input Receiver: Reference voltage for all Data input buffers.
VSS	Supply	Ground
VSSCA	Supply	Ground for Input Receivers
VSSQ	Supply	I/O Ground: Ground for data input/output buffers
ZQ	I/O	Reference Pin for Output Drive Strength Calibration

Functional Description

LPDDR3-SDRAM is a high-speed synchronous DRAM device internally configured as an 8-bank memory.

These devices contain the following number of bits:
8 Gb has 8,589,934,592 bits

LPDDR3 devices use a doubled data rate architecture on the Command/Address (CA) bus to reduce the number of input pins in the system. The 10-bit CA bus contains command, address, and bank information. Each command uses one clock cycle, during which command information is transferred on both the positive and negative edge of the clock. These devices also use a doubled data rate architecture on the DQ pins to achieve high speed operation. The doubled data rate architecture is essentially an 8n prefetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pins. A single read or write access for the LPDDR3 SDRAM effectively consists of a single 8n-bit wide, one clock cycle data transfer at the internal DRAM core and eight corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

Read and write accesses to the LPDDR3 SDRAMs are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an Activate command, which is then followed by a Read or Write command. The address and BA bits registered coincident with the Activate command are used to select the row and the bank to be accessed. The address bits registered coincident with the Read or Write command are used to select the bank and the starting column location for the burst access.

Prior to normal operation, the LPDDR3 SDRAM must be initialized. The following section provides detailed information covering device initialization, register definition, command description and device operation.

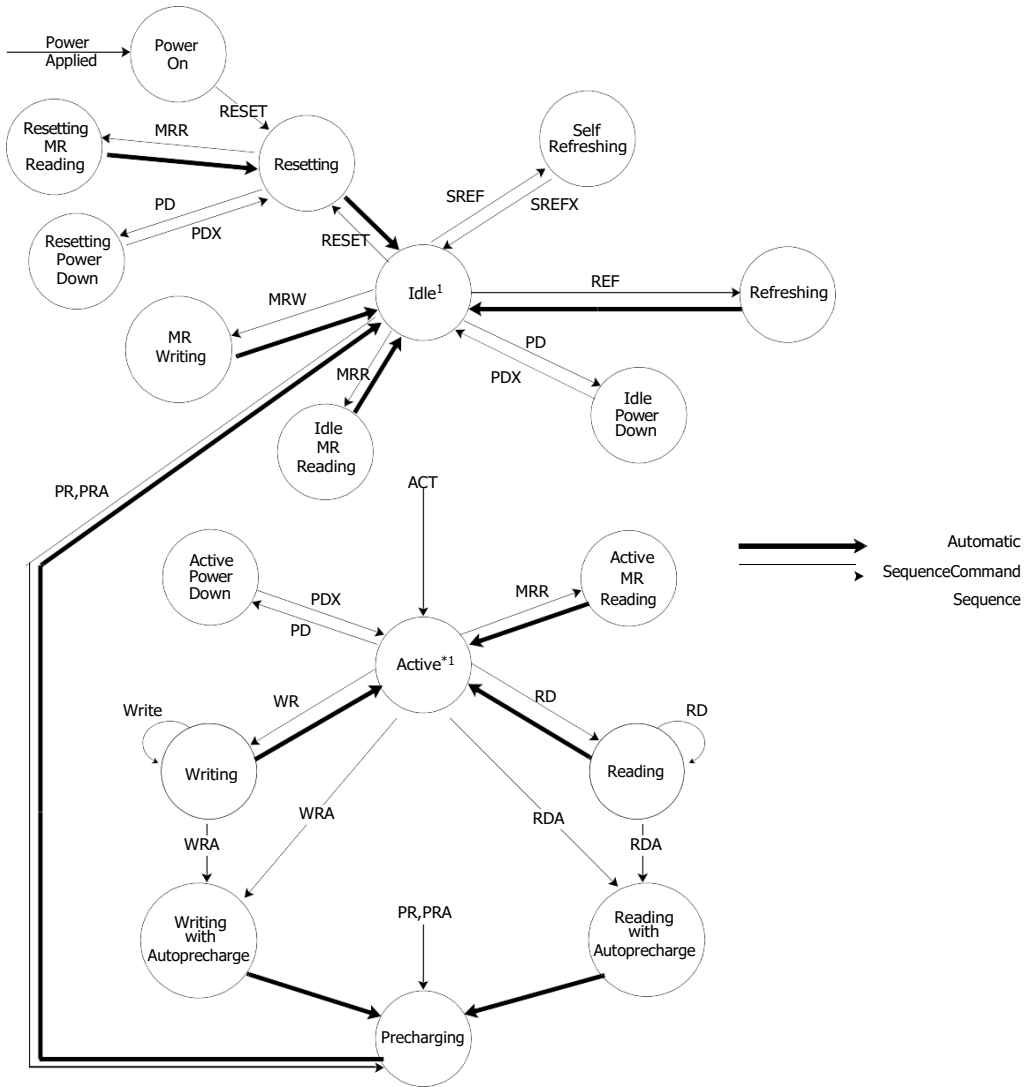
LPDDR3 SDRAM Addressing

Density		8Gb
Number of Banks		8
Bank Addresses		BA0 - BA2
$t_{REFI}(us)^2$		3.9
x16	Row Addresses	R0 - R14
	Column Addresses ¹	C0 - C10
x32	Row Addresses	R0 - R14
	Column Addresses ¹	C0 - C9

Note:

1. The least-significant column address C0 is not transmitted on the CA bus, and is implied to be zero.
2. t_{REFI} values for all bank refresh is $T_c = 0 \sim 85 \text{ }^\circ\text{C}$, T_c means Operating Case Temperature.
3. Row and Column Address values on the CA bus which are not used are "don't care".
4. No memory present at addresses with R13=R14=HIGH. ACT command with R13=R14=HIGH is ignored (NOP). Write to R13=R14=HIGH is ignored (NOP).

STATE DIAGRAM



PR(A) = Precharge (All)
 ACT = Activate
 WR(A) = Write (with Autoprecharge)
 RD(A) = Read (with Autoprecharge)
 RESET=Reset is achieved through MRW command
 MRW=Mode Register Write
 MRR = Mode Register Read

PD = Enter Power Down
 PDX = Exit Power Down
 SREF = Enter Self Refresh
 SREFX = Exit Self Refresh
 REF = Refresh

Note:

1. In the Idle state, all banks are precharged.
2. In the case of MRW to enter CA Training mode or Write Leveling Mode, the state machine will not automatically return to the Idle state. In these cases an additional MRW command is required to exit either operating mode and return to the Idle state. See sections "CA Training" or "Write Leveling".
3. Terminated bursts are not allowed. For these state transitions, the burst operation must be completed before the transition can occur.
4. Use caution with this diagram. It is intended to provide a floorplan of the possible state transitions and commands to control them, not all details. In particular, situations involving more than one bank are not captured in full detail.

Power-up, Initialization and Power-off

Voltage Ramp and Device Initialization

The following sequence must be used to power up the device. Unless specified otherwise, this procedure is mandatory.

1. Voltage Ramp

While applying power (after T_a), CKEmust be held LOW ($\leq 0.2 \times VDDCA$), and all other inputs must be between VIL_{min} and VIH_{max} . The device outputs remain at High-Z while CKE is held LOW.

Following the completion of the voltage ramp (T_b), CKEmust be maintained LOW. DQ, DM, DQS_tand DQS_c voltage levels must be between VSSQ and VDDQ during voltage ramp to avoid latch-up. CK_t, CK_c, CS_n, and CA input levels must be between VSSCA and VDDCA during voltage ramp to avoid latch-up. Voltage ramp power supply requirements are provided in the table "Voltage Ramp Conditions".

After...	Applicable Conditions
Ta is reached	VDD1 must be greater than VDD2-200mV.
	VDD1 and VDD2 must be greater than VDDCA-200mV.
	VDD1 and VDD2 must be greater than VDDQ-200mV.
	VREF must always be less than all other supply voltages.

Note:

1. T_a is the point when any power supply first reaches 300mV.
2. Noted conditions apply between T_a and power-off (controlled or uncontrolled).
3. T_b is the point at which all supply and reference voltages are within their defined operating ranges.
4. Power ramp duration t_{INIT0} ($T_b - T_a$) must not exceed 20ms.
5. The voltage difference between any of VSS, VSSQ, and VSSCA pins must not exceed 100mV.

Beginning at T_b , CKEmust remain LOW for at least t_{INIT1} , after which CKE can be asserted HIGH. The clock must be stable at least t_{INIT2} prior to the first CKELow-to-HIGH transition (T_c). CKE, CS_n, and CA inputs must observe setup and hold requirements (t_{IS} , t_{IH}) with respect to the first rising clock edge (as well as to subsequent falling and rising edges). If any MRW commands are issued, the clock period must be within the range defined for CKb. MRW commands can be issued at normal clock frequencies as long as all AC timings are met. Some AC parameters (for example, t_{DQSCK}) could have relaxed timings (such as t_{DQSCKb}) before the system is appropriately configured. While keeping CKE HIGH, NOP commands must be issued for at least t_{INIT3} (T_d). The ODT input signal may be in undefined state until IS before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal shall be statically held at either LOW or HIGH. The ODT input signal remains static until the power up initialization sequence is finished, including the expiration of t_{ZQINIT} .

2. Reset Command

After t_{INIT3} is satisfied, the MRW RESET command must be issued (T_d).

An optional PRECHARGE ALL command can be issued prior to the MRW RESET command. Wait at least t_{INIT4} while keeping CKE asserted and issuing NOP commands. Only NOP commands are allowed during t_{INIT4} .

3. MRRs and Device Auto Initialization (DAI) Polling

After t_{INIT4} is satisfied (T_e), only MRR commands and power-down entry/exit commands are supported. After T_e , CKE can go LOW in alignment with power-down entry and exit specifications. MRR commands are only valid at this time if the CA bus does not need to be trained. may only begin after time T_f . User may issue MRR command to poll the DAI bit which will indicate if device auto initialization is complete; once DAI bit indicates completion, SDRAM is in idle state. Device will also be in idle state after t_{INIT5} (max) has expired (whether or not DAI bit has been read by MRR command). As the memory output buffers are not properly configured by T_e , some AC parameters must have relaxed timings before the system is appropriately configured.

4. ZQ Calibration

If CA Training is not required, the MRW initialization calibration (ZQ_CAL) command can be issued to the memory

(MR10) after time T_f . If CA Training is required, the CA Training may begin at time T_f . See the section of "Mode Register Write - CA Training Mode" for the CA Training command. No other CA commands (other than RESET or NOP) may be issued prior to the completion of CA Training. At the completion of CA Training (T_f), the MRW initialization calibration (ZQ_CAL) command can be issued to the memory (MR10).

This command is used to calibrate output impedance over process, voltage, and temperature. In systems where more than one LPDDR3 device exists on the same bus, the controller must not overlap MRW ZQ_CAL commands. The device is ready for normal operation after t_{ZQINIT} .

5. Normal Operation

After t_{ZQINIT} (T_g), MRW commands must be used to properly configure the memory (for example the output buffer drive strength, latencies, etc.). Specifically, MR1, MR2, and MR3 must be set to configure the memory for the target frequency and memory configuration.

After the initialization sequence is complete, the device is ready for any valid command. After T_g , the clock frequency can be changed using the procedure described in the LPDDR3 specification.

Table. Timing Parameters for initialization

Symbol	Parameter	Value		Unit
		min	max	
t_{INIT0}	Maximum Voltage Ramp Time	-	20	ms
t_{INIT1}	Minimum CKE low time after completion of voltage ramp	100	-	ns
t_{INIT2}	Minimum stable clock before first CKE high	5	-	tCK
t_{INIT3}	Minimum idle time after first CKE assertion	200	-	us
t_{INIT4}	Minimum idle time after Reset command	1	-	us
t_{INIT5}	Maximum duration of Device Auto-Initialization	-	10	us
t_{ZQINIT}	ZQ Initial Calibration for LPDDR3 devices	1	-	us
tCKb	Clock cycle time during boot	18	100	ns

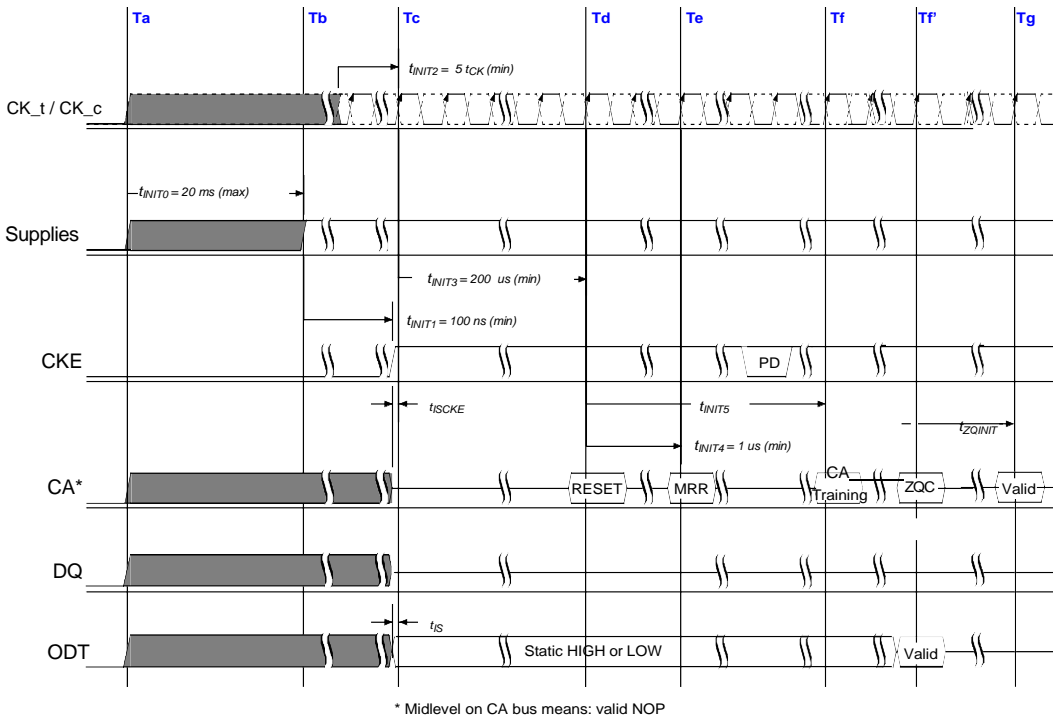


Figure. Power Ramp and Initialization Sequence

Notes

1. High-Z on the CA bus indicates NOP.
2. For tINIT values, see the table "Timing Parameters for Initialization".
3. After RESET command (time Te), RTT is disabled until ODT function is enabled by MRW to MR11 following Tg.
4. CA Training is optional.

Initialization After Reset (without Power ramp)

If the RESET command is issued before or after the power-up initialization sequence, there-initialization procedure must begin at Td.

Power-off Sequence

The following procedure is required to power off the device.

While powering off, CKE must be held LOW ($\leq 0.2 \times VDDCA$); all other inputs must be between VIL_{min} and VIH_{max} . The device outputs remain at High-Z while CKE is held LOW.

DQ, DM, DQS_t, and DQS_cv voltage levels must be between $VSSQ$ and $VDDQ$ during the power-off sequence to avoid latch-up. CK_t, CK_c, CS_n, and CA input levels must be between $VSSCA$ and $VDDCA$ during the power-off sequence to avoid latch-up.

Tx is the point where any power supply drops below the minimum value specified.

Tz is the point where all power supplies are below 300mV. After Tz, the device is powered off (see the table "Power Supply Conditions").

Table. Power Supply Conditions

Between...	Applicable Conditions
Tx and Tz	VDD1 must be greater than $VDD2 - 200mV$
	VDD1 must be greater than $VDDCA - 200mV$
	VDD1 must be greater than $VDDQ - 200mV$
	VREF must always be less than all other supply voltages

The voltage difference between any of VSS, VSSQ, and VSSCA pins must not exceed 100mV.

Uncontrolled Power-Off Sequence

When an uncontrolled power-off occurs, the following conditions must be met:

At Tx, when the power supply drops below the minimum values specified, all power supplies must be turned off and all power-supply current capacity must be at zero, except for any static charge remaining in the system.

After Tz (the point at which all power supplies first reach 300mV), the device must power off. The time between Tx and Tz must not exceed 10ms. During this period, the relative voltage between power supplies is uncontrolled. $VDD1$ and $VDD2$ must decrease with a slope lower than $0.5V/\mu s$ between Tx and Tz.

An uncontrolled power-off sequence can occur a maximum of 400 times over the life of the device.

Table. Power-Off Timing

Symbol	Parameter	Value		Unit
		min	max	
tPOFF	Maximum power-off ramp time	-	2	sec

Mode Register Definition

Table below shows the mode registers for LPDDR3 SDRAM. Each register is denoted as "R" if it can be read but not written, "W" if it can be written but not read, and "R/W" if it can be read and written. A Mode Register Read command shall be used to read a mode register. A Mode Register Write command shall be used to write a mode register.

Table. Mode Register Assignment

MR #	MA <7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	Link
0	00H	Device Info.	R	RL3	WL setB	(RFU)	RZQI (Optional)	(RFU)		DAI		go to MR0
1	01H	Device Feature 1	W	nWR (for AP)			(RFU)	BT	BL			go to MR1
2	02H	Device Feature 2	W	WR Lev	WL Select	(RFU)	nWRE	RL & WL				go to MR2
3	03H	I/O Config-1	W	(RFU)			DS				go to MR3	
4	04H	Device Temperature	R	TUF	(RFU)			Refresh Rate			go to MR4	
5	05H	Basic Config-1	R	Manufacturer ID								go to MR5
6	06H	Basic Config-2	R	Revision ID1								go to MR6
7	07H	Basic Config-3	R	Revision ID2								go to MR7
8	08H	Basic Config-4	R	I/O width		Density			Type			go to MR8
9	09H	Test Mode	W	Vendor-Specific Test Mode								go to MR9
10	0AH	Calibration	W	Calibration Code								go to MR10
11	0BH	ODT	W	(RFU)				PD CTL	DQ ODT			go to MR11
16	10H	PASR_Bank	W	PASR Bank Mask								go to MR16
17	11H	PASR_Segment	W	PASR Segment Mask								go to MR17
32	20H	DQ Calibration Pattern A	R	See the section "DQ Calibration"								go to MR32
40	28H	DQ Calibration Pattern B	R	See the section "DQ Calibration"								go to MR40
41	29H	CA Training Entry for CA0-3, CA5-8	W	See the section "Mode Register Write - CA Training Mode"								go to MR41
42	2AH	CA Training Exit	W	See the section "Mode Register Write - CA Training Mode"								go to MR42
48	30H	CA Training Entry for CA4, 9	W	See the section "Mode Register Write - CA Training Mode"								go to MR48
63	3FH	Reset	W	X								go to MR63

Note:

1. RFU bits shall be set to '0' during Mode Register writes.
2. RFU bits shall be read as '0' during Mode Register reads.
3. All Mode Registers that are specified as RFU or write-only shall return undefined data when read and DQS_t, DQS_c shall be toggled.
4. All Mode Registers that are specified as RFU shall not be written.
5. Write to read-only registers shall have no impact on the functionality of the device.

MRO Device Information (MA<7:0> = 00H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RL3	WL (Set B) Support	(RFU)	RZQI (Optional)		(RFU)		DAI
DAI (Device Auto-Initialization Status)			Read-only	OP0	0B: DAI complete 1B: DAI still in progress		
RZQI (Built in Self Test for RZQ Information)			Read-only	OP4:OP3	00B: RZQ self test not supported 01B: ZQ-pin may connect to VDDCA or float 10B: ZQ-pin may short to GND 11B: ZQ-pin self test completed, no error condition detected (ZQ-pin may not connect to VDD or float nor short to GND)		
WL (Set B) Support			Read-only	OP<6>	0B: DRAM does not support WL (Set B) 1B: DRAM supports WL (Set B)		
RL3 Option Support			Read-only	OP<7>	0B : DRAM does not support RL=3, nWR=3, WL=1 1B : DRAM supports RL=3, nWR=3, WL=1 for frequencies <=166		

Note:

1. RZQI, if supported, will be set upon completion of the MRW ZQ Initialization Calibration command.
2. If ZQ is connected to VDDCA to set default calibration, OP[4:3] shall be set to 01. If ZQ is not connected to VDDCA, either OP[4:3]=01 or OP[4:3]=10 might indicate a ZQ-pin assembly error. It is recommended that the assembly error is corrected.
3. In the case of possible assembly error (either OP[4:3]=01 or OP[4:3]=10 per Note 4), the LPDDR3 device will default to factory trim settings for RON, and will ignore ZQ calibration commands. In either case, the system may not function as intended.
4. In the case of the ZQ self-test returning a value of 11b, this result indicates that the device has detected a resistor connection to the ZQ pin. However, this result cannot be used to validate the ZQ resistor value or that the ZQ resistor tolerance meets the specified limits (i.e. 240-ohm +/-1%).

MR1 Device Feature 1 (MA<7:0> = 01H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
nWR (for AP)			(RFU)	BT	BL		
BL		Write-only	OP<2:0>	011B: BL8 (default)			
				100B: Reserved			
				All others: reserved			
BT		Write-only	OP<3>	0B: Don't care			
nWR		Write-only	OP<7:5>	If nWRE (in MR2 OP4) = 0			
				001B : nWR=3 (optional)			
				100B : nWR=6			
				110B : nWR=8			
				111B : nWR=9			
				If nWRE (in MR2 OP4) = 1			
				000B : nWR=10 (default)			
				001B : nWR=11			
				010B : nWR=12			
				100B : nWR=14			
110B : nWR=16							
All others: reserved							

Note:

1. Programmed value in nWR register is the number of clock cycles which determines when to start internal precharge operation for a write burst with AP enabled. It is determined by RU(tWR/tCK).

Table. Burst Sequence by BL and BT

C2	C1	C0	BT	BL	Burst Cycle Number and Burst Address Sequence							
					1	2	3	4	5	6	7	8
0B	0B	0B	seq	8	0	1	2	3	4	5	6	7
0B	1B	0B			2	3	4	5	6	7	0	1
1B	0B	0B			4	5	6	7	0	1	2	3
1B	1B	0B			6	7	0	1	2	3	4	5

Note:

1. C0 inputs are not present on CA bus. Those are implied zero.
2. For BL=8, the burst address represents C2 -C0.

MR2 Device Feature 2 (MA<7:0> = 02H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
WR Lev	WL Select	(RFU)	nWRE	RL & WL			
RL & WL		Write-only	OP<3:0>	If OP<6> =0 (WL Set A, default) 0001B: RL = 3 / WL = 1 (≤ 166 MHz, optional ¹) 0100B: RL = 6 / WL = 3 (≤ 400MHz) 0110B: RL = 8 / WL = 4 (≤ 533MHz) 0111B: RL = 9 / WL = 5 (≤ 600MHz) 1000B: RL = 10 / WL = 6 (≤ 667 MHz, default) 1001B: RL = 11 / WL = 6 (≤ 733MHz) 1010B: RL = 12 / WL = 6 (≤ 800MHz) 1100B: RL = 14 / WL = 8 (≤ 933MHz) 1110B: RL = 16 / WL = 8 (≤ 1066 MHz) All others: reserved If OP<6> =1 (WL Set B, optional ²) 0001B: RL = 3 / WL = 1 (≤ 166 MHz, optional ¹) 0100B: RL = 6 / WL = 3 (≤ 400MHz) 0110B: RL = 8 / WL = 4 (≤ 533MHz) 0111B: RL = 9 / WL = 5 (≤ 600MHz) 1000B: RL = 10 / WL = 8 (≤ 667 MHz, default) 1001B: RL = 11 / WL = 9 (≤ 733MHz) 1010B: RL = 12 / WL = 9 (≤ 800MHz) 1100B: RL = 14 / WL = 11 (≤ 933MHz) 1110B: RL = 16 / WL = 13 (≤ 1066MHz) All others: reserved			
nWRE		Write-only	OP<4>	0B : Enable nWR programing ≤ 9 1B : Enable nWR programing > 9 (default)			
WL Select		Write-only	OP<6>	0B : Select WL Set A (default) 1B : Select WL Set B (optional ²)			
Write Leveling		Write-only	OP<7>	0B : Disabled (default) 1B : Enabled			

Note:

1. See MR0,OP<7>.
2. See MR0,OP<6>

MR3 I/O Configuration 1 (MA<7:0> = 03H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)				DS			
DS	Write-only	OP<3:0>	0000B: reserved				
			0001B: 34.3Ωtypical pull-down/pull-up				
			0010B: 40Ωtypical pull-down/pull-up (default)				
			0011B: 48Ωtypical pull-down/pull-up				
			0100B: reserved for 60Ωtypical pull-down/pull-up				
			0110B: reserved for 80Ωtypical pull-down/pull-up				
			1001B: 34.3Ωtypical pull-down, 40ΩTypical Pull-up (optional ¹)				
			1010B: 40Ωtypical pull-down, 48ΩTypical Pull-up (optional ¹)				
			1011B: 34.3Ωtypical pull-down, 48ΩTypical Pull-up (optional ¹)				
			All others: reserved				

Note:

1. Please contact us, for the supportability of the optionalfeature.

MR4 Device Temperature (MA<7:0> = 04H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
TUF	(RFU)			Refresh Rate			
Refresh Rate	Read-only	OP<2:0>	000B: Low temperature operating limit exceeded				
			001B: 4 x tREFI, 4 x tREFIpb, 4 x tREFW				
			010B: 2 x tREFI, 2 x tREFIpb, 2 x tREFW				
			011B: 1 x tREFI, 1 x tREFIpb, 1 x tREFW ($\leq 85^{\circ}\text{C}$)				
			100B: 1/2 x tREFI, 1/2 x tREFIpb, 1/2 x tREFW, do not de-rate AC timing				
			101B: 1/4 x tREFI, 1/4 x tREFIpb, 1/4 x tREFW, do not de-rate AC timing				
			110B: 1/4 x tREFI, 1/4 x tREFIpb, 1/4 x tREFW, de-rate AC timing				
Temperature Update Flag (TUF)	Read-only	OP<7>	0B: OP<2:0> value has not changed since last read of MR4				
			1B: OP<2:0> value has changed since last read of MR4				

Note:

1. A Mode Register Read from MR4 will reset OP7 to '0'.
2. OP7 is reset to '0' at power-up.
3. If OP2 equals '1', the device temperature is greater than 85°C.
4. OP7 is set to '1' if OP2:OP0 has changed at any time since the last read of MR4.
5. LPDDR3 might not operate properly when OP[2:0]=000B or 111B.
6. For specified operating temperature range and maximum operating temperature refer to the section of Operating Temperature Range.
7. LPDDR3 devices shall be de-rated by adding derating values to the following core timing parameters: tRCD, tRC, tRAS, tRP and tRRD. tDQCK shall be de-rated according to the tDQCK de-rating in "AC timing table". Prevailing clock frequency spec and related setup and hold timings shall remain unchanged.
8. See the section of Temperature Sensor for information on the recommended frequency of reading MR4.

MR5BasicConfiguration1(MA<7:0>=05H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Manufacturer ID							
Company ID	Read-only	OP<7:0>	0000 0110B: Hynix Semiconductor				

MR6BasicConfiguration2(MA<7:0>=06H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID 1							
Revision ID1	Read-only	OP<7:0>	00000011B				

MR7BasicConfiguration3(MA<7:0>=07H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID 2							
Revision ID2	Read-only	OP<7:0>	00000000B: A-version				

MR8BasicConfiguration4(MA<7:0>=08H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
I/O width		Density				Type	
Type	Read-only	OP<1:0>	11B: S8 All Others : Reserved				
Density	Read-only	OP<5:2>	0110B : 4Gb 0111B : 8Gb 1000B : 16Gb All Others : Reserved				
I/O width	Read-only	OP<7:6>	00B: x32 01B: x16 All Others : Reserved				

MR9 Test Mode (MA<7:0> = 09H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Vendor-specific Test Mode							

MR10 Calibration (MA<7:0> = 0AH)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Calibration Code							
Calibration Code	Write Only	OP<7:0>	1111 1111B: Calibration command after initialization				
			1010 1011B: Long Calibration				
			0101 0110B: Short Calibration				
			1100 0011B: ZQ Reset				
			others: reserved				

Note:

- Host processor shall not write MR10 with "Reserved" values
- LPDDR3 devices shall ignore calibration command when a "Reserved" value is written into MR10.
- See AC timing table for the calibration latency.
- If ZQ is connected to VSSCA through RZQ, either the ZQ calibration function (see "Mode Register Write ZQ Calibration Command") or default calibration (through the ZQRESET command) is supported. If ZQ is connected to VDDCA, the device operates with default calibration, and ZQ calibration commands are ignored. In both cases, the ZQ connection shall not change after power is applied to the device.
- LPDDR3 devices that do not support calibration shall ignore the ZQ Calibration command.
- Optionally, the MRW ZQ Initialization Calibration command will update MR0 to indicate RZQ pin connection.

MR11 ODT (MA<7:0> = 0BH)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)					PD Control	DQ ODT	
DQ ODT	Write Only	OP<1:0>	00B : Disable (Default)				
			01B : RZQ/4 (See the Note 1.)				
			10B : RZQ/2				
			11B : RZQ/1				
Power Down Control	Write Only	OP<2>	0B : ODT disabled by DRAM during power down				
			1B : ODT enabled by DRAM during power down				

Note:

- RZQ/4 shall be supported for LPDDR3-1866 devices. RZQ/4 support is optional for LPDDR3-1333 and LPDDR3-1600 devices. Consult manufacturer specifications for RZQ/4 support for LPDDR3-1333 and LPDDR3-1600.

MR12:15 (Reserved) (MA<7:0> = 0CH - 0FH)

MR16 PASR Bank Mask (MA<7:0> = 10H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Bank Mask							

Bank <7:0> Mask	Write-only	OP<7:0>	0B : refresh enable to the bank (=unmasked, default) 1B : refresh blocked (=masked)
-----------------	------------	---------	--

OP	Bank Mask	LPDDR3 SDRAM
0	XXXXXXX1	Bank 0
1	XXXXXX1X	Bank 1
2	XXXXX1XX	Bank 2
3	XXXX1XXX	Bank 3
4	XXX1XXXX	Bank 4
5	XX1XXXXX	Bank 5
6	X1XXXXXX	Bank 6
7	1XXXXXXX	Bank 7

MR17 PASR Segment Mask (MA<7:0> = 11H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Segment Mask							

Segment <7:0> Mask	Write-only	OP<7:0>	0B : refresh enable to the segment (=unmasked, default) 1B : refresh blocked (=masked)
--------------------	------------	---------	---

Segment	OP	Segment Mask	4Gb R13:11	6Gb ² R14:12	8Gb R14:12	12Gb ² R14:12	16Gb R14:12
0	0	XXXXXXX1	000B				
1	1	XXXXXX1X	001B				
2	2	XXXXX1XX	010B				
3	3	XXXX1XXX	011B				
4	4	XXX1XXXX	100B				
5	5	XX1XXXXX	101B				
6	6	X1XXXXXX	110B				
7	7	1XXXXXXX	111B				

Note:

1. This table indicates the range of row addresses in each masked segment. X is do not care for a particular segment.

MR18:31 (Reserved) (MA<7:0> = 12H - 1FH)

MR32 DQ Calibration Pattern A (MA<7:0> = 20H): MRR only

Reads to MR32 return DQ Calibration Pattern A. See the section of DQ Calibration.

MR33:39 (Reserved) (MA<7:0> = 21H - 27H)

MR40 DQ Calibration Pattern B (MA<7:0> = 28H): MRR only

Reads to MR40 return DQ Calibration Pattern B. See the section of DQ Calibration.

MR41 CA Calibration Mode Entry for CA0-3, CA5-8 (MA<7:0> = 29H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
A4							

See the section of CA Calibration.

MR42 CA Calibration Mode Exit (MA<7:0> = 2AH)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
A8							

See the section of CA Calibration.

MR43:47 (Reserved) (MA<7:0> = 2BH - 2FH)

MR48 CA Calibration Mode Entry for CA4, 9 (MA<7:0> = 30H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
C0							

See the section of CA Calibration.

MR49:62 (Reserved) (MA<7:0> = 31H - 3EH)

MR63 Reset (MA<7:0> = 3FH): MRW only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
X or 0xFC							

Note: For additional information on MRW RESET, see Mode Register Write Command section.

TRUTH TABLES

Operation timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the LPDDR3 device must be powered down and then restarted through the specified initialization sequence before normal operation can continue.

COMMAND TRUTH TABLE

Command	SDR Command Pins (2)		DDR CA Pins (10)										CK_t edge	
	CKE		CS_n	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8		CA9
	CK_t(n-1)	CK_t(n)												
MRW	H	H	L	L	L	L	L	MA0	MA1	MA2	MA3	MA4	MA5	rising
			X	MA6	MA7	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	falling
MRR	H	H	L	L	L	L	H	MA0	MA1	MA2	MA3	MA4	MA5	rising
			X	MA6	MA7	X								
Refresh (per bank)	H	H	L	L	L	H	L	X					rising	
			X	X										falling
Refresh (all bank)	H	H	L	L	L	H	H	X					rising	
			X	X										falling
Enter Self Refresh	H	L	L	L	L	H	X					rising		
			X	X										falling
Active (bank)	H	H	L	L	H	R8	R9	R10	R11	R12	BA0	BA1	BA2	rising
			X	R0	R1	R2	R3	R4	R5	R6	R7	R13	R14	falling
Write (bank)	H	H	L	H	L	L	RFU	RFU	C1	C2	BA0	BA1	BA2	rising
			X	AP ³	C3	C4	C5	C6	C7	C8	C9	C10	C11	falling
Read (bank)	H	H	L	H	L	H	RFU	RFU	C1	C2	BA0	BA1	BA2	rising
			X	AP ³	C3	C4	C5	C6	C7	C8	C9	C10	C11	falling
Precharge (perbank, all bank) ¹¹	H	H	L	H	H	L	H	AB	X	X	BA0	BA1	BA2	rising
			X	X	X	X	X	X	X	X	X	X	X	falling
NOP	H	H	L	H	H	H	X					rising		
			X	X										falling
Maintain SREF, PD (NOP) ⁴	L	L	X	H	H	H	X					rising		
			X	X										falling
NOP	H	H	H	X					rising					
			X	X					falling					
Maintain PD, SREF (NOP) ⁴	L	L	X	X					rising					
			X	X					falling					
Enter Power Down	H	L	H	X					rising					
			X	X					falling					
Exit PD, SREF	L	H	H	X					rising					
			X	X					falling					

Note:

- All LPDDR3 commands are defined by states of CS_n, CA0, CA1, CA2, CA3, and CKE at the rising edge of the clock.
- Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated upon.
- AP³ "high" during a READ or WRITE command indicates that an auto-precharge will occur to the bank associated with the READ or WRITE command.
- "X" means "H or L (but a defined logic level)", except when the LPDDR3 SDRAM is in PD, or SREF, in which case CS_n, CK_t/CK_c, and CA can be floated after the required tCPDED time is satisfied, and until the required exit procedure is initiated as described in the respective entry/exit procedure.
- Self refresh exit is asynchronous.
- VREF must be between 0 and VDDQ during Self Refresh operation.
- CAx refers to command/address bit "x" on the rising edge of clock.
- CAXf refers to command/address bit "x" on the falling edge of clock.
- CS_n and CKE are sampled at the rising edge of clock.
- The least-significant column address C0 is not transmitted on the CA bus, and is implied to be zero.
- AB³ "high" during Precharge command indicates that all bank Precharge will occur. In this case, Bank Address is do-not-care.
- When CS_n is HIGH, LPDDR3 CA bus can be floated.

CKE TRUTH TABLE

Current State ³	CKE _{n-1} ⁴	CKE _n ⁴	CS _n ⁵	Command n ⁶	Operationn ⁶	Next State	Notes
Active Power Down	L	L	X	X	Maintain Active Power Down	Active Power Down	
	L	H	H	NOP	Exit Active Power Down	Active	7
Idle Power Down	L	L	X	X	Maintain Idle Power Down	Idle Power Down	
	L	H	H	NOP	Exit Idle Power Down	Idle	7
Resetting Power Down	L	L	X	X	Maintain Resetting Power Down	Resetting Power Down	
	L	H	H	NOP	Exit Resetting Power Down	Idle or Resetting	7,9
Self Refresh	L	L	X	X	Maintain Self Refresh	Self Refresh	
	L	H	H	NOP	Exit Self Refresh	Idle	8
Bank(s) Active	H	L	H	NOP	Enter Active Power Down	Active Power-Down	
All Banks Idle	H	L	H	NOP	Enter Idle Power Down	Idle Power Down	11
	H	L	L	Enter Self Refresh	Enter Self Refresh	Self Refresh	
Resetting	H	L	H	NOP	Enter Resetting Power Down	Resetting Power Down	
	H	H	Refer to the Command Truth Table				

Note:

- All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
- 'X' means 'Don'tcare'.
- "Currentstate" is the state of the LPDDR3 device immediately prior to clocked edge n.
- "CKEn" is the logic state of CKE at clock rising edge n; "CKEn-1" was the state of CKE at the previous clock edge.
- "CS_n" is the logic state of CS_n at the clock rising edge n.
- "Commandn" is the command registered at clock edge n, and "Operationn" is a result of "Commandn".
- PowerDown exit time (tXP) should elapse before a command other than NOP is issued. The clock must toggle at least twice during the tXP period.
- Self-Refresh exit time (tXSR) should elapse before a command other than NOP is issued. The clock must toggle at least twice during the tXSR time.
- Upon exiting Resetting Power Down, the device will return to the Idle state if tINIT5 has expired.
- In the case of ODT disabled, all DQ output shall be Hi-Z. In the case of ODT enabled, all DQ shall be terminated to VDDQ.

Current State Bank n - Command to Bank n

Current State	Command	Operation	Next State	Note
Any	NOP	Continue previous operation	Current State	
Idle	Activate	Select and activate row	Active	
	Refresh (Per Bank)	Begin to refresh	Refreshing (Per Bank)	6
	Refresh (All Bank)	Begin to refresh	Refreshing (All Bank)	7
	MRW	Write value to Mode Register	MR Writing	7
	MRR	Read value from Mode Register	Idle MR Reading	
	Reset	Begin Device Auto-Initialization	Resetting	8
	Precharge	Deactive row in bank or banks	Precharging	9, 12
Row Active	Read	Select Column, and start read burst	Reading	
	Write	Select Column, and start write burst	Writing	
	MRR	Read value from Mode Register	Active MR Reading	
	Precharge	Deactivate row in bank or banks	Precharging	9
Reading	Read	Select column, and start new read burst	Reading	10,11
	Write	Select column, and start write burst	Writing	10,11,13
Writing	Write	Select Column, and start new write burst	Writing	10,11
	Read	Select column, and start read burst	Reading	10,11,14
Power On	Reset	Begin Device Auto-Initialization	Resetting	7, 9
Resetting	MRR	Read value from Mode Register	Resetting MR Reading	

Note:

1. The table applies when both CKE_{n-1} and CKE_n are HIGH, and after XSR or XPh has been met if the previous state was Power Down.

2. All states and sequences not shown are illegal or reserved.

3. Current State Definitions:

Idle: The bank or banks have been precharged, and tRP has been met.

Row Active: A row in the bank has been activated, and tRCD has been met. No data bursts / accesses and no register accesses are in progress.

Reading: A READ burst has been initiated, with Auto Precharge disabled.

Writing: A WRITE burst has been initiated, with Auto Precharge disabled.

4. The following states must not be interrupted by a command issued to the same bank. NOP commands or allowable commands to the other banks should be issued on any clock edge occurring during these states. Allowable commands to the other banks are determined by its current state and Table "Current State Bank n - Command to Bank n", and according to Table "Current State Bank n - Command to Bank n".

Precharging: starts with the registration of a PRECHARGE command and ends when tRP is met. Once tRP is met, the bank will be in the idle state.

Row Activating: starts with registration of an ACTIVE command and ends when tRCD is met. Once tRCD is met, the bank will be in the 'Active' state.

Read with AP Enabled: starts with the registration of the READ command with Auto Precharge enabled and ends when tRP has been met. Once tRP has been met, the bank will be in the idle state.

Write with AP Enabled: starts with registration of a WRITE command with Auto Precharge enabled and ends when tRP has been met. Once tRP is met, the bank will be in the idle state.

5. The following states must not be interrupted by any executable command; NOP commands must be applied to each positive clock edge during these states.

Refreshing (Per Bank): starts with registration of a REFRESH (Per Bank) command and ends when tRFCpb is met. Once tRFCpb is met, the bank will be in an 'idle' state.

Refreshing (All Bank): starts with registration of a REFRESH (All Bank) command and ends when tRFCab is met. Once tRFCab is met, the device will be in an 'all banks idle' state.

Idle MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Idle state.

Resetting MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Resetting state.

Active MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Row Active state.

MR Writing: starts with the registration of a MRW command and ends when tMRW has been met. Once tMRW has been met, the bank will be in the Idle state.

PrechargingAll: starts with the registration of a PRECHARGEALL command and ends when tRP is met. Once tRP is met, the bank will be in the idle state.

6. Bank-specific; requires that the bank is idle and no bursts are in progress.
7. Not bank-specific; requires that all banks are idle and no bursts are in progress.
8. Not bank-specific reset command is achieved through MODE REGISTER WRITE command.
9. This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.
10. A command other than NOP should not be issued to the same bank while a READ or WRITE burst with Auto Precharge is enabled.
11. The new Read or Write command could be Auto Precharge enabled or Auto Precharge disabled.
12. If a Precharge command is issued to a bank in the Idle state, tRP shall still apply.
13. A Write command may be applied after the completion of the Read burst, burst terminates are not permitted.
14. A Read command may be applied after the completion of the Write burst, burst terminates are not permitted.

Current State Bank n - Command to Bank m

Current State of Bank n	Command for Bank m	Operation	Next State for Bank m	Note
Any	NOP	Continue previous operation	Current State of Bank m	
Idle	Any	Any command allowed to Bank m	-	
Row Activating, Active, or Precharging	Activate	Select and activate row in Bank m	Active	6
	Read	Select column, and start read burst from Bank m	Reading	7
	Write	Select column, and start write burst to Bank m	Writing	7
	Precharge	Deactivate row in bank or banks	Precharging	8
	MRR	Read value from Mode Register	Idle MR Reading or Active MR Reading	9,10,12
Reading (Autoprecharge disabled)	Read	Select column, and start read burst from Bank m	Reading	7
	Write	Select column, and start write burst to Bank m	Writing	7,15
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	8
Writing (Autoprecharge disabled)	Read	Select column, and start read burst from Bank m	Reading	7,16
	Write	Select column, and start write burst to Bank m	Writing	7
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	8
Reading with Autoprecharge	Read	Select column, and start read burst from Bank m	Reading	7,13
	Write	Select column, and start write burst to Bank m	Writing	7,15,13
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	8
Writing with Autoprecharge	Read	Select column, and start read burst from Bank m	Reading	7,13,16
	Write	Select column, and start write burst to Bank m	Writing	7,13
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	8
Power On	Reset	Begin Device Auto-Initialization	Resetting	11, 14
Resetting	MRR	Read value from Mode Register	Resetting MR Reading	

Note:

- The table applies when both CKE_{n-1} and CKE_n are HIGH, and after tXSR or tXP has been met if the previous state was Self Refresh or PowerDown.
- All states and sequences not shown are illegal or reserved.
- Current State Definitions:
 - Idle: the bank has been precharged, and tRP has been met.
 - Active: a row in the bank has been activated, and tRCD has been met. No data bursts/accesses and no register accesses are in progress.
 - Reading: a READ burst has been initiated, with Auto Precharge disabled.
 - Writing: a WRITE burst has been initiated, with Auto Precharge disabled.
- REFRESH, SELFREFRESH, and MODEREGISTERWRITE commands may only be issued when all banks are idle.
- The following states must not be interrupted by any executable command; NOP commands must be applied during each clock cycle while in these states:
 - Idle MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Idle state.
 - Resetting MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Resetting state.
 - Active MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Row Active state.
 - MR Writing: starts with the registration of a MRW command and ends when tMRW has been met. Once tMRW has been met, the bank will be in the Idle state.
- tRRD must be met between Activate command to Bank n and a subsequent Activate command to Bank m.

7. READs or WRITEs listed in the Command column include READs and WRITEs with Auto Precharge enabled and READs and WRITEs with Auto Precharge disabled.
8. This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.
9. MRR is allowed during the Row Activating state and MRW is prohibited during the Row Activating state. (Row Activating starts with registration of an Activate command and ends when RCD is met.)
10. MRR is allowed during the Precharging state. (Precharging starts with registration of a Precharge command and ends when tRP is met.)
11. Not bank-specific; requires that all banks are idle and no bursts are in progress.
12. The next state for Bank m depends on the current state of Bank m (Idle, Row Activating, Precharging, or Active). The reader shall note that the state may be in transition when a MRR is issued. Therefore, if Bank m is in the Row Activating state and Precharging, the next state may be Active and Precharge dependent upon tRCD and tRP respectively.
13. Read with auto precharge enabled or a Write with auto precharge enabled may be followed by any valid command to other banks provided that the timing restrictions in the section of Precharge and Auto Precharge clarification are followed.
14. Reset command is achieved through MODE REGISTER WRITE command.
15. A Write command may be applied after the completion of the Read burst, burst terminates are not permitted.
16. A Read command may be applied after the completion of the Write burst, burst terminates are not permitted.

DATA MASK TRUTH TABLE

Function	DM	DQ	Note
Write Enable	L	Valid	1
Write Inhibit	H	X	1

Note:

1. Used to mask write data, provided coincident with the corresponding data.

Absolute Maximum DC Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Parameter	Symbol	Min	Max	Unit	Notes
VDD1 supply voltage relative to VSS	VDD1	-0.4	2.3	V	1
VDD2 supply voltage relative to VSS	VDD2	-0.4	1.6	V	1
VDDCA supply voltage relative to VSSCA	VDDCA	-0.4	1.6	V	1, 2
VDDQ supply voltage relative to VSSQ	VDDQ	-0.4	1.6	V	1, 3
Voltage on Any Pin relative to VSS	VIN, VOUT	-0.4	1.6	V	
Storage Temperature	TSTG	-55	125	°C	4

Note:

1. See the section "Power-up, Initialization, and Power-off" for relationships between power supplies.
2. $V_{REFC A} \leq 0.6 \times V_{DDCA}$; however, $V_{REFC A}$ may be $\geq V_{DDCA}$ provided that $V_{REFC A} \leq 300\text{mV}$.
3. $V_{REFDQ} \leq 0.7 \times V_{DDQ}$; however, V_{REFDQ} may be $\geq V_{DDQ}$ provided that $V_{REFDQ} \leq 300\text{mV}$.
4. Storage Temperature is the case surface temperature on the center/topside of the device. For the measurement conditions, please refer to JESD51-2 standard.

AC and DC Operating Conditions

Operation or timing that is not specified is illegal, and a failure such as an event, in order to guarantee proper operation, the LPDDR3 device must be powered down and then restarted through the specialized initialization sequence before normal operation can continue.

Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Core Power 1	VDD1	1.70	1.80	1.95	V
Core Power 2	VDD2	1.14	1.20	1.30	V
Input Buffer Power	VDDCA	1.14	1.20	1.30	V
I/O Buffer Power	VDDQ	1.14	1.20	1.30	V

Note :

1. VDD1 uses significantly less current than VDD2.
2. The voltage range is for DC voltage only. DC is defined as the voltages supplied at the DRAM and is inclusive of all noise up to 1MHz at the DRAM package ball.

Input Leakage Current

Parameter	Symbol	Min	Max	Unit	Note
Input Leakage current	IL	-2	2	uA	2
VREF supply leakage current	IVREF	-1	1	uA	1

Note:

1. For CA, CKE, CS_n, CK_t, CK_c. Any input $0V \leq V_{IN} \leq V_{DDCA}$ (All other pins not under test = 0V)
2. Although DM is for input only, the DM leakage shall match the DQ and DQS_t/DQS_c output leakage specification.
3. The minimum limit requirement is for testing purposes. The leakage current on VREFCA and VREFDQ pins should be minimal.
4. VREFDQ = VDDQ/2 or VREFCA = VDDCA/2. (All other pins not under test = 0V)

Operating Temperature

Parameter	Symbol	Min	Max	Unit	Note
Operating Temperature	T _{OPER}	-25	85	°C	1

Note:

1. Operating Temperature is the case surface temperature on the center-top side of the LPDDR3 device. For the measurement conditions, please refer to JESD51-2 standard.

AC and DC Input Measurement Levels

AC and DC Logic Input Levels for Single-Ended CA and CS_n Signals

Parameter	Symbol	LPDDR3 1600/1333		Unit	Note
		Min	Max		
AC Input Logic High	VIHCA	VREF + 0.150	Note 2	V	1,2
AC Input Logic Low	VILCA	Note 2	VREF - 0.150	V	1,2
DC Input Logic High	VIHCA	VREF + 0.100	VDDCA	V	1
DC Input Logic Low	VILCA	VSSCA	VREF - 0.100	V	1
Reference Voltage for CA and CS _n Inputs	VREFCA(DC)	0.49 * VDDCA	0.51 * VDDCA	V	3,4

Note:

1. For CA and CS_n input only pins. VREF = VREFCA(DC).
2. See the section "Overshoot and Undershoot Specifications".
3. The ac peak noise on VREFCA may not allow VREFCA to deviate from VREFCA(DC) by more than +/-1% VDDCA (for reference: approx. +/- 12mV).
4. For reference: approx. VDDCA/2 +/- 12mV.

AC and DC Logic Input Levels for CKE

Parameter	Symbol	Min	Max	Unit	Note
CKE Input High Level	VIHCKE	0.65 * VDDCA	Note 1	V	1
CKE Input Low Level	VILCKE	Note 1	0.35 * VDDCA	V	1

Note: 1. See the section "Overshoot and Undershoot Specifications".

AC and DC Logic Input Levels for Single-Ended Data (DQ and DM) Signals

Parameter	Symbol	LPDDR3 1600/1333		Unit	Note
		Min	Max		
AC Input High Voltage	VIHDQ	VREF + 0.150	Note 2	V	1,2
AC Input Low Voltage	VILDQ	Note 2	VREF - 0.150	V	1,2
DC Input High Voltage	VIHDQ	VREF + 0.100	VDDQ	V	1
DC Input Low Voltage	VILDQ	VSSCA	VREF - 0.100	V	1
Reference Voltage for DQ and DM Inputs	VREFDQ(DC) (DQ ODT disabled)	0.49 * VDDQ	0.51 * VDDQ	V	3,4
Reference Voltage for DQ and DM Inputs	VREFDQ(DC) (DQODT enabled)	0.5 * Vodtr - 0.01 * VDDQ	0.5 * Vodtr + 0.01 * VDDQ	V	3,5,6

Note:

1. For DQ input only pins. VREF = VREFDQ(DC).
2. See the section of Overshoot and Undershoot Specifications.
3. The ac peak noise on VREFDQ may not allow VREFDQ to deviate from VREFDQ(DC) by more than +/-1% VDDQ (for reference: approx. +/- 12mV).
4. For reference: approx. VDDQ/2 +/- 12mV.
5. For reference: approx. VODTR/2 +/- 12mV.
6. The nominal mode register programmed value for RODT and the nominal controller output impedance RON are used for the calculation of VODTR. For testing purposes a controller RON value of 50 Ω is used.

$$\text{Vodtr} = (2 * \text{RON} + \text{RTT}) / (\text{RON} + \text{RTT}) * \text{VDDQ}$$

VREF Tolerances

The dc-tolerance limits and ac-noise limits for the reference voltages VREFCA and VREFDQ are illustrated in Figure below. It shows a valid reference voltage VREF(t) as a function of time. (VREF stands for VREFCA and VREFDQ likewise). VDD stands for VDDCS for VREFCA and VDDQ for VREFDQ. VREF(DC) is the linear average of VREF(t) over a very long period of time (e.g. 1sec) and is specified as a fraction of the linear average of VDDCA or VDDQ also over a very long period of time (e.g. 1sec). This average has to meet the min/max requirements in Table "Electrical Characteristics and Operating Conditions". Furthermore VREF(t) may temporarily deviate from VREF(DC) by no more than +/-1%VDD. VREF(t) cannot track noise on VDDQ or VDDCA if this would send VREF outside these specifications.

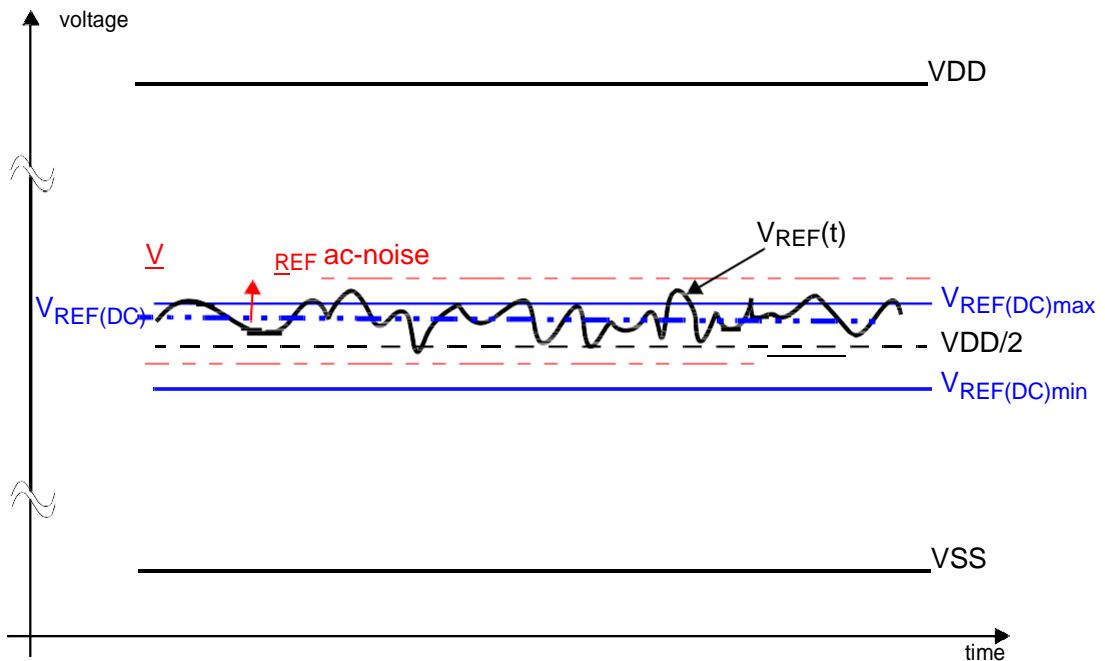


Figure. Illustration of VREF(DC) tolerance and VREF ac-noise limits

The voltage levels for setup and hold time measurements VIH(AC), VIH(DC), VIL(AC) and VIL(DC) are dependent on VREF. "VREF" shall be understood as VREF(DC), as defined in Figure above.

This clarifies that dc-variations of VREF affect the absolute voltage as a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for VREF(DC) deviations from the optimum position within the data-eye of the inputs signals.

This also clarifies that the LPDDR3 setup/hold specification and derating values need to include time and voltage associated with VREF ac-noise. Timing and voltage effects due to ac-noise on VREF up to the specified limit (+/-1% of VDD) are included in LPDDR3 timings and their associated deratings.

Input Signal

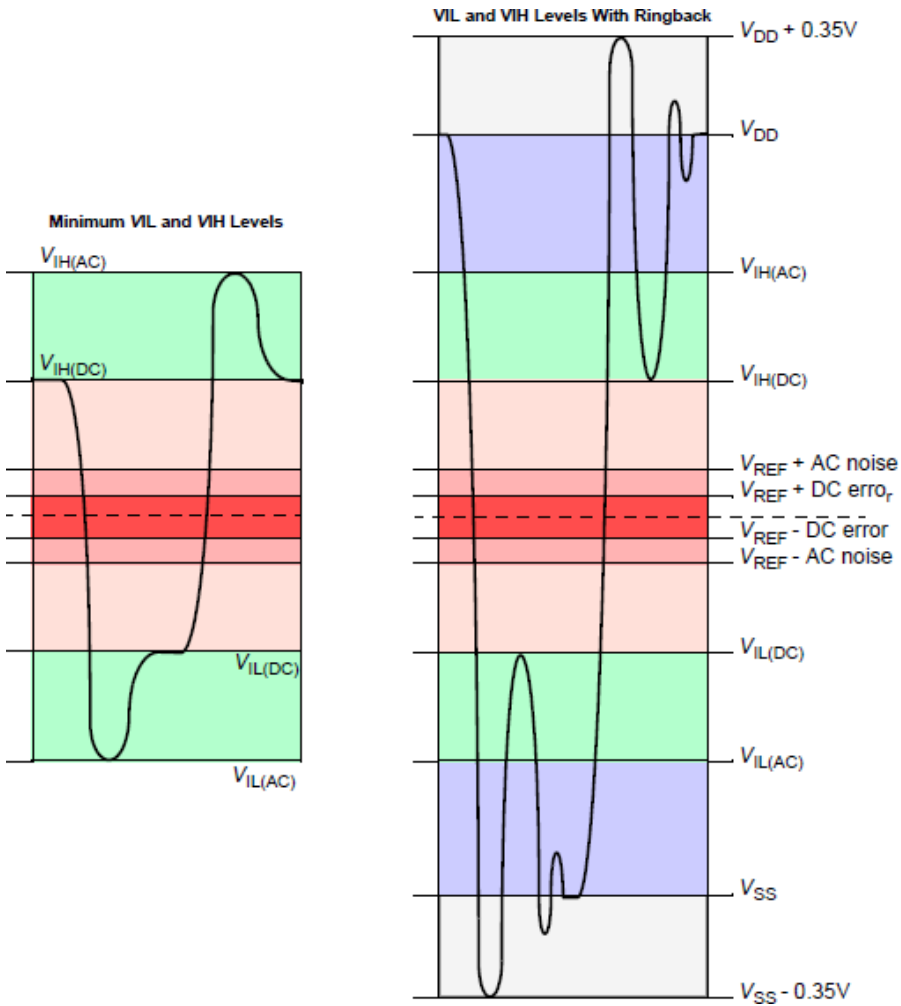


Figure. LPDDR3 Input signal

Note:

1. Numbers reflect nominal values.
2. For CA0-9, CK_t, CK_c and CS_n, VDD stands for VDDCA. For DQ, DM/DNV, DQS_t and DQS_c, VDD stands for VDDQ.
3. For CA0-9, CK_t, CK_c and CS_n, VSS stands for VSSCA. For DQ, DM/DNV, DQS_t and DQS_c, VSS stands for VSSQ.

AC and DC Logic Input Levels for Differential Signals

DifferentialSignalDefinition

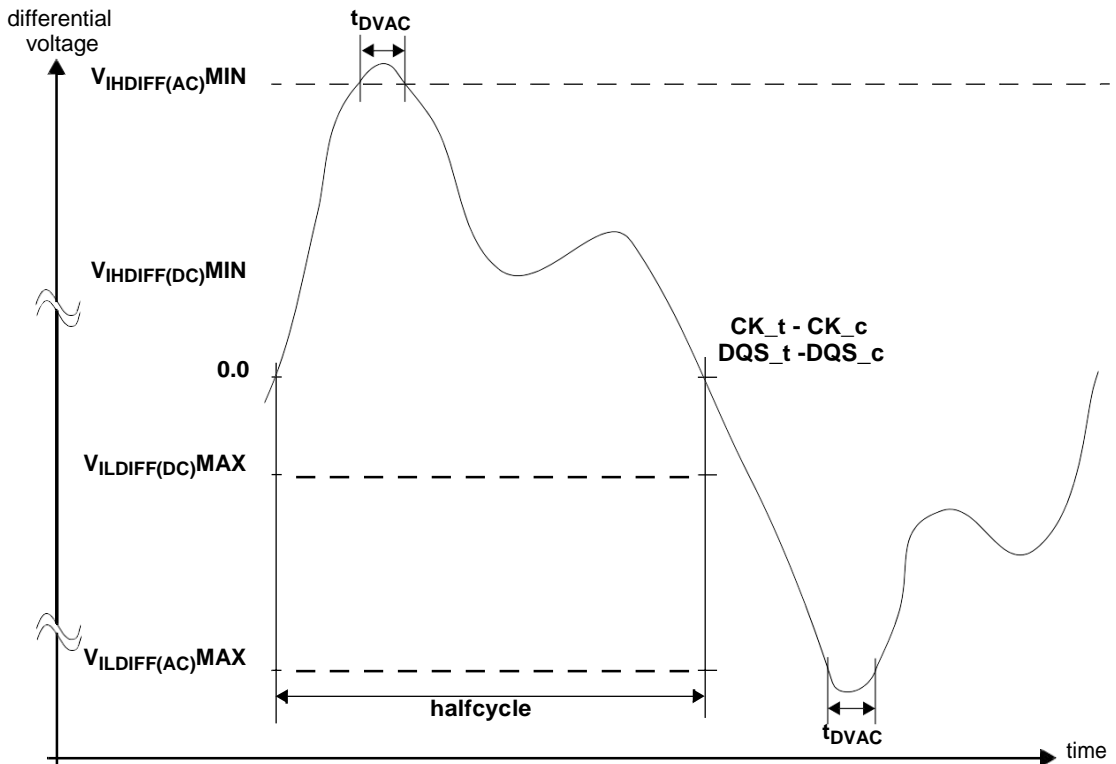


Figure. Definition of differential ac-swing and Time above ac-level t_{DVAC}

Differential swing requirements for clock and strobe

Parameter	Symbol	Min	Max	Unit	Note
DC Differential Input High	VIHDIFF(DC)	2 x (VIH(DC) - VREF)	Note 3	V	1
DC Differential Input Low	VILDIFF(DC)	Note 3	2 x (VIL(DC) - VREF)	V	1
AC Differential Input High	VIHDIFF(AC)	2 x (VIH(AC) - VREF)	Note 3	V	2
AC Differential Input Low	VILDIFF(AC)	Note 3	2 x (VIL(AC) - VREF)	V	2

Note:

- Used to define a differential signal slew-rate. For CK_t - CK_c use VIH/VIL(dc) of CA and VREFCA; for DQS_t - DQS_c, use VIH/VIL(dc) of DQs and VREFDQ; if a reduced dc-high or dc-low level is used for a signal group, then the reduced level applies also here.
- For CK_t - CK_c use VIH/VIL(ac) of CA and VREFCA; for DQS_t - DQS_c, use VIH/VIL(ac) of DQs and VREFDQ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.
- These values are not defined, however the single-ended signals CK_t, CK_c, DQS_t, and DQS_c need to be within the respective limits (VIH(dc)max, VIL(dc)min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to the section of "Overshoot and Undershoot Specifications".
- For CK_t and CK_c, Vref = VrefCA(DC). For DQS_t and DQS_c, Vref = VrefDQ(DC).

Table. Allowed time before ringback (tDVAC) for DQS_t - DQS_c

Slew Rate [V/ns]	t _{DVAC} [ps] @ VIH/Ldiff(ac) = 300mV	t _{DVAC} [ps] @ VIH/Ldiff(ac) = 300mV
	1600Mbps	1333Mbps
	MIN	MIN
> 8.0	48	58
8.0	48	58
7.0	46	56
6.0	43	53
5.0	40	50
4.0	35	45
3.0	27	37
<3.0	27	37

Table. Allowed time before ringback (tDVAC) for CK_t - CK_c

Slew Rate [V/ns]	t _{DVAC} [ps] @ VIH/Ldiff(ac) = 300mV	t _{DVAC} [ps] @ VIH/Ldiff(ac) = 300mV
	1600Mbps	1333Mbps
	MIN	MIN
> 8.0	48	58
8.0	48	58
7.0	46	56
6.0	43	53
5.0	40	50
4.0	35	45
3.0	27	37
<3.0	27	37

Single-ended Requirements for Differential Signals

Each individual component of a differential signal (CK_t, DQS_t, CK_c, or DQS_c) has also to comply with certain requirements for single-ended signals.

CK_t and CK_c shall meet $V_{SEH}(AC)_{min}$ / $V_{SEL}(AC)_{max}$ in every half-cycle.

DQS_t, DQS_c shall meet $V_{SEH}(AC)_{min}$ / $V_{SEL}(AC)_{max}$ in every half-cycle proceeding and following a valid transition.

Note that the applicable ac-levels for CA and DQ's are different per speed-bin.

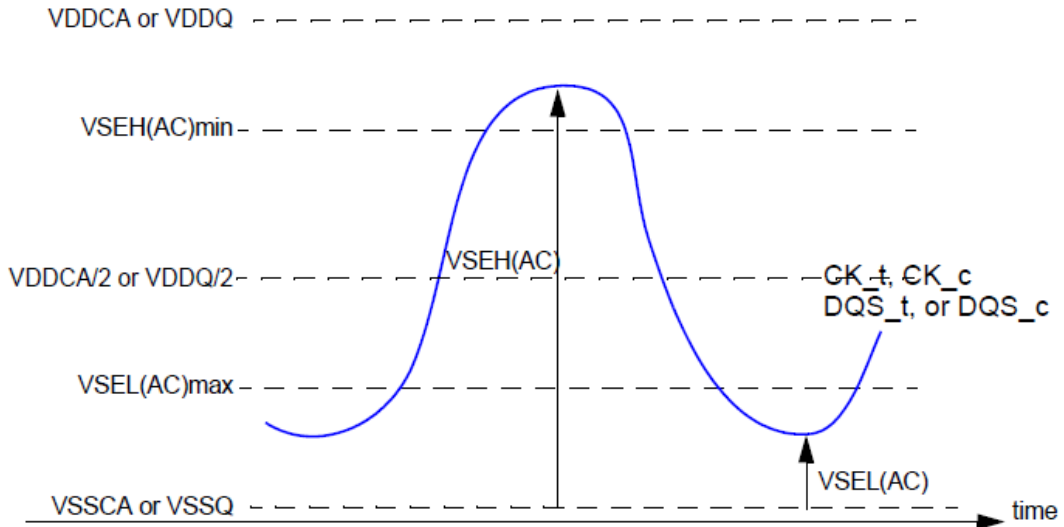


Figure. Single-ended requirement for differential signals

Note that while CA and DQ signal requirements are with respect to V_{REF} , the single-ended component of differential signals have a requirement with respect to $V_{DDQ}/2$ for DQS_t, DQS_c and $V_{DDCA}/2$ for CK_t, CK_c; this is nominally the same. The transition of single-ended signals through the ac-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach $V_{SEL}(AC)_{max}$, $V_{SEH}(AC)_{min}$ has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

Table. Single-ended Levels for Clock and Strobe

Parameter	Symbol	Min	Max	Unit	Note
Single-ended High Level for strobes	VSEH (AC150)	$(VDDQ/2) + 0.150$	Note 3	V	1, 2
Single-ended High Level for CK_t and CK_c		$(VDDCA/2) + 0.150$	Note 3	V	1, 2
Single-ended Low Level for strobes	VSEL (AC150)	Note 3	$(VDDQ / 2) - 0.150$	V	1, 2
Single-ended Low Level for CK_t and CK_c		Note 3	$(VDDCA / 2) - 0.150$	V	1, 2
Single-ended High Level for strobes	VSEH (AC135)	$(VDDQ/2) + 0.135$	Note 3	V	1, 2
Single-ended High Level for CK_t and CK_c		$(VDDCA/2) + 0.135$	Note 3	V	1, 2
Single-ended Low Level for strobes	VSEL (AC135)	Note 3	$(VDDQ / 2) - 0.135$	V	1, 2
Single-ended Low Level for CK_t and CK_c		Note 3	$(VDDCA / 2) - 0.135$	V	1, 2

Note:

1. For CK_t, CK_c use VSEH/VSEL(AC) of CA; for strobes (DQS0_t, DQS0_c, DQS1_t, DQS1_c, DQS2_t, DQS2_c, DQS3_t, DQS3_c) use VIH/VIL(AC) of DQs.
2. IH(AC)/VIL(AC) for DQs is based on VREFDQ; VSEH(AC)/VSEL(AC) for CA is based on VREFCA; if a reduced level is used for a signal group, then the reduced level applies also here.
3. These values are not defined, however the single-ended signals CK_t, CK_c, DQS0_t, DQS0_c, DQS1_t, DQS1_c, DQS2_t, DQS2_c, DQS3_t, DQS3_c need to be within the respective limits (VIH(DC)max, VIL(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to the section of Overshoot and Undershoot Specifications.

Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK_t, CK_c and DQS_t, DQS_c) must meet the requirements in "Single-ended Levels for Clock and Strobe". The differential input cross point voltage V_{IX} is measured from the actual cross point of true and complement signals to the midlevel between V_{DD} and V_{SS}.

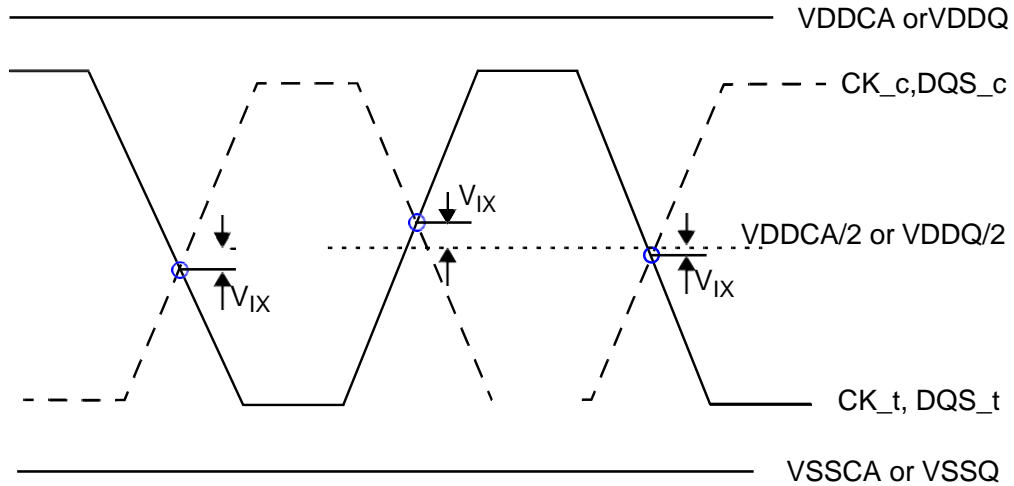


Figure. V_{IX} definition

Table. Cross Point Voltage for Differential Input Signals (Clock and Strobe)

Parameter	Symbol	Min	Max	Unit	Note
Differential Input Cross Point Voltage relative to V _{DDCA} /2 for CK_t and CK_c	V _{IXCA}	-120	120	mV	1, 2
Differential Input Cross Point Voltage relative to V _{DDQ} /2 for DQS_t and DQS_c	V _{IXDQ}	-120	120	mV	1, 2

Note:

- The typical value of V_{IX(AC)} is expected to be about 0.5xV_{DD} of the transmitting device, and V_{IX(AC)} is expected to track variations in V_{DD}. V_{IX(AC)} indicates the voltage at which differential input signals must cross.
- For CK_t and CK_c, V_{REF} = V_{REFCA}(DC). For DQS_t and DQS_c, V_{REF} = V_{REFDQ}(DC).

Slew Rate Definitions for Single-ended Input Signals

See "CAandCS_nSetup, HoldandDerating" for single-ended slew rate definitions for address and command signals.

See "Data Setup, Hold and Slew Rate Derating" for single-ended slew rate definitions for data signals.

Slew Rate Definitions for Differential Input Signals

Input slew rate for differential signals (CK_t, CK_c and DQS_t, DQS_c) are defined and measured as shown in the table and figure below.

Table. Differential Input Slew Rate Definition

Parameter	Measured		Defined by
	From	To	
Differential Input Slew Rate for Rising Edge (CK_t - CK_c and DQS_t - DQS_c)	V _{ILdiffmax}	V _{IHdiffmin}	$[V_{IHdiffmin} - V_{ILdiffmax}] / \Delta TR_{diff}$
Differential Input Slew Rate for Falling Edge (CK_t - CK_c and DQS_t - DQS_c)	V _{IHdiffmin}	V _{ILdiffmax}	$[V_{IHdiffmin} - V_{ILdiffmax}] / \Delta TF_{diff}$

Note: 1. The differential signal (i.e. CK_t - CK_c and DQS_t - DQS_c) must be linear between these thresholds.

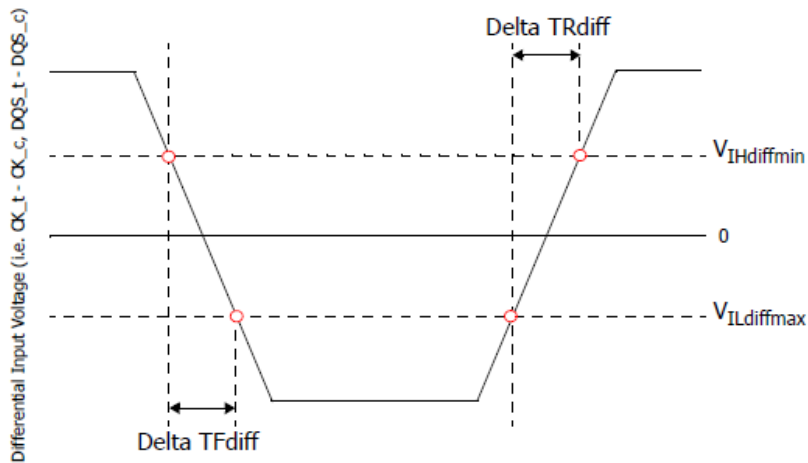


Figure. Differential Input Slew Rate Definition for CK_t, CK_c and DQS_t, DQS_c

AC and DC Output Measurement Levels

Single Ended AC and DC Output Levels

Parameter	Symbol	Levels	Unit	Note
DC Output Logic High Measurement Level (for IV curve linearity)	VOH(DC)	$0.9 \times VDDQ$	V	1
DC Output Logic Low Measurement Level (for IV curve linearity)	VOL(DC) ODT disabled	$0.1 \times VDDQ$	V	2
	VOL(DC) ODT enabled	$VDDQ * [0.1 + 0.9 * (RON / (RTT + RON))]$	V	3
AC Output Logic High Measurement Level (for output slew rate)	VOH(AC)	$VREFDQ + 0.12$	V	
AC Output Logic Low Measurement Level (for output slew rate)	VOL(AC)	$VREFDQ - 0.12$	V	
Output Leakage current (DQ, DM, DQS_t and DQS_c) (DQ, DQS_t and DQS_c are disabled; $0V \leq VOUT \leq VDDQ$)	Min	-5	uA	
	Max	5	uA	
Delta RON between pull-up and pull-down for DQ and DM	Min	-15	%	
	Max	15	%	

Note:

- IOH = -0.1mA,
- IOL = 0.1mA
- The min value is derived when using RTT, min and RON,max (+/- 30% uncalibrated, +/-15% calibrated).

Differential AC and DC Output Levels (DQS_t, DQS_c)

Parameter	Symbol	Levels	Unit	Note
AC Differential Output High measurement Level (for Output SR)	VOHdiff(AC)	$+ 0.20 \times VDDQ$	V	
AC Differential Output Low measurement Level (for Output SR)	VOLdiff(AC)	$- 0.20 \times VDDQ$	V	

Note:

- IOH = -0.1mA,
- IOL = 0.1mA

Single Ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC) for single ended signals as shown in below Table and Figure.

Parameter	Measured		Defined by
	From	To	
Single Ended Output Slew Rate for Rising Edge	VOL(AC)	VOH(AC)	$[VOH(AC) - VOL(AC)] / \Delta TRse$
Single Ended Output Slew Rate for Falling Edge	VOH(AC)	VOL(AC)	$[VOH(AC) - VOL(AC)] / \Delta TFse$

Note: Output slew rate is verified by design and characterization and may not be subject to production test.

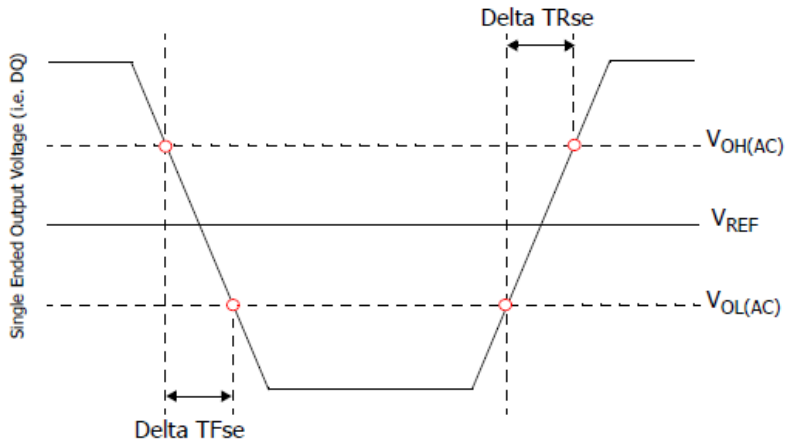


Figure. Single Ended Output Slew Rate Definition

Table. Output Slew Rate (Single Ended)

Parameter	Symbol	Min	Max	Unit	Note
Single-ended Output Slew Rate (RON = 40Ω +/- 30%)	SRQse	1.5	4.0	V/ns	
Output slew-rate matching Ratio (Pull-up to Pull-down)		0.7	1.4		

Description:

SR: Slew Rate

Q: Query Output (like in DQ, which stands for Data-in, Query-Output)

se: Single-ended Signals

Note:

1. Measured with output reference load.
2. The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.
3. The output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC).
4. Slew rates are measured under average SSO conditions, with 50% of DQ signals per data byte switching.

Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OLdiff(AC)}$ and $V_{OHdiff(AC)}$ for differential signals as shown in below Table and Figure.

Parameter	Measured		Defined by
	From	To	
Differential Output Slew Rate for Rising Edge	$V_{OLdiff(AC)}$	$V_{OHdiff(AC)}$	$[V_{OHdiff(AC)} - V_{OLdiff(AC)}] / \Delta TR_{diff}$
Differential Output Slew Rate for Falling Edge	$V_{OHdiff(AC)}$	$V_{OLdiff(AC)}$	$[V_{OHdiff(AC)} - V_{OLdiff(AC)}] / \Delta TF_{diff}$

Note: 1. Output slew rate is verified by design and characterization, and may not be subject to production test.

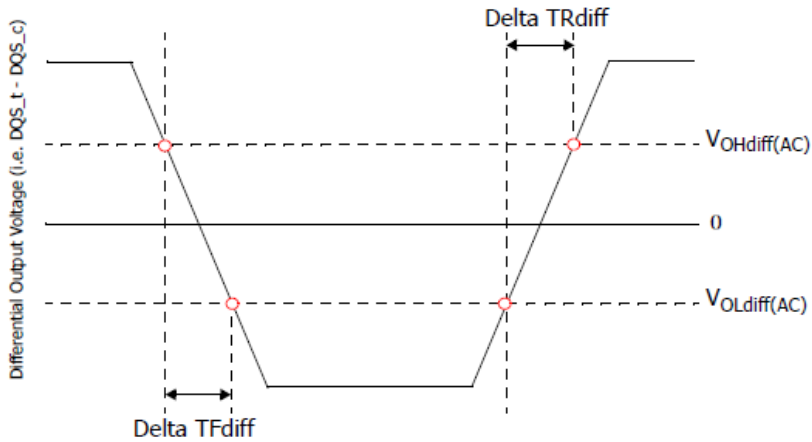


Figure. Differential Output Slew Rate Definition

Table. Output Slew Rate (Differential)

Parameter	Symbol	Min	Max	Unit	Note
Differential Output Slew Rate (RON = 40Ω +/- 30%)	SRQ _{diff}	3.0	8.0	V/ns	

Description:

SR: Slew Rate

Q: Query Output (like in DQ, which stands for Data-in, Query-Output)

diff: Differential Signals

Note:

1. Measured with output reference load.
2. The output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$.
3. Slew rates are measured under average SSO conditions, with 50% of DQ signals per data byteswitching.

Overshoot and Undershoot Specifications

Parameter	1600	1333	Unit
Maximum peak amplitude allowed for overshoot area	0.35		V
Maximum peak amplitude allowed for undershoot area	0.35		V
Maximum overshoot area above VDD	0.10	0.12	V-ns
Maximum undershoot area below VSS	0.10	0.12	V-ns

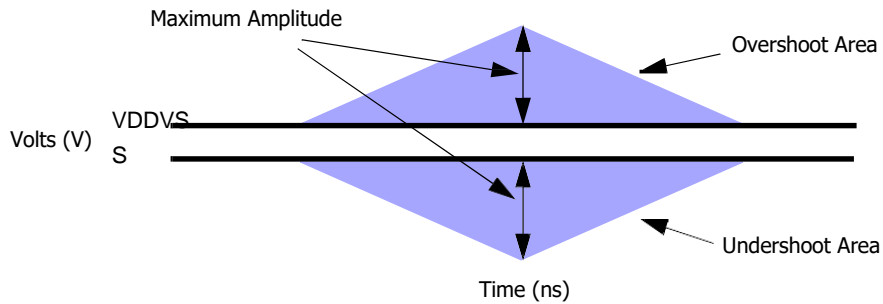


Figure. Overshoot and Undershoot Definition

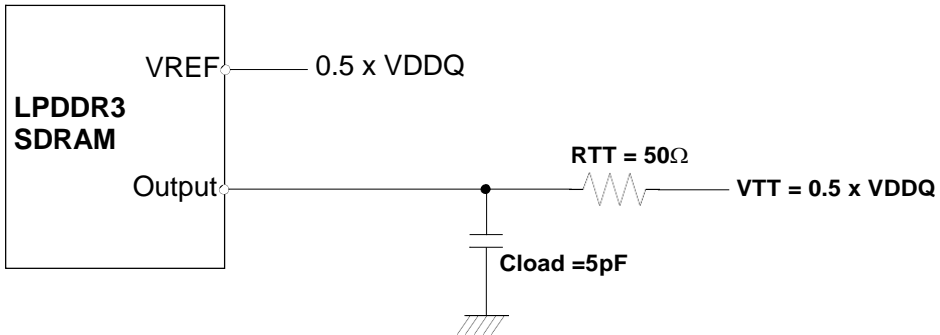
Note:

1. VDD stands for VDDCA for CA0-9, CK_t, CK_c, CS_n, and CKE. VDD stands for VDDQ for DQ, DM, ODT, DQS_t, and DQS_c.
2. VSS stands for VSSCA for CA0-9, CK_t, CK_c, CS_n, and CKE. VSS stands for VSSQ for DQ, DM, ODT, DQS_t, and DQS_c.
3. Absolute maximum requirements apply.
4. Maximum peak amplitude values are referenced from actual VDD and VSS values.
5. Maximum area values are referenced from maximum operating VDD and VSS values.

Output Buffer Characteristics

HSUL_12 Driver Output Timing Reference Load

These Timing Reference Loads are not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the test electronics.



Note: 1. All output timing parameter values (like t_{DQSQ} , t_{DQSQ} , t_{QHS} , t_{HZ} , t_{RPRE} etc.) are reported with respect to this reference load. This reference load is also used to report slewrate.

Figure. HSUL_12 Driver Output Reference Load for Timing and Slew Rate

RON_{PU} and RON_{PD} resistor Definition

$$RON_{PU} = \frac{(VDDQ - V_{out})}{ABS(I_{out})}$$

Note 1: This is under the condition that RON_{PD} is turned off

$$RON_{PD} = \frac{V_{out}}{ABS(I_{out})}$$

Note 1: This is under the condition that RON_{PU} is turned off

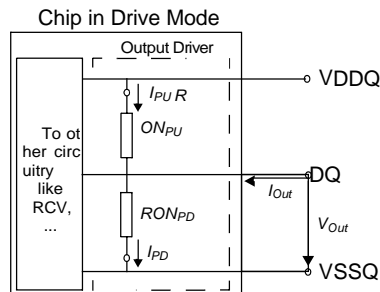


Figure. Output Driver: Definition of Voltages and Currents

RON_{PU} and RON_{PD} Characteristics with ZQ Calibration

Output driver impedance RON is defined by the value of the external reference resistor RZQ. Nominal RZQ is 240Ω.

Table - Output Driver DC Electrical Characteristics with ZQ Calibration

RON _{NOM}	Resistor	Vout	Min	Typ	Max	Unit	Notes
34.3Ω	RON34PD	0.5 x VDDQ	0.85	1.00	1.15	RZQ/7	1,2,3,4
	RON34PU	0.5 x VDDQ	0.85	1.00	1.15	RZQ/7	1,2,3,4
40.0Ω	RON40PD	0.5 x VDDQ	0.85	1.00	1.15	RZQ/6	1,2,3,4
	RON40PU	0.5 x VDDQ	0.85	1.00	1.15	RZQ/6	1,2,3,4
48.0Ω	RON48PD	0.5 x VDDQ	0.85	1.00	1.15	RZQ/5	1,2,3,4
	RON48PU	0.5 x VDDQ	0.85	1.00	1.15	RZQ/5	1,2,3,4
Mismatch between pull-up and pull-down	MM _{PUPD}		-15.00		+15.00	%	1,2,3,4,5

Note:

1. Across the operating temperature range, after calibration. 2.

RZQ = 240Ω.

3. The tolerance limits are specified after calibration with fixed voltage and temperature. For behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.

4. Pull-down and pull-up output driver impedances are recommended to be calibrated at 0.5xVDDQ.

5. Measurement definition for mismatch between pull-up and pull-down, MM_{PUPD}: Measure RON_{PU} and RON_{PD}, both at 0.5xVDDQ:

$$MM_{PUPD} = \frac{RON_{PU} - RON_{PD}}{RON_{NOM}} \times 100$$

For example, with MM_{PUPD}(max) = 15% and RON_{PD} = 0.85, RON_{PU} must be less than 1.0.

6. Output driver strength measured without ODT.

Output Driver Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to the Tables shown below.

Table. Output Driver Sensitivity Definition

Resistor	Vout	Min	Max	Unit	Notes
RONPD	0.5 x VDDQ	$85 - (dRONdT_x \Delta T) - (dRONdV_x \Delta V)$	$115 + (dRONdT_x \Delta T) + (dRONdV_x \Delta V)$	%	1,2
RONPU					
RTT	0.5 x VDDQ	$85 - (dRTTdT_x \Delta T) - (dRTTdV_x \Delta V)$	$115 + (dRTTdT_x \Delta T) + (dRTTdV_x \Delta V)$	%	1,2

Note

1. $\Delta T = T - T(@\text{calibration})$, $\Delta V = V - V(@\text{calibration})$

2. dRONdT and dRONdV are not subject to production test but are verified by design and characterization.

Table. Output Driver Temperature and Voltage Sensitivity

Symbol	Parameter	Min	Max	Unit
dRONdT	RON Temperature Sensitivity	0.00	0.75	% / C
dRONdV	RON Voltage Sensitivity	0.00	0.20	% / mV
dRTTdT	RTT Temperature Sensitivity	0.00	0.75	% / C
dRTTdV	RTT Voltage Sensitivity	0.00	0.20	% / mV

RON_{PU} and RON_{PD} Characteristics without ZQ Calibration

Output driver impedance RON is defined by design and characterization as default setting.

Table. Output Driver DC Electrical Characteristics without ZQ Calibration

RON _{NOM}	Resistor	Vout	Min	Nom	Max	Unit	Notes
34.3Ω	RON40PD	0.5 x VDDQ	24	34.3	44.6	Ω	1
	RON40PU	0.5 x VDDQ	24	34.3	44.6	Ω	1
40.0Ω	RON40PD	0.5 x VDDQ	28	40	52	Ω	1
	RON40PU	0.5 x VDDQ	28	40	52	Ω	1
48.0Ω	RON48PD	0.5 x VDDQ	33.6	48	62.4	Ω	1
	RON48PU	0.5 x VDDQ	33.6	48	62.4	Ω	1
60.0Ω (optional)	RON60PD	0.5 x VDDQ	42	60	78	Ω	1
	RON60PU	0.5 x VDDQ	42	60	78	Ω	1
80.0Ω (optional)	RON80PD	0.5 x VDDQ	56	80	104	Ω	1
	RON80PU	0.5 x VDDQ	56	80	104	Ω	1

Note:

1. Across entire operating temperature range, without calibration.

RZQ I-V Curve

Table. RZQ I-V Curve

Voltage(V)	RON = 240Ω(RZQ)							
	Pull-Down				Pull-Up			
	Current [mA] / RON [Ω]				Current [mA] / RON [Ω]			
	default value after ZQReset		with Calibration		default value after ZQReset		with Calibration	
	Min	Max	Min	Max	Min	Max	Min	Max
	[mA]	[mA]	[mA]	[mA]	[mA]	[mA]	[mA]	[mA]
0.00	0.00	0.00	n/a	n/a	0.00	0.00	n/a	n/a
0.05	0.17	0.35	n/a	n/a	-0.17	-0.35	n/a	n/a
0.10	0.34	0.70	n/a	n/a	-0.34	-0.70	n/a	n/a
0.15	0.50	1.03	n/a	n/a	-0.50	-1.03	n/a	n/a
0.20	0.67	1.39	n/a	n/a	-0.67	-1.39	n/a	n/a
0.25	0.83	1.73	n/a	n/a	-0.83	-1.73	n/a	n/a
0.30	0.97	2.05	n/a	n/a	-0.97	-2.05	n/a	n/a
0.35	1.13	2.39	n/a	n/a	-1.13	-2.39	n/a	n/a
0.40	1.26	2.71	n/a	n/a	-1.26	-2.71	n/a	n/a
0.45	1.39	3.01	n/a	n/a	-1.39	-3.01	n/a	n/a
0.50	1.51	3.32	n/a	n/a	-1.51	-3.32	n/a	n/a
0.55	1.63	3.63	n/a	n/a	-1.63	-3.63	n/a	n/a
0.60	1.73	3.93	2.17	2.94	-1.73	-3.93	-2.17	-2.94
0.65	1.82	4.21	n/a	n/a	-1.82	-4.21	n/a	n/a
0.70	1.90	4.49	n/a	n/a	-1.90	-4.49	n/a	n/a
0.75	1.97	4.74	n/a	n/a	-1.97	-4.74	n/a	n/a
0.80	2.03	4.99	n/a	n/a	-2.03	-4.99	n/a	n/a
0.85	2.07	5.21	n/a	n/a	-2.07	-5.21	n/a	n/a
0.90	2.11	5.41	n/a	n/a	-2.11	-5.41	n/a	n/a
0.95	2.13	5.59	n/a	n/a	-2.13	-5.59	n/a	n/a
1.00	2.17	5.72	n/a	n/a	-2.17	-5.72	n/a	n/a
1.05	2.19	5.84	n/a	n/a	-2.19	-5.84	n/a	n/a
1.10	2.21	5.95	n/a	n/a	-2.21	-5.95	n/a	n/a
1.15	2.23	6.03	n/a	n/a	-2.23	-6.03	n/a	n/a
1.20	2.25	6.11	n/a	n/a	-2.25	-6.11	n/a	n/a

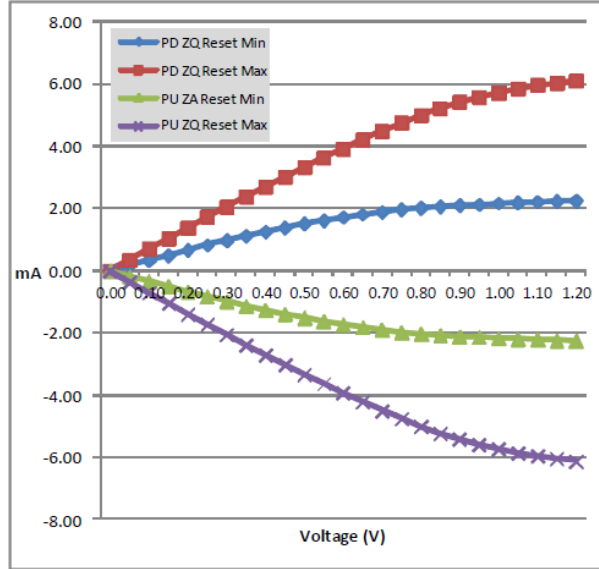


Figure. I-V Curve After ZQ Reset

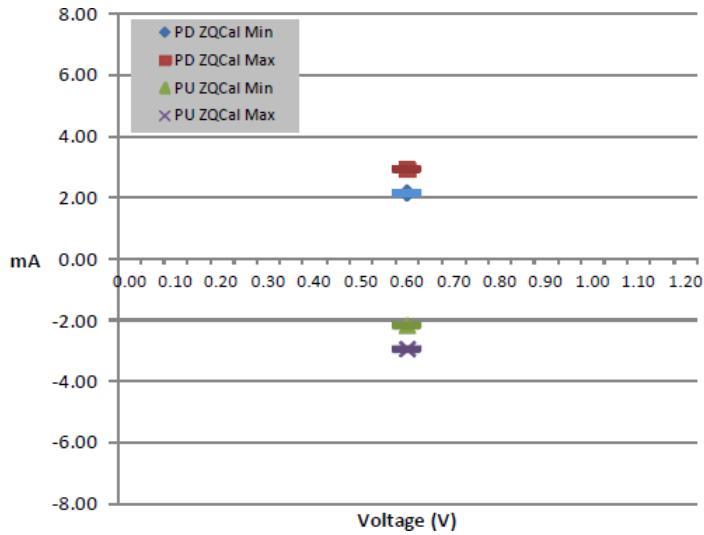


Figure. I-V Curve After Calibration

ODT Levels and I-V Characteristics

On-Die Termination effective resistance, R_{TT} , is defined by mode register MR11[1:0]. ODT is applied to the DQ, DM, and DQS_t/DQS_cpins. A functional representation of the on-die termination is shown in the figure below. R_{TT} is defined by the following formula:

$$R_{TT_{PU}} = (V_{DDQ} - V_{Out}) / |I_{Out}|$$

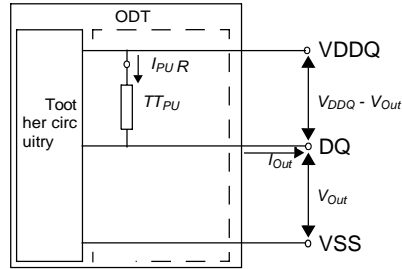


Table. ODT DC Electrical Characteristics, assuming RZQ = 240 ohm after proper ZQ calibration

RTT (ohm)	VOUT (V)	IOUT	
		Min (mA)	Max (mA)
RZQ/1	0.6	-2.17	-2.94
RZQ/2	0.6	-4.34	-5.88
RZQ/4	0.6	-8.68	-11.76

Input/Output Capacitance

Parameter	Symbol	Min	Max	Unit	Note
Input capacitance, CK_t and CK_c	CCK	0.5	1.2	pF	1,2
Input capacitance delta, CK_t and CK_c	CDCK	0	0.15	pF	1,2,3
Input capacitance, all other input-only pins	CI	0.5	1.1	pF	1,2,4
Input capacitance delta, all other input-only pins	CDI	-0.2	0.2	pF	1,2,5
Input/output capacitance, DQ, DM, DQS_t, DQS_c	CIO	1.0	1.8	pF	1,2,6,7
Input/output capacitance delta, DQS_t and DQS_c	CDDQS	0	0.2	pF	1,2,7,8
Input/output capacitance delta, DQ and DM	CDIO	-0.25	0.25	pF	1,2,7,9
Input/Output Capacitance ZQ	CZQ	0	2.0	pF	1,2

(TOPER; VDDQ = 1.14-1.3V; VDDCA = 1.14-1.3V; VDD1 = 1.7-1.95V, VDD2 = 1.14-1.3V)

Note:

1. This parameter applies to die device only (does not include package capacitance).
2. This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA) with VDD1, VDD2, VDDQ, VSS, VSSCA, VSSQ applied and all other pins floating).
3. Absolute value of CCK_t - CCK_c.
4. CI applies to CS_n, CKE, CA0-CA9.
5. $CDI = CI - 0.5 * (CCK_t + CCK_c)$
6. DM loading matches DQ and DQS.
7. MR3 I/O configuration DS OP3-OP0 = 0001B (34.30ohm typical)
8. Absolute value of CDQS_t and CDQS_c.
9. $CDIO = CIO - 0.5 * (CDQS_t + CDQS_c)$ in byte-lane.

IDD Specification Parameters and Test Conditions

IDD Measurement Conditions

The following definitions are used within the IDD measurement tables:

LOW: $V_{IN} \leq V_{IL}(DC)$ MAX HIGH:

$V_{IN} \geq V_{IH}(DC)$ MIN

STABLE: Inputs are stable at a HIGH or LOW level.

SWITCHING: See tables below.

Table. Switching for CA Input Signals

Switching for CA								
	CK_t (Rising) /CK_c (Falling)	CK_t (Falling) /CK_c (Rising)	CK_t (Rising) /CK_c (Falling)	CK_t (Falling) /CK_c (Rising)	CK_t (Rising) /CK_c (Falling)	CK_t (Falling) /CK_c (Rising)	CK_t (Rising) /CK_c (Falling)	CK_t (Falling) /CK_c (Rising)
Cycle	N		N+1		N+2		N+3	
CS_n	HIGH		HIGH		HIGH		HIGH	
CA0	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA1	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA2	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA3	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA4	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA5	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA6	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA7	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA8	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA9	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH

Note:

1. CS_n must always be driven HIGH.
2. For each clock cycle, 50% of the CA bus is changing between HIGH and LOW once per clock for the CA bus.
3. The above pattern (N, N+1, N+2, N+3...) is used continuously during IDD measurement for IDD values that require switching on the CA bus.

Table. Switching for IDD4R

Clock	CKE	CS_n	Clock Cycle Number	Command	CA[0:2]	CA[3:9]	All DQs
Rising	HIGH	LOW	N	Read_Rising	HLH	LHLHLHL	L
Falling	HIGH	LOW	N	Read_Falling	LLL	LLLLLLL	L
Rising	HIGH	HIGH	N+1	NOP	LLL	LLLLLLL	H
Falling	HIGH	HIGH	N+1	NOP	LLL	LLLLLLL	L
Rising	HIGH	HIGH	N+2	NOP	LLL	LLLLLLL	H
Falling	HIGH	HIGH	N+2	NOP	LLL	LLLLLLL	H
Rising	HIGH	HIGH	N+3	NOP	LLL	LLLLLLL	H
Falling	HIGH	HIGH	N+3	NOP	HLH	HLHLLHL	L
Rising	HIGH	LOW	N+4	Read_Rising	HLH	HLHLLHL	H
Falling	HIGH	LOW	N+4	Read_Falling	LHH	HHHHHHH	H
Rising	HIGH	HIGH	N+5	NOP	HHH	HHHHHHH	H
Falling	HIGH	HIGH	N+5	NOP	HHH	HHHHHHH	L
Rising	HIGH	HIGH	N+6	NOP	HHH	HHHHHHH	L
Falling	HIGH	HIGH	N+6	NOP	HHH	HHHHHHH	L
Rising	HIGH	HIGH	N+7	NOP	HHH	HHHHHHH	H
Falling	HIGH	HIGH	N+7	NOP	HLH	LHLHLHL	L

Note:

1. Data strobe (DQS) is changing between HIGH and LOW every clockcycle.
2. The above pattern (N, N+1, ...) is used continuously during IDD measurement forIDD4R.

Table. Switching for IDD4W

Clock	CKE	CS_n	Clock Cycle Number	Command	CA[0:2]	CA[3:9]	All DQs
Rising	HIGH	LOW	N	Write_Rising	HLL	LHLHLHL	L
Falling	HIGH	LOW	N	Write_Falling	LLL	LLLLLLL	L
Rising	HIGH	HIGH	N+1	NOP	LLL	LLLLLLL	H
Falling	HIGH	HIGH	N+1	NOP	LLL	LLLLLLL	L
Rising	HIGH	HIGH	N+2	NOP	LLL	LLLLLLL	H
Falling	HIGH	HIGH	N+2	NOP	LLL	LLLLLLL	H
Rising	HIGH	HIGH	N+3	NOP	LLL	LLLLLLL	H
Falling	HIGH	HIGH	N+3	NOP	HLL	HLHLHL	L
Rising	HIGH	LOW	N+4	Write_Rising	HLL	HLHLHL	H
Falling	HIGH	LOW	N+4	Write_Falling	LHH	HHHHHHH	H
Rising	HIGH	HIGH	N+5	NOP	HHH	HHHHHHH	H
Falling	HIGH	HIGH	N+5	NOP	HHH	HHHHHHH	L
Rising	HIGH	HIGH	N+6	NOP	HHH	HHHHHHH	L
Falling	HIGH	HIGH	N+6	NOP	HHH	HHHHHHH	L
Rising	HIGH	HIGH	N+7	NOP	HHH	HHHHHHH	H
Falling	HIGH	HIGH	N+7	NOP	HLL	LHLHLHL	L

Note:

1. Data strobe (DQS) is changing between HIGH and LOW every clockcycle.
2. Data masking (DM) must always be drivenLOW.
3. The above pattern (N, N+1...) is used continuously during IDD measurement forIDD4W.

IDD specifications (1/2)

- All IDD values are single-die-equivalent values. Total current consumption is dependent on user operating condition.

Parameter / Condition	Symbol	Power Supply	1600	Unit	Note
Operating one bank active-precharge current: tCK = tCKmin; tRC = tRCmin; CKE is HIGH; CS_n is HIGH between valid commands; CA bus inputs are switching; Data bus inputs are stable ODT disabled	IDD0 ₁	VDD1	18	mA	
	IDD0 ₂	VDD2 VDDCA	28	mA	
	IDD0 _{IN}	VDDQ	0.2	mA	4
Idle power-down standby current: tCK = tCKmin; CKE is LOW; CS_n is HIGH; All banks are idle; CA bus inputs are switching; Data bus inputs are stable ODT disabled	IDD2P ₁	VDD1	0.9	mA	
	IDD2P ₂	VDD2 VDDCA	3	mA	
	IDD2P _{IN}	VDDQ	0.2	mA	4,8
Idle power-down standby current with clock stop: CK_t = LOW, CK_c = HIGH; CKE is LOW; CS_n is HIGH; All banks are idle; CA bus inputs are stable; Data bus inputs are stable ODT disabled	IDD2PS ₁	VDD1	0.9	mA	
	IDD2PS ₂	VDD2 VDDCA	3	mA	
	IDD2PS _{IN}	VDDQ	0.2	mA	4,8
Idle non-power-down standby current: tCK = tCKmin; CKE is HIGH; CS_n is HIGH; All banks are idle; CA bus inputs are switching; Data bus inputs are stable ODT disabled	IDD2N ₁	VDD1	1.1	mA	
	IDD2N ₂	VDD2 VDDCA	15	mA	
	IDD2N _{IN}	VDDQ	0.2	mA	4
Idle non-power-down standby current with clock stopped: CK_t = LOW; CK_c = HIGH; CKE is HIGH; CS_n is HIGH; All banks are idle; CA bus inputs are stable; Data bus inputs are stable ODT disabled	IDD2NS ₁	VDD1	1.1	mA	
	IDD2NS ₂	VDD2 VDDCA	15	mA	
	IDD2NS _{IN}	VDDQ	0.2	mA	4
Active power-down standby current: tCK = tCKmin; CKE is LOW; CS_n is HIGH; One bank is active; CA bus inputs are switching; Data bus inputs are stable ODT disabled	IDD3P ₁	VDD1	3.3	mA	
	IDD3P ₂	VDD2 VDDCA	6	mA	
	IDD3P _{IN}	VDDQ	0.2	mA	4,8
Active power-down standby current with clock stop: CK = LOW, CK# = HIGH; CKE is LOW; CS_n is HIGH; One bank is active; CA bus inputs are stable; Data bus inputs are stable ODT disabled	IDD3PS ₁	VDD1	3.3	mA	
	IDD3PS ₂	VDD2 VDDCA	6	mA	
	IDD3PS _{IN}	VDDQ	0.2	mA	4,8
Active non-power-down standby current: tCK = tCKmin; CKE is HIGH; CS_n is HIGH; One bank is active; CA bus inputs are switching; Data bus inputs are stable ODT disabled	IDD3N ₁	VDD1	3.3	mA	
	IDD3N ₂	VDD2 VDDCA	18	mA	
	IDD3N _{IN}	VDDQ	0.2	mA	4

IDD specifications (2/2)

- All IDD values are single-die-equivalent values. Total current consumption is dependent on user operating condition.

Parameter / Test Condition	Symbol	Power Supply	1600		Unit	Note
Active non-power-down standby current with clock stopped: CK = LOW, CK# = HIGH CKE is HIGH; CS_n is HIGH; One bank is active; CA bus inputs are stable; Data bus inputs are stable ODT disabled	IDD3NS ₁	VDD1	3		mA	
	IDD3NS ₂	VDD2 VDDCA	15		mA	
	IDD3NS _{IN}	VDDQ	0.2		mA	4
Operating burst READ current: tCK = tCKmin; CS_n is HIGH between valid commands; One bank is active; BL = 8; RL = RL (MIN); CA bus inputs are switching; 50% data change each burst transfer ODT disabled	IDD4R ₁	VDD1	20	18	mA	
	IDD4R ₂	VDD2 VDDCA	200	180	mA	
	IDD4R _{IN}	VDDQ	275	250	mA	
Operating burst WRITE current: tCK = tCKmin; CS_n is HIGH between valid commands; One bank is active; BL = 8; WL = WLmin; CA bus inputs are switching; 50% data change each burst transfer ODT disabled	IDD4W ₁	VDD1	16	14	mA	
	IDD4W ₂	VDD2 VDDCA	180	160	mA	
	IDD4W _{IN}	VDDQ	55	50	mA	4
All-bank REFRESH burst current: tCK = tCKmin; CKE is HIGH between valid commands; tRC = tRFCabmin; Burst refresh; CA bus inputs are switching; Data bus inputs are stable ODT disabled	IDD5 ₁	VDD1	80		mA	
	IDD5 ₂	VDD2 VDDCA	120		mA	
	IDD5 _{IN}	VDDQ	0.2		mA	4
All-bank REFRESH average current: tCK = tCKmin; CKE is HIGH between valid commands; tRC = tREFI; CA bus inputs are switching; Data bus inputs are stable ODT disabled	IDD5ab ₁	VDD1	5		mA	
	IDD5ab ₂	VDD2 VDDCA	20		mA	
	IDD5ab _{IN}	VDDQ	0.2		mA	4
Per-bank REFRESH average current: tCK = tCKmin; CKE is HIGH between valid commands; tRC = tREFI/8; CA bus inputs are switching; Data bus inputs are stable ODT disabled	IDD5pb ₁	VDD1	5		mA	
	IDD5pb ₂	VDD2 VDDCA	20		mA	
	IDD5pb _{IN}	VDDQ	0.2		mA	4
Self refresh current (0°C to +85°C): CK_t = LOW, CK_c = HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable Maximum 1x self refresh rate ODT disabled	IDD6 ₁	VDD1	4		mA	6
	IDD6 ₂	VDD2 VDDCA	7.7		mA	6
	IDD6 _{IN}	VDDQ	0.2		mA	4,6,8

Note:

1. Published IDD values are the maximum of the distribution of the arithmetic mean.
2. IDD current specifications are tested after the device is properly initialized.
3. The 1x self refresh rate is the rate at which the device is refreshed internally during self refresh, before going into the elevated temperature range.
4. Measured currents are the summation of VDDQ and VDDCA.
5. Guaranteed by design without output load = T_{BDp} and $R_{ON} = 40\text{ohm}$.
6. This is the general definition that applies to full-array SELFREFRESH.
7. IDD6ET is a typical value, is sampled only, and is not tested.
8. For all IDD measurements, $V_{IHCKE} = 0.8 \times V_{DDCA}$, $V_{ILCKE} = 0.2 \times V_{DDCA}$.
9. DPD (Deep Powerdown) function is an optional feature. Please contact SKhynix for more information to use this feature.

AC TIMING PARAMETERS (1/5)

Parameter	Symbol	min max	LPDDR3 1600	LPDDR3 1333	Unit	Note
Maximum clock Frequency		-	800	667	MHz	
Clock Timing						
Average Clock Period	tCK(avg)	min	1.25	1.5	ns	
		max	100			
Average high pulse width	tCH(avg)	min	0.45		tCK(avg)	
		max	0.55			
Average low pulse width	tCL(avg)	min	0.45		tCK(avg)	
		max	0.55			
Absolute Clock Period	tCK(abs)	min	tCK(avg)min + tJIT(per)min		ns	
Absolute clock HIGH pulse width (with allowed jitter)	tCH(abs), allowed	min	0.43		tCK(avg)	
		max	0.57			
Absolute clock LOW pulse width (with allowed jitter)	tCL(abs), allowed	min	0.43		tCK(avg)	
		max	0.57			
Clock Period Jitter (with allowed jitter)	tJIT(per), allowed	min	-70	-80	ps	
		max	70	80		
Maximum Clock Jitter between two consecutive clock cycles (with allowed jitter)	tJIT(cc), allowed	max	140	160	ps	
Duty cycle Jitter (with allowed jitter)	tJIT(duty), allowed	min	min((tCH(abs)min - tCH(avg)min), (tCL(abs)min - tCL(avg)min)) * tCK(avg)		ps	
		max	max((tCH(abs)max - tCH(avg)max), (tCH(abs)max - tCL(avg)max)) * tCK(avg)			
Cumulative error across 2 cycles	tERR(2per), allowed	min	-103	-118	ps	
		max	103	118		
Cumulative error across 3 cycles	tERR(3per), allowed	min	-122	-140	ps	
		max	122	140		
Cumulative error across 4 cycles	tERR(4per), allowed	min	-136	-155	ps	
		max	136	155		
Cumulative error across 5 cycles	tERR(5per), allowed	min	-147	-168	ps	
		max	147	168		
Cumulative error across 6 cycles	tERR(6per), allowed	min	-155	-177	ps	
		max	155	177		
Cumulative error across 7 cycles	tERR(7per), allowed	min	-163	-186	ps	
		max	163	186		
Cumulative error across 8 cycles	tERR(8per), allowed	min	-169	-193	ps	
		max	169	193		
Cumulative error across 9 cycles	tERR(9per), allowed	min	-175	-200	ps	
		max	175	200		
Cumulative error across 10 cycles	tERR(10per), allowed	min	-180	-205	ps	
		max	180	205		

AC TIMING PARAMETERS (2/5)

Parameter	Symbol	min max	LPDDR3 1600	LPDDR3 1333	Unit	Note
Clock Timing (continued)						
Cumulative error across 11 cycles	tERR(11per), allowed	min	-184	-210	ps	
		max	184	210		
Cumulative error across 12 cycles	tERR(12per), allowed	min	-188	-215	ps	
		max	188	215		
Cumulative error across n cycles (n = 13, 14, . . . ,20)	tERR(nper), allowed	min	tERR(nper),allowed min = (1 + 0.68ln(n)) * tJIT(per),allowed min		ps	
		max	tERR(nper),allowed max = (1 + 0.68ln(n)) * tJIT(per),allowed max			
ZQ Calibration Parameters						
Initialization Calibration Time	tZQINIT	min	1		us	
Long Calibration Time	tZQCL	min	360		ns	
Short Calibration Time	tZQCS	min	90		ns	
Calibration Reset Time	tZQRESET	min	max(50ns, 3nCK)		ns	
Read Parameters						3
DQS output access time from CK/CK#	tDQSCK	min	2.5		ns	
		max	5.5			
DQSCK Delta short	tDQSCKDS	max	220	265	ps	4
DQSCK Delta Medium	tDQSCKDM	max	511	593	ps	5
DQSCK Delta Long	tDQSCKDL	max	614	733	ps	6
DQS-DQ skew	tDQSQ	max	135	165	ps	
DQS Output High Pulse Width	tQSH	min	tCH(abs) - 0.05		tCK(avg)	
DQS Output Low Pulse Width	tQSL	min	tCL(abs) - 0.05		tCK(avg)	
DQ/DQS output hold time from DQS	tQH	min	MIN (tQSH, tQSL)		ps	
Read preamble	tRPRE	min	0.9		tCK(avg)	7,10
Read postamble	tRPST	min	0.3		tCK(avg)	7,11
DQS low-Z from clock	tLZ(DQS)	min	tDQSCK(min) - 300		ps	7
DQ low-Z from clock	tLZ(DQ)	min	tDQSCK(min) - 300		ps	7
DQS high-Z from clock	tHZ(DQS)	max	tDQSCK(max) - 100		ps	7
DQ high-Z from clock	tHZ(DQ)	max	tDQSCK(max) + (1.4 x tDQSQ-max)		ps	7

AC TIMING PARAMETERS (3/5)

Parameter	Symbol	min max	LPDDR3 1600	LPDDR3 1333	Unit	Note
Write Parameters						3
DQ and DM input setup time (Vref based)	tDS	min	150	175	ps	
DQ and DM input hold time (Vref based)	tDH	min	150	175	ps	
DQ and DM input pulse width	tDIPW	min	0.35		tCK(avg)	
Write command to 1st DQS latching transition	tDQSS	min	0.75		tCK(avg)	
		max	1.25			
DQS input high-level width	tDQSH	min	0.4		tCK(avg)	
DQS input low-level width	tDQSL	min	0.4		tCK(avg)	
DQS falling edge to CK setup time	tDSS	min	0.2		tCK(avg)	
DQS falling edge hold time from CK	tDSH	min	0.2		tCK(avg)	
Write postamble	tWPST	min	0.4		tCK(avg)	
Write preamble	tWPRE	min	0.8		tCK(avg)	
CKE Input Parameters						
CKE min. pulse width (high/low pulse width)	tCKE	min	max(7.5ns, 3nCK)		ns	
CKE input setup time	tISCKE	min	0.25		tCK(avg)	12
CKE input hold time	tIHCKE	min	0.25		tCK(avg)	13
Command path disable delay	tCPDED	min	2		tCK(avg)	
Command Address Input Parameters						3
Address and control input setup time	tISCA	min	150	175	ps	14
Address and control input hold time	tIHCA	min	150	175	ps	14
CS_n input setup time	tISCS	min	270	290	ps	14
CS_n input hold time	tIHCS	min	270	290	ps	14
Address and control input pulse width	tIPWCA	min	0.35		tCK(avg)	
CS_n input pulse width	tIPWCS	min	0.7		tCK(avg)	
Boot Parameters (10MHz-55MHz)						15,16, 17
Clock Cycle Time	tCKb	min	18		ns	
		max	100			
CKE Input Setup Time	tISCKEb	min	2.5		ns	
CKE Input Hold Time	tIHCKEb	min	2.5		ns	
Address & Control Input Setup Time	tISb	min	1150		ps	
Address & Control Input Hold Time	tIHb	min	1150		ps	
DQS Output Data Access Time from CK/CK#	tDQSCKb	min	2.0		ns	
		max	10.0			
Data Strobe Edge to Output Data Edge tDQSQb	tDQSQb	max	1.2		ns	
Mode Register Parameters						
MODE REGISTER Write command period	tMRW	min	10		tCK(avg)	
MODE REGISTER Read command period	tMRR	min	4		tCK(avg)	
Additional time after tXP has expired until MRR command may be issued	tMRRI	min	tRCD(MIN)		ns	

AC TIMING PARAMETERS (4/5)

Parameter	Symbol	min max	LPDDR3 1600	LPDDR3 1333	Unit	Note
Core Parameters						18
Read Latency	RL	min	12	10	tCK(avg)	
Write Latency (Set A)	WL	min	6	6	tCK(avg)	
Write Latency (Set B)	WL	min	9	8	tCK(avg)	
ACTIVE to ACTIVE command period	tRC	min	tRAS+tRPab (with all-bank Precharge) tRAS+tRPpb (with per-bank Precharge)		ns	
CKE min. pulse width during Self-Refresh (low pulse width during Self-Refresh)	tCKESR	min	max(15ns, 3nCK)		ns	
Self refresh exit to next valid command delay	tXSR	min	max(tRFCab + 10ns, 2nCK)		ns	
Exit power down to next valid command delay	tXP	min	max(7.5ns, 3nCK)		ns	
CAS to CAS delay	tCCD	min	4		tCK(avg)	
Internal Read to Precharge command delay	tRTP	min	max(7.5ns, 4nCK)		ns	
RAS to CAS Delay	tRCD	min	max(18ns, 3nCK)		ns	
Row Precharge Time (single bank)	tRPpb	min	max(18ns, 3nCK)		ns	
Row Precharge Time (all banks) - 8-bank	tRPab	min	max(21ns, 3nCK)		ns	
Row Active Time	tRAS	min	max(42ns, 3nCK)		ns	
		max	70,000			
Write Recovery Time	tWR	min	max(15ns, 4nCK)		ns	
Internal Write to Read Command Delay	tWTR	min	max(7.5ns, 4nCK)		ns	
Active bank A to Active bank B	tRRD	min	max(10ns, 2nCK)		ns	
Four Bank Activate Window	tFAW	min	max(50ns, 8nCK)		ns	
ODT Parameters						
Asynchronous RTT turn-on delay from ODT in- put	tODTon	min	1.75		ns	
		max	3.5			
Asynchronous RTT turn-off delay from ODT in- put	tODToff	min	1.75		ns	
		max	3.5			
Automatic RTT turn-on delay after READ data	tAODTon	max	tDQSCkmax + 1.4 * tDQSQ- max + tCK(avg,min)		ps	
Automatic RTT turn-off delay after READ data	tAODToff	min	tDQSCkmin - 300		ps	
RTT disable delay from power down and self- refresh	tODTd	min	12		ns	
RTTenabledelayfrompowerdownandselfre- freshexit	tODTe	max	12		ns	

AC TIMING PARAMETERS (5/5)

Parameter	Symbol	min max	LPDDR3 1600	LPDDR3 1333	Unit	Note
CA Training Parameters						
First CA calibration command after CA calibration mode is programmed	tCAMRD	min	20		tCK(avg)	
First CA calibration command after CKE is LOW	tCAENT	min	10		tCK(avg)	
CA calibration exit command after CKE is HIGH	tCAEXT	min	10		tCK(avg)	
CKE LOW after CA calibration mode is programmed	tCACKEL	min	10		tCK(avg)	
CKE HIGH after the last CA calibration results are driven	tCACKEH	min	10		tCK(avg)	
Data out delay after CA training calibration command is programmed	tADR	max	20		ns	
MRW CA exit command to DQ tri-state	tMRZ	min	3		ns	
CA calibration command to CA calibration command delay	tCAD	min	RU(tADR+2*tCK)		tCK(avg)	
Write Leveling Parameters						
DQS_t/DQS_c delay after write leveling mode is programmed	tWLDQSEN	min	25		ns	
		max	-			
First DQS_t/DQS_c edge after write leveling mode is programmed	tWLMRD	min	40		ns	
		max	-			
Write leveling output delay	tWLO	min	0		ns	
		max	20			
Write leveling hold time	tWLH	min	150	135	ps	
Write leveling setup time	tWLS	min	150	135	ps	
Mode register set command delay	tMRD	min	Max(14ns, 10nCK)		ns	
		max	-			
Temperature De-Rating						17
tdQSCK De-Rating	tDQSCK (Derated)	max	5620		ps	
Core Timings Temperature De-Rating	tRCD (Derated)	min	tRCD + 1.875		ns	
	tRC (Derated)	min	tRC + 1.875		ns	
	tRAS (Derated)	min	tRAS + 1.875		ns	
	tRP (Derated)	min	tRP + 1.875		ns	
	tRRD (Derated)	min	tRRD + 1.875		ns	

CA and CS_n Setup, Hold and Derating

For all input signals (CA and CS_n) the total tIS (setup time) and tIH (hold time) required is calculated by adding the data sheet tIS (base) and tIH (base) value to the ΔtIS and ΔtIH derating values respectively. Example: $tIS(\text{total setup time}) = tIS(\text{base}) + \Delta tIS$

Setup (tIS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(DC) and the first crossing of VIH(AC) min. Setup (tIS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREF(DC) and the first crossing of VIL(AC) max. If the actual signal is always earlier than the nominal slew rate line between shaded 'VREF(DC) to a region', use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded 'VREF(DC) to a region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value.

Hold (tIH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(DC) max and the first crossing of VREF(DC). Hold (tIH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(DC) min and the first crossing of VREF(DC). If the actual signal is always later than the nominal slew rate line between shaded 'DC to VREF(DC) region', use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'DC to VREF(DC) region', the slew rate of a tangent line to the actual signal from the dc level to VREF(DC) level is used for derating value.

For a valid transition the input signal has to remain above/below VIH/IL(AC) for some time tVAC. Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached VIH/IL(AC) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach VIH/IL(AC). For slew rates in between the values listed in Table, the derating values may be obtained by linear interpolation. These values are typically not subject to production test. They are verified by design and characterization.

Table. CA Setup and Hold Base-Values

unit [ps]	LPDDR3 1600	LPDDR3 1333	Reference
tIS(base)	75	100	VIH/L(AC)=VREF(DC)+/-150mV
tIS(base)	-	-	VIH/L(AC)=VREF(DC)+/-135mV
tIH(base)	100	125	VIH/L(DC)=VREF(DC)+/-100mV

Note 1: AC/DC referenced for 2V/ns CA slew rate and 4V/ns differential CK_t/CK_c slew rate.

Table. CS_n Setup and Hold Base-Values

unit [ps]	LPDDR3 1600	LPDDR3 1333	Reference
tIS(base)	195	215	VIH/L(AC)=VREF(DC)+/-150mV
tIS(base)	-	-	VIH/L(AC)=VREF(DC)+/-135mV
tIH(base)	220	240	VIH/L(DC)=VREF(DC)+/-100mV

Note 1: AC/DC referenced for 2V/ns CS_n slew rate and 4V/ns differential CK_t/CK_c slew rate.

Table. Derating values tIS/tIH - ac/dc based AC150

		Δt_{ISCA} , Δt_{IHCA} , Δt_{ISCS} , Δt_{IHCS} derating in [ps] AC/DC based AC150 Threshold -> $V_{IH(ac)}=V_{REF(dc)}+150mV$, $V_{IL(ac)}=V_{REF(dc)}-150mV$ DC100 Threshold -> $V_{IH(dc)}=V_{REF(dc)}+100mV$, $V_{IL(dc)}=V_{REF(dc)}-100mV$											
		8.0 V/ns		7.0 V/ns		6.0 V/ns		5.0 V/ns		4.0 V/ns		3.0 V/ns	
		Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}
CA, CS_n Slew rate V/ns	4.0	38	25	38	25	38	25	38	25	38	25		
	3.0			25	17	25	17	25	17	25	17	38	29
	2.0					0	0	0	0	0	0	13	13
	1.5							-25	-17	-25	-17	-12	-4

Note 1: Cell contents shaded in red are defined as 'not supported'

Table. Derating values tIS/tIH - ac/dc based AC135

		Δt_{ISCA} , Δt_{IHCA} , Δt_{ISCS} , Δt_{IHCS} derating in [ps] AC/DC based AC135 Threshold -> $V_{IH(ac)}=V_{REF(dc)}+135mV$, $V_{IL(ac)}=V_{REF(dc)}-135mV$ DC100 Threshold -> $V_{IH(dc)}=V_{REF(dc)}+100mV$, $V_{IL(dc)}=V_{REF(dc)}-100mV$											
		8.0 V/ns		7.0 V/ns		6.0 V/ns		5.0 V/ns		4.0 V/ns		3.0 V/ns	
		Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}
CA, CS_n Slew rate V/ns	4.0	34	25	34	25	34	25	34	25	34	25		
	3.0			23	17	23	17	23	17	23	17	34	29
	2.0					0	0	0	0	0	0	11	13
	1.5							-23	-17	-23	-17	-12	-4

Note 1: Cell contents shaded in red are defined as 'not supported'

Table. Required time t_{VAC} above $V_{IH(ac)}$ {below $V_{IL(ac)}$ } for valid transition

Slew Rate [V/ns]	t_{VAC} [ps] @150mV		t_{VAC} [ps] @150mV	
	1600Mbps		1333Mbps	
	MIN	MAX	MIN	MAX
> 4.0	48	-	58	-
4.0	48	-	58	-
3.5	46	-	56	-
3.0	43	-	53	-
2.5	40	-	50	-
2.0	35	-	45	-
1.5	27	-	37	-
<1.5	27	-	37	-

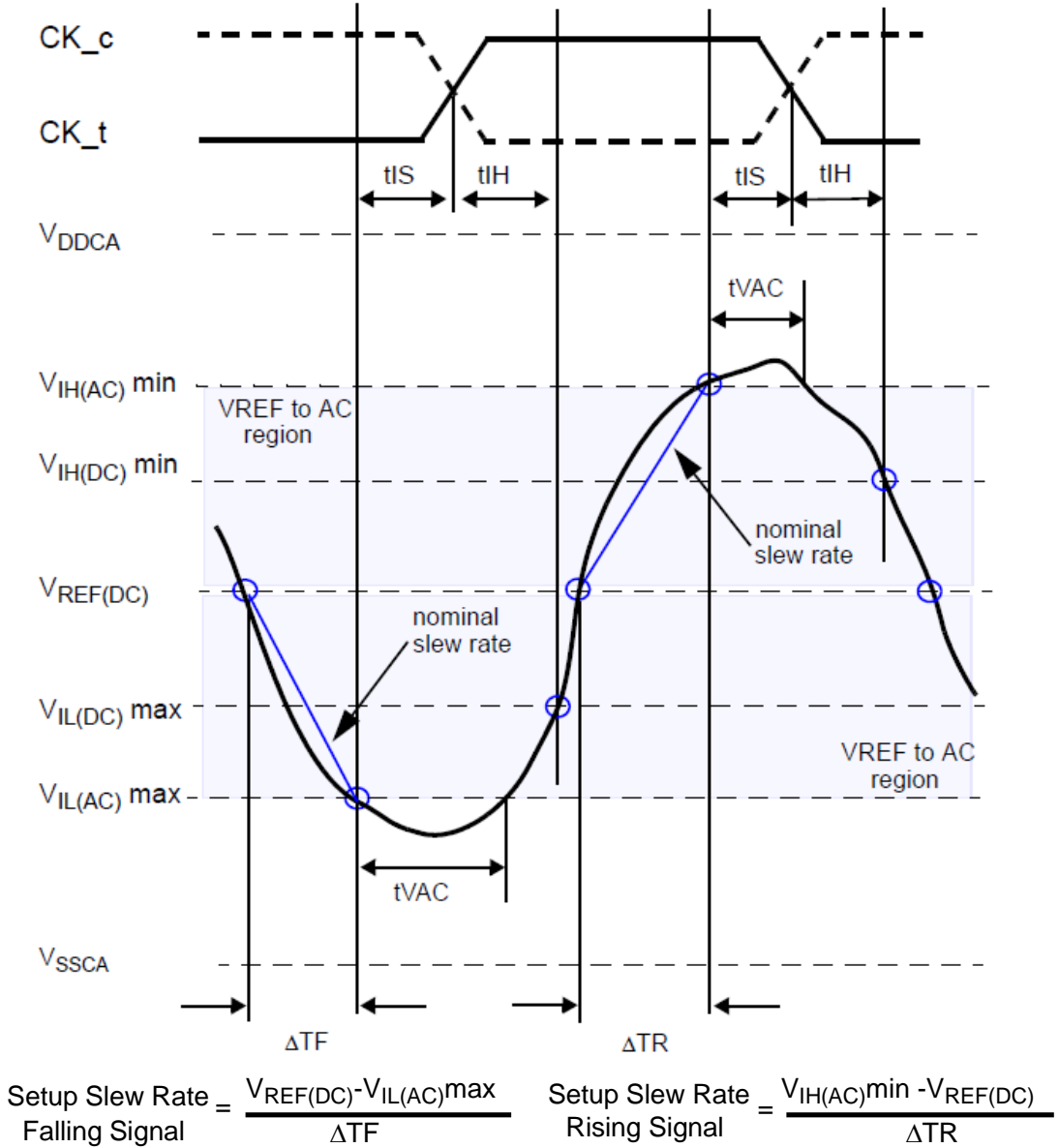
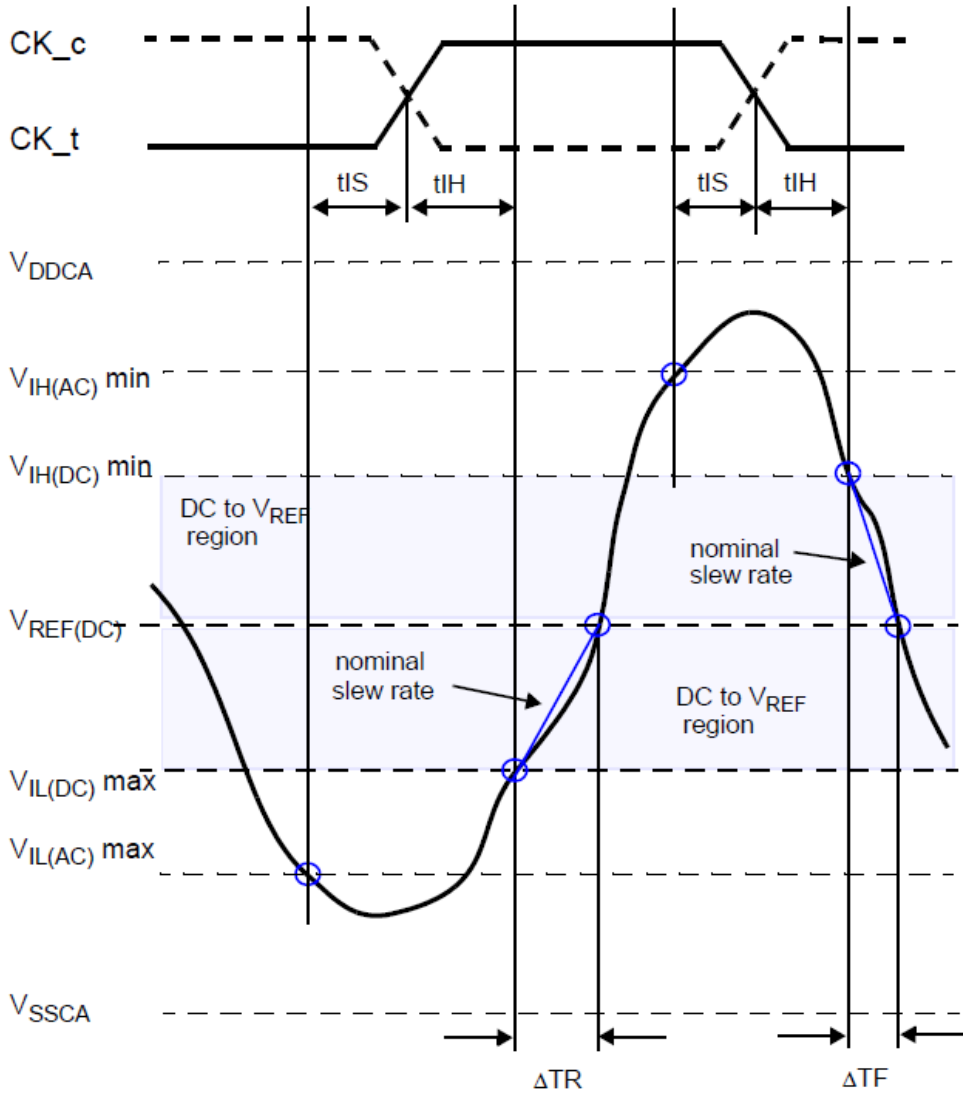


Figure. Illustration of nominal slew rate and t_{VAC} for setup time t_{IS} for CA and CS_n with respect to clock



Hold Slew Rate
Rising Signal = $\frac{V_{REF(DC)} - V_{IL(DC)max}}{\Delta TR}$

Hold Slew Rate
Falling Signal = $\frac{V_{IH(DC)min} - V_{REF(DC)}}{\Delta TF}$

Figure. Illustration of nominal slew rate for hold time t_{IH} for CA and CS_n with respect to clock

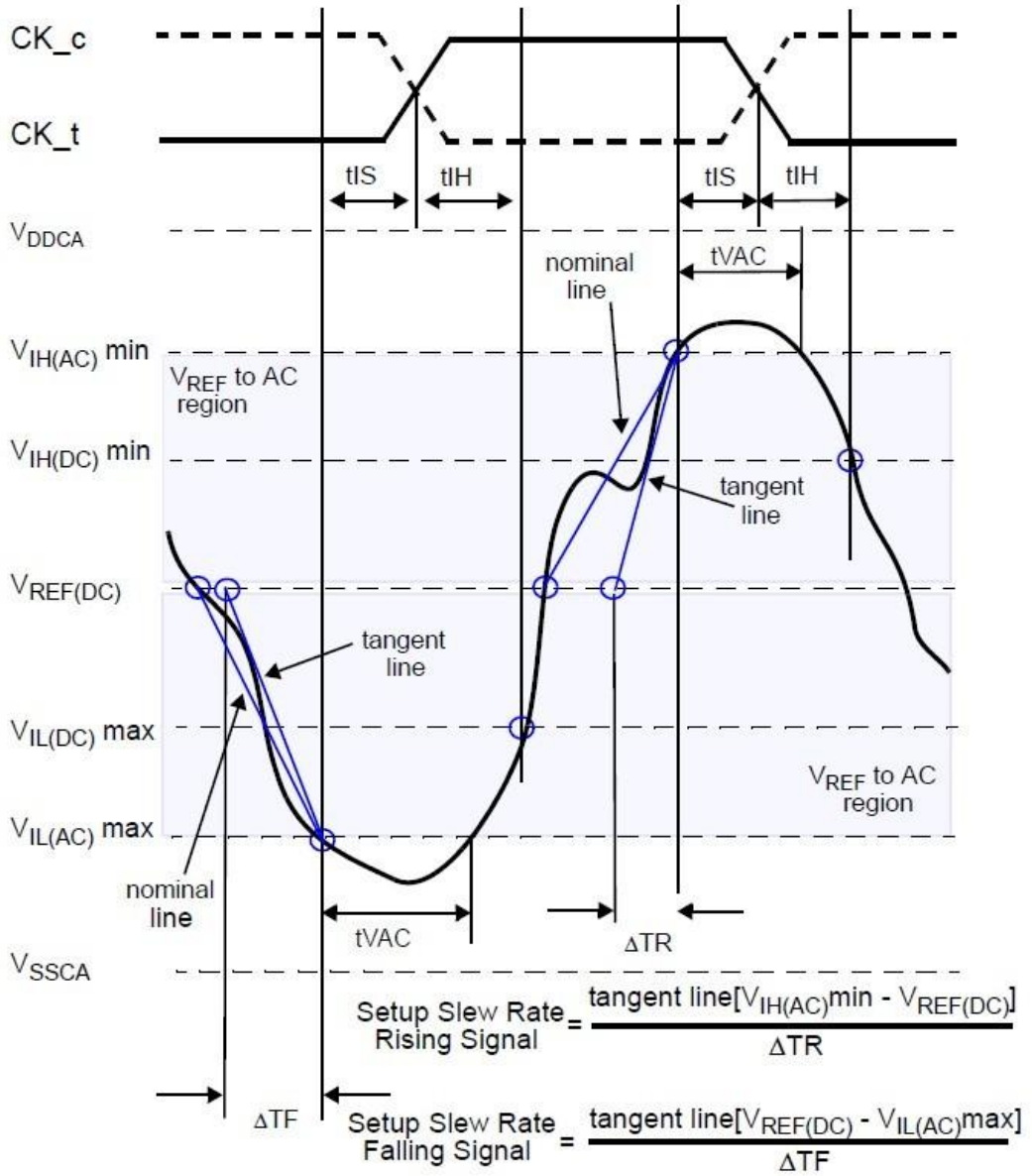


Figure. Illustration of tangent line for setup time t_{IS} for CA and CS_n with respect to clock

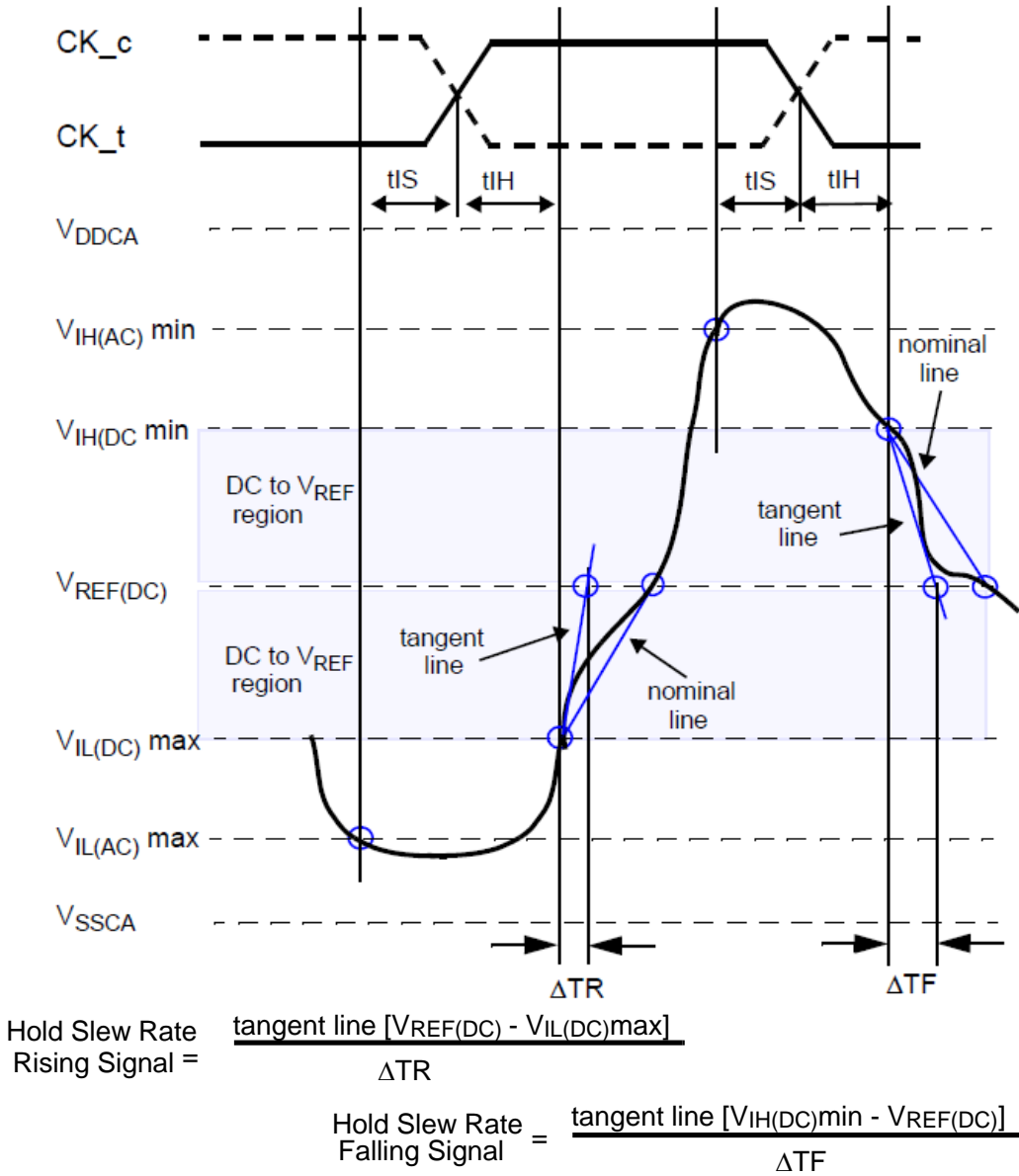


Figure. Illustration of tangent line for hold time t_{IH} for CA and CS_n with respect to clock

Data Setup, Hold and Slew Rate Derating

For all input signals (DQ, DM) the total t_{DS} (setup time) and t_{DH} (hold time) required is calculated by adding the data sheet $t_{DS}(\text{base})$ and $t_{DH}(\text{base})$ value to the Δt_{DS} and Δt_{DH} derating values respectively. Example: $t_{DS}(\text{total setup time}) = t_{DS}(\text{base}) + \Delta t_{DS}$.

Setup (t_{DS}) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF}(\text{DC})$ and the first crossing of $V_{IH}(\text{AC})_{\text{min}}$. Setup (t_{DS}) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF}(\text{DC})$ and the first crossing of $V_{IL}(\text{AC})_{\text{max}}$. If the actual signal is always earlier than the nominal slew rate line between shaded 'VREF(DC) to ac region', use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded 'VREF(DC) to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value.

Hold (t_{DH}) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL}(\text{DC})_{\text{max}}$ and the first crossing of $V_{REF}(\text{DC})$. Hold (t_{DH}) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH}(\text{DC})_{\text{min}}$ and the first crossing of $V_{REF}(\text{DC})$. If the actual signal is always later than the nominal slew rate line between shaded 'dc level to VREF(DC) region', use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to VREF(DC) region', the slew rate of a tangent line to the actual signal from the dc level to VREF(DC) level is used for derating value.

For a valid transition the input signal has to remain above/below $V_{IH}/V_{IL}(\text{AC})$ for some time t_{VAC} .

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached $V_{IH}/V_{IL}(\text{AC})$ at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach $V_{IH}/V_{IL}(\text{AC})$.

For slew rates in between the values listed in the tables the derating values may be obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization.

Table. Data Setup and Hold Base-Values

unit [ps]	LPDDR3 1600	LPDDR3 1333	Reference
$t_{DS}(\text{base})$	75	100	$V_{IH}/V_{L}(\text{AC}) = V_{REF}(\text{DC}) \pm 150\text{mV}$
$t_{DS}(\text{base})$	-	-	$V_{IH}/V_{L}(\text{AC}) = V_{REF}(\text{DC}) \pm 135\text{mV}$
$t_{DH}(\text{base})$	100	125	$V_{IH}/V_{L}(\text{DC}) = V_{REF}(\text{DC}) \pm 100\text{mV}$

Note 1: AC/DC referenced for 2V/ns DQ, DM slew rate and 4V/ns differential DQS_t-DQS_c slew rate.

Table. Derating values LPDDR3 tDS/tDH - AC/DC based AC150

		$\Delta t_{DS}, \Delta t_{DH}$ derating in [ps] AC/DC based											
		AC150 Threshold -> $V_{IH}(ac)=V_{REF}(dc)+150mV$, $V_{IL}(ac)=V_{REF}(dc)-150mV$ DC100 Threshold -> $V_{IH}(dc)=V_{REF}(dc)+100mV$, $V_{IL}(dc)=V_{REF}(dc)-100mV$											
		8.0 V/ns		7.0 V/ns		6.0 V/ns		5.0 V/ns		4.0 V/ns		3.0 V/ns	
		Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}
DQ,DM Slew rate V/ns Cellcontent	4.0	38	25	38	25	38	25	38	25	38	25		
	3.0			25	17	25	17	25	17	25	17	38	29
	2.0					0	0	0	0	0	0	13	13
	1.5							-25	-17	-25	-17	-12	-4

Note 1

Table. Derating values LPDDR3 tDS/tDH - AC/DC based AC135

		$\Delta t_{DS}, \Delta t_{DH}$ derating in [ps] AC/DC based											
		AC135 Threshold -> $V_{IH}(ac)=V_{REF}(dc)+135mV$, $V_{IL}(ac)=V_{REF}(dc)-135mV$ DC100 Threshold -> $V_{IH}(dc)=V_{REF}(dc)+100mV$, $V_{IL}(dc)=V_{REF}(dc)-100mV$											
		8.0 V/ns		7.0 V/ns		6.0 V/ns		5.0 V/ns		4.0 V/ns		3.0 V/ns	
		Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}
DQ,DM Slew rate V/ns Cellcontent	4.0	34	25	34	25	34	25	34	25	34	25		
	3.0			23	17	23	17	23	17	23	17	34	29
	2.0					0	0	0	0	0	0	11	13
	1.5							-23	-17	-23	-17	-12	-4

Note 1

Table. Required time t_{VAC} above $V_{IH}(ac)$ {below $V_{IL}(ac)$ } for valid transition

Slew Rate [V/ns]	t_{VAC} [ps] @150mV		t_{VAC} [ps] @150mV	
	1600Mbps		1333Mbps	
	MIN	MAX	MIN	MAX
> 4.0	48	-	58	-
4.0	48	-	58	-
3.5	46	-	56	-
3.0	43	-	53	-
2.5	40	-	50	-
2.0	35	-	45	-
1.5	27	-	37	-
<1.5	27	-	37	-

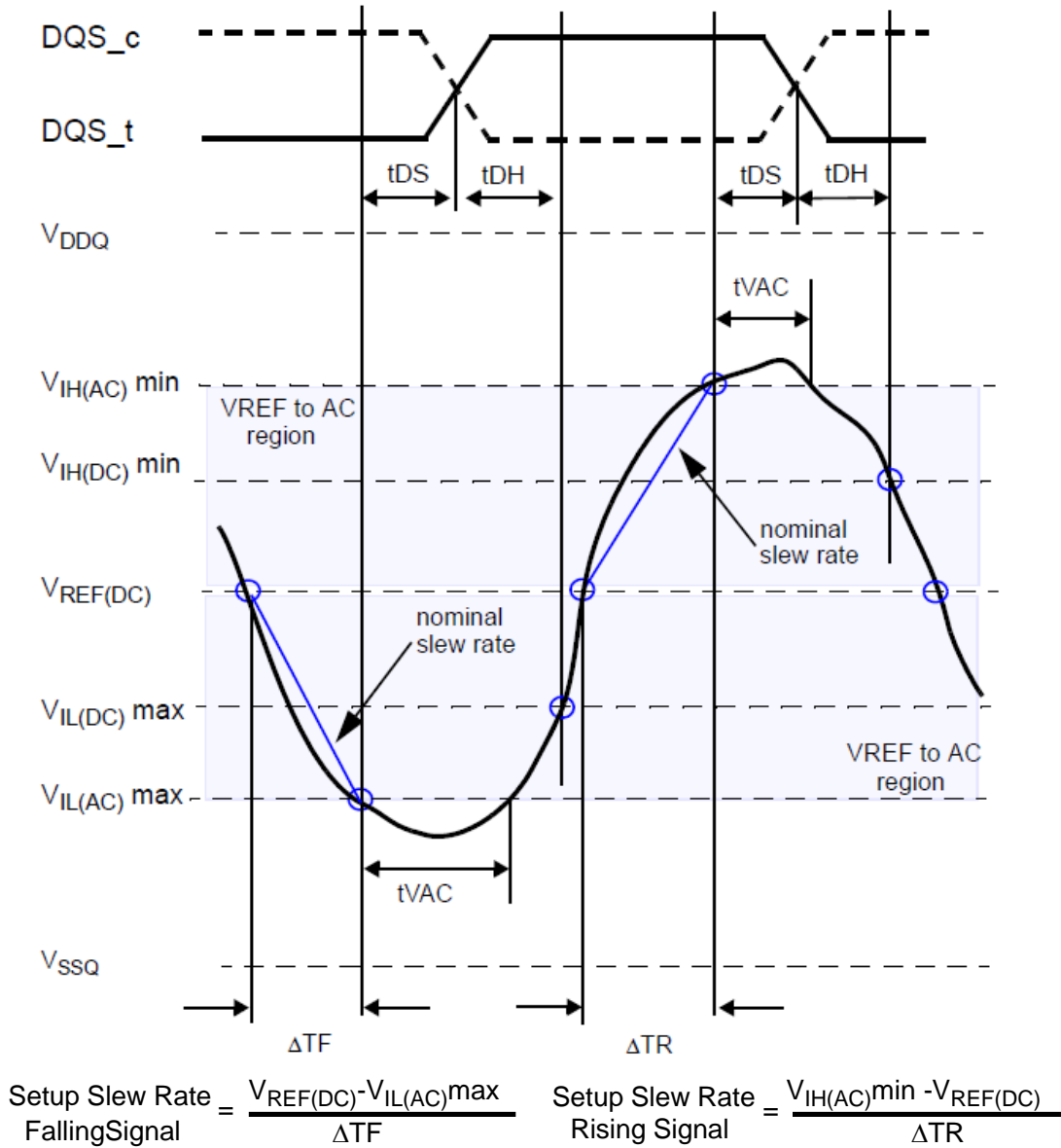


Figure. Illustration of nominal slew rate and t_{VAC} for setup time t_{DS} for DQ with respect to strobe

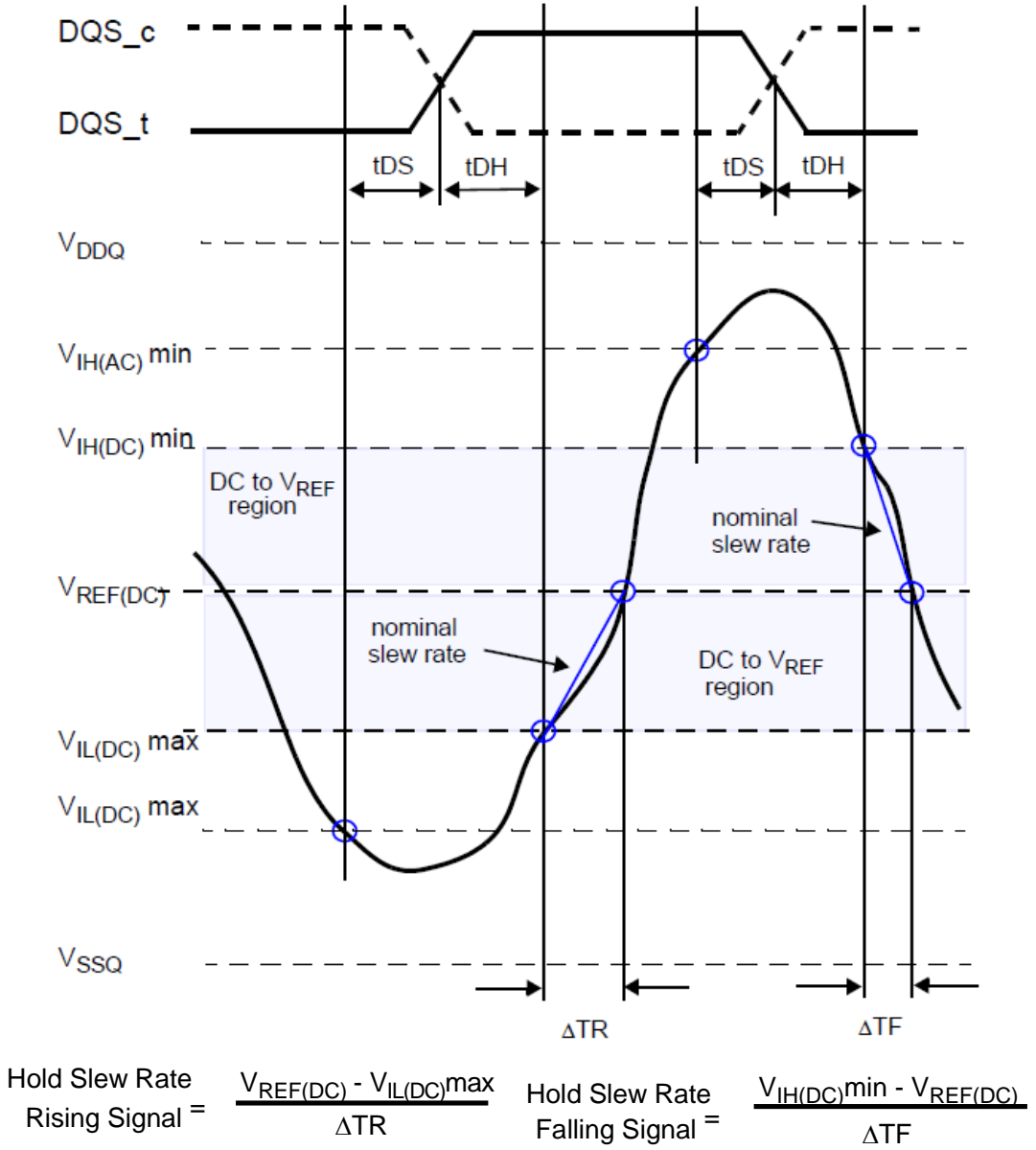


Figure. Illustration of nominal slew rate for hold time t_{DH} for DQ with respect to strobe

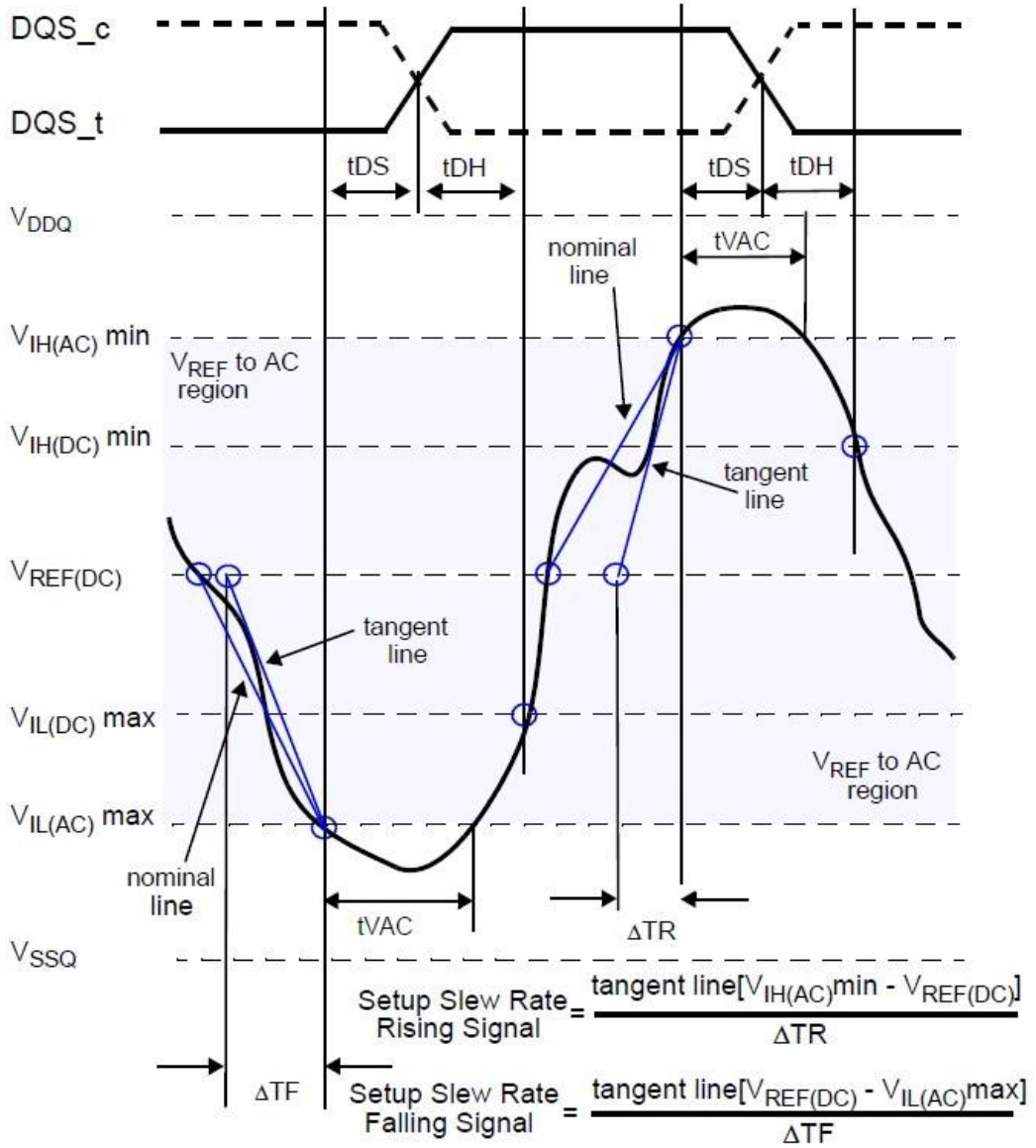


Figure. Illustration of tangent line for setup time t_{DS} for DQ with respect to strobe

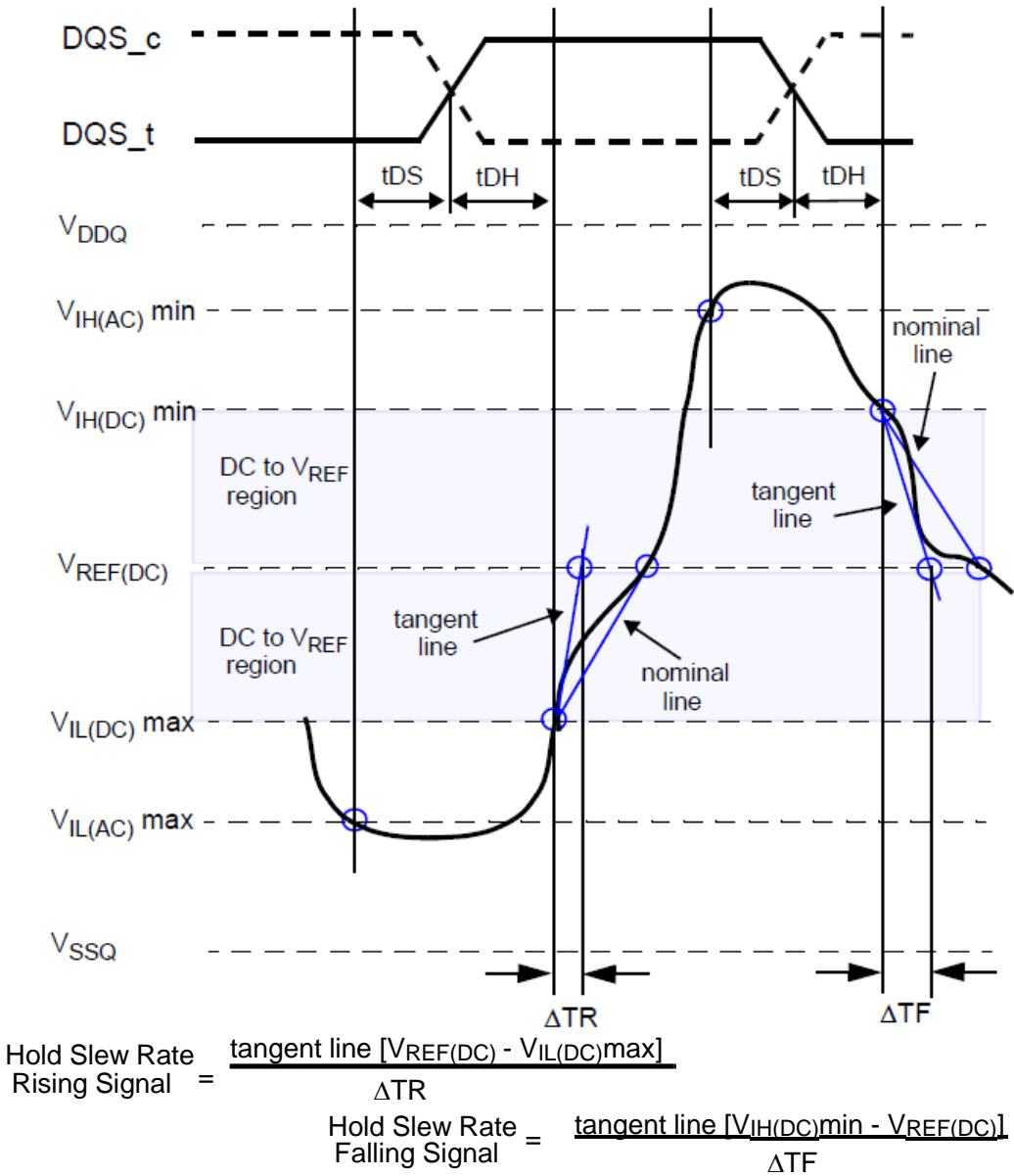


Figure. Illustration of tangent line for hold time t_{DH} for DQ with respect to strobe

Clock Specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input clocks violating the min/max values may result in malfunction of the LPDDR3 device.

Definition for tCK(avg) and nCK

tCK(avg) is calculated as the average clock period across any consecutive 200 cycle window, where each clock period is calculated from rising edge to rising edge.

$$tCK(avg) = \left(\sum_{j=1}^N tCK_j \right) / N$$

where $N = 200$

Unit 'tCK(avg)' represents the actual clock average tCK(avg) of the input clock under operation. Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges.

tCK(avg) may change by up to +/-1% within a 100 clock cycle window, provided that all jitter and timing specifications are met.

Definition for tCK(abs)

tCK(abs) is defined as the absolute clock period, as measured from one rising edge to the next consecutive rising edge. tCK(abs) is not subject to production test.

Definition for tCH(avg) and tCL(avg)

tCH(avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

$$tCH(avg) = \left(\sum_{j=1}^N tCH_j \right) / (N \times tCK(avg))$$

where $N = 200$

tCL(avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$tCL(avg) = \left(\sum_{j=1}^N tCL_j \right) / (N \times tCK(avg))$$

where $N = 200$

Definition for tJIT(per)

tJIT(per) is the single period jitter defined as the largest deviation of any signal tCK from tCK(avg).
 $tJIT(per) = \text{Min}/\text{max of } \{tCK_i - tCK(avg) \text{ where } i = 1 \text{ to } 200\}.$?
 tJIT(per),act is the actual clock jitter for a given system.
 tJIT(per),allowed is the specified allowed clock period jitter.
 tJIT(per) is not subject to production test.

Definition for tJIT(cc)

tJIT(cc) is defined as the absolute difference in clock period between two consecutive clock cycles.
 $tJIT(cc) = \text{Max of } |tCK_{i+1} - tCK_i|.$?
 tJIT(cc) defines the cycle to cycle jitter.
 tJIT(cc) is not subject to production test.

Definition for tERR(nper)

tERR(nper) is defined as the cumulative error across n multiple consecutive cycles from tCK(avg).
 tERR(nper),act is the actual clock jitter over n cycles for a given system.
 tERR(nper),allowed is the specified allowed clock period jitter over n cycles.
 tERR(nper) is not subject to production test.

$$tERR(nper) = \left(\sum_{j=i}^{i+n-1} tCK_j \right) - n \times tCK(avg)$$

tERR(nper),min can be calculated by the formula shown below:

$$tERR(nper), min = (1 + 0.68 LN(n)) \times tJIT(per), min$$

tERR(nper),max can be calculated by the formula shown below:

$$tERR(nper), max = (1 + 0.68 LN(n)) \times tJIT(per), max$$

Using these equations, tERR(nper) tables can be generated for each tJIT(per),act value

Definition for duty cycle jitter tJIT(duty)

tJIT(duty) is defined with absolute and average specification of tCH/tCL.

tJIT(duty), min can be calculated by the formula shown below:

$$tJIT(duty), min = MIN((tCH(abs), min - tCH(avg), min), (tCL(abs), min - tCL(avg), min)) \times tCK(avg)$$

tJIT(duty), max can be calculated by the formula shown below:

$$tJIT(duty), max = MAX((tCH(abs), max - tCH(avg), max), (tCL(abs), max - tCL(avg), max)) \times tCK(avg)$$

Definition for tCK(abs), tCH(abs) and tCL(abs)

These parameters are specified per their average values, however it is understood that the following relationship between the average timing and the absolute instantaneous timing holds at all times.

Parameter	Symbol	Min	Unit
Absolute Clock Period	tCK(abs)	tCK(avg),min + tJIT(per),min	ps
Absolute Clock HIGH Pulse Width	tCH(abs)	tCH(avg),min + tJIT(duty),min / tCK(avg)min	tCK(avg)
Absolute Clock LOW Pulse Width	tCL(abs)	tCL(avg),min + tJIT(duty),min / tCK(avg)min	tCK(avg)

Note:

1. tCK(avg),min is expressed in ps for this table
2. tJIT(duty),min is a negative value

Period Clock Jitter

LPDDR3 devices cannot tolerate some clock period jitter without core timing parameter de-rating. This section describes device timing requirements in the presence of clock period jitter (tJIT(per)) in excess of the values found in "ACTiming table" and how to determine cycle time de-rating and clock cycle de-rating.

Clock period jitter effects on core timing parameters (tRCD, tRP, tRTP, tWR, tWRA, tWTR, tRC, tRAS, tRRD, tFAW)

Core timing parameters extend across multiple clock cycles. Period clock jitter will impact these parameters when measured in numbers of clock cycles. When the device is operated with clock jitter within the specification limits, the LPDDR3 device is characterized and verified to support $tnPARAM = RU \{tPARAM / tCK(avg)\}$.

When the device is operated with clock jitter outside specification limits, the number of clocks or tCK(avg) may need to be increased based on the values for each core timing parameter.

Cycle time de-rating for core timing parameters

For a given number of clocks (tnPARAM), for each core timing parameter, average clock period (tCK(avg)) and actual cumulative period error (tERR(tnPARAM), act) in excess of the allowed cumulative period error

(tERR(tnPARAM), allowed), the equation below calculates the amount of cycle time de-rating (inns) required if the equation results in a positive value for a core timing parameter (tCORE).

$$Cycle\ Time\ Derating = MAX \left\{ \left(\frac{tPARAM + tERR(tnPARAM), act - tERR(tnPARAM), allowed}{tnPARAM} - tCK(avg) \right), 0 \right\}$$

A cycle time derating analysis should be conducted for each core timing parameter. The amount of cycle time derating required is the maximum of the cycle time de-ratings determined for each individual core timing parameter.

Clock Cycle de-rating for core timing parameters

For a given number of clocks (tnPARAM) for each core timing parameter, clock cycle de-ratings should be specified with amount of period jitter (tJIT(per)).

For a given number of clocks (tnPARAM), for each core timing parameter, average clock period (tCK(avg)) and actual cumulative period error (tERR(tnPARAM), act) in excess of the allowed cumulative period error

(tERR(tnPARAM), allowed), the equation below calculates the clock cycle derating (in clocks) required if the equation results in a positive value for a core timing parameter (tCORE).

$$Clock\ Cycle\ Derating = RU \left\{ \frac{tPARAM + tERR(tnPARAM), act - tERR(tnPARAM), allowed}{tCK(avg)} \right\} - tnPARAM$$

A clock cycle de-rating analysis should be conducted for each core timing parameter.

Clock jitter effects on Command/Address timing parameters (tIS, tIH, tISCKE, tIHCKE, tISb, tIHb, tISCKEb, tIHCKEb)

These parameters are measured from a command/address signal (CKE, CS, CA0-CA9) transitioned edge to its respective clock signal (CK_t/CK_c) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per)), as the setup and hold are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values shall be met.

Clock jitter effects on Read timing parameters

tRPRE

When the device is operated with input clock jitter, tRPRE need to be de-rated by the actual period jitter

tJIT(per),act,max) of the input clock in excess of the allowed period jitter (tJIT(per),allowed,max). Output de-ratings are relative to the input clock.

$$tRPRE(min, derated) = 0.9 - \left(\frac{tJIT(per), act,max - tJIT(per), allowed,max}{tCK(avg)} \right)$$

tLZ(DQ), tHZ(DQ), tDQSCK, tLZ(DQS), tHZ(DQS)

These parameters are measured from a specific clock edge to a data signal (DMn, DQm: n=0,1,2,3, m=0-31) transition and will be met with respect to that clock edge. Therefore, they are not affected by the amount of clock jitter applied (i.e. tJIT(per)).

tQSH, tQSL

These parameters are affected by duty cycle jitter which is represented by tCH(abs)min and tCL(abs)min. These parameters determine absolute Data-Valid Window (DVW) at the LPDDR3 device pin.

Absolute min DVW @ LPDDR3 device pin =
min{ (tQSH(abs)min – tDQSQmax) , (tQSL(abs)min – tDQSQmax) }

This minimum DVW shall be met at the target frequency regardless of clock jitter.

tRPST

tRPST is affected by duty cycle jitter which is represented by tCL(abs). Therefore tRPST(abs)min can be specified by tCL(abs)min.

tRPST(abs)min = tCL(abs)min – 0.05 = tQSL(abs)min

Clock jitter effects on Write timing parameters

tDS, tDH

These parameters are measured from a data signal (DM_n, DQ_m: n=0,1,2,3. m=0 –31) transition edge to its respective data strobe signal (DQSn_t, DQSn_c : n=0,1,2,3) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), as the setup and hold are relative to the data strobe signal crossing that latches the data. Regardless of clock jitter values, these values shall be met.

tDSS, tDSH

These parameters are measured from a data strobe signal (DQSx_t, DQSx_c) crossing to its respective clock signal

(CK_t/CK_c) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), as the setup and hold of the data strobes are relative to the corresponding clock signal crossing. Regardless of clock jitter values, these values shall be met.

tDQSS

This parameter is measured from a data strobe signal (DQSx_t, DQSx_c) crossing to the subsequent clock signal (CK_t/CK_c) crossing. When the device is operated within put clock jitter, this parameter need to be derated by the actual period jitter tJIT(per), act of the input clock in excess of the allowed period jitter tJIT(per), allowed.

tDQSS(min, derated) can be calculated by the formula shown below:

$$tDQSS(min, derated) = 0.75 - \frac{tJIT(per), act, min - tJIT(per), allowed, min}{tCK(avg)}$$

tDQSS(max, derated) can be calculated by the formula shown below:

$$tDQSS(max, derated) = 1.25 - \frac{tJIT(per), act, max - tJIT(per), allowed, max}{tCK(avg)}$$

Refresh Requirements

Density	Symbol	8Gb	Unit	
Number of Banks		8	-	
Refresh Window Tcase <= 85°C	tREFW	32	ms	
RefreshWindow 1/2-RateRefresh	tREFW	16	ms	
RefreshWindow 1/4-RateRefresh	tREFW	8	ms	
Required number of REFRESH commands (min)	R	8,192	-	
average time between REFRESH commands (for referenceonly) Tcase <=85°C	REFab	tREFI	3.9	us
	REFpb	tREFIpb	0.4875	us
Refresh Cycle time	tRFCab	210	ns	
Per Bank Refresh Cycle time	tRFCpb	90	ns	
Burst Refresh Window = 4 x 8 x tRFCab	tREFBW	6.72	us	

LPDDR3 Read and Write Latencies

Parameter	LPDDR3							Unit
	333	800	1066	1200	1333	1466	1600	
Max. Clock Frequency	166	400	533	600	667	733	800	NHz
Max. Data Rate	333	800	1066	1200	1333	1466	1600	MT/s
Average Clock Period	6	2.5	1.875	1.667	1.5	1.364	1.25	ns
Read Latency	3	6	8	9	10	11	12	tCK(avg)
Write Latency (Set A)	1	3	4	5	6	6	6	tCK(avg)
Write Latency (Set B)	1	3	4	5	8	9	9	tCK(avg)

Note:

1. RL=3/WL=1 setting is an optional feature. Refer to MR0OP<7>.
2. Write Latency (Set B) support is an optional feature. Refer toMR0 OP<6>.

Revision History

Rev. B – 2019/12/18

- Updated Operating temperature

Rev. A – 2018/11/14

- Initial release

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