



REALTEK

RTD2556QR-VL-CG

MULTI-FUNCTION DISPLAY CONTROLLER

DATASHEET

(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2021/04/15	First release.

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1. General Description

The Realtek RTD2556QR-VL-CG monitor controller combines an analog RGB input interface, multiple DP1.2 digital input interfaces with HDCP1.4, multiple HDMI1.4 digital input interfaces with HDCP1.4, DVI digital input interfaces with HDCP1.4. The embedded MCU is based on an industrial standard 8051 core with external serial flash.

The RTD2556QR-VL-CG is suitable for multiple market segments and display applications, such as monitor, All in One PC, and embedded applications.

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2. Features

General

- RTD2556QR-VL-CG supports input format up to 2560x1600 @ 60Hz, 2560x2048 @ 50Hz.
- Support eDP and LVDS panel interfaces
- Zoom scaling up and down
- Embedded one MCU with SPI flash controller.
- It contains 2 ADCs in key pad application
- Require only one crystal to generate all timing.
- Programmable internal low-voltage-reset (LVR)
- High resolution 6 channels PWM output, and wide range selectable PWM frequency.

Crystal

- Support 14.318MHz crystal type

Analog RGB Input Interface

- 1 Analog input supported
- Integrated 8-bit triple-channel 210MHz ADC/PLL
- Embedded programmable Schmitt trigger of HSYNC
- Support Sync-On-Green (SOG) and various kinds of composite sync modes
- On-chip high-performance hybrid PLLs
- High resolution true 64 phase ADC PLL

- YPbPr support up to HDTV 1080 resolution

High Speed Receiver

- RTD2556QR-VL-CG supports 3 ports of high speed receivers including one port of DisplayPort1.2 receiver, one port of HDMI1.4 and DisplayPort1.2 combo receiver and one ports of HDMI1.4/DVI combo receiver.
- In HDMI mode, the latest HDMI1.4 is supported
- In HDMI mode, data enable only mode is supported
- In HDMI mode, 6-bit, 8-bit, 10-bit, and 12-bit color depth transport is supported
- In HDMI mode, High-Bandwidth Digital Content Protection (HDCP 1.4) is supported
- In HDMI mode, HDMI audio is allowed to transmit to I2S/SPDIF output
- In HDMI mode, AMD HDMI Freesync technology is supported
- In DisplayPort mode, the latest DisplayPort 1.2 is supported
- In DisplayPort mode, two link layer speed HBR (2.7GHz), RBR (1.62GHz) are supported
- In DisplayPort mode, 6-bit, 8-bit, 10-bit, and 12-bit color depth transport is supported
- In DisplayPort mode, High-Bandwidth Digital Content Protection (HDCP 1.4) is supported
- In DisplayPort mode, audio is allowed to transmit to I2S/SPDIF output

- In DisplayPort mode, VESA Adaptive Sync technology is supported
- In DVI mode, Digital Content Protection (HDCP 1.4) is supported
- In DVI mode, two adjacent receivers to support dual-link DVI with HDCP

Embedded MCU

- Industrial standard 8051 core with external serial flash
- Low speed ADC for various application
- I2C Master or Slave hardware supported

Auto Detection /Auto Calibration

- Input format detection
- Compatibility with standard VESA mode and support user-defined mode
- Smart engine for Phase/Image position/Color calibration

Audio

- Output: IIS , SPDIF
- Embedded Audio DAC
- Embedded headphone amp

Scaling

- Fully programmable zoom ratios
- Independent horizontal/vertical scaling
- Advanced zoom algorithm provides high image quality
- Sharpness/Smooth filter enhancement

- Support non-linear scaling from 4:3 to 16:9 or 16:9 to 4:3

Color Processor

- True 12-bit color processing engine
- Programmable 14-bit gamma support
- xvYCC supported
- Adobe/sRGB compliance
- Advanced dithering logic for the fewer panel color depth enhancement
- Dynamic overshoot-smear canceling engine
- Brightness and contrast control
- Peaking/Coring function for video sharpness
- Support UltraVivid III function to enhance image quality with minimal artificial effect on productivity applications

VividColor™

- Independent color management (ICM)
- Dynamic contrast control (DCC)
- 2nd generation of Precise color mapping (PCM)
- Image Adaptive Power Saving (IAPS)
- Support ADC Noise Reduction

Output Interface

- Support 8-bit output through either LVDS
- Support 4-port LVDS with the speed of each port up to 93MHz

- Supports 4-lane eDP (HBR) with the output format up to 2560x1600 @ 60Hz.
- Fully programmable display timing generator
- Flexible data pair swapping for easier system design.
- Fixed Last Line output for perfect panel capability

Embedded OSD

- Embedded 30K SRAM dynamically stores OSD command and fonts
- Support multi-color RAM font, 1, 2 and 4-bit per pixel
- 64 color palette
- Maximum 26 window with alpha-blending / gradient / gradient target color / gradient reversed color/ dynamic fade-in/fade-out, bordering/ shadow
- Rotate 90,180,270 degree
- Independent row shadowing/bordering

- Programmable blinking effects for each character
- OSD-made internal pattern generator for factory mode
- Support 12x18 ~ 4x18 proportion
- Hardware decompression for OSD font
- Support OSD scrolling
- Support 2 independent font based OSD

Frame Buffer Support

- LiveShow™ Function, High-performance RTC (response time compensation).
- Embedded frame buffer

Power Supply

- 3.3V / 2.5V / 1.1V power supply

3. System Applications

- Display System on Motherboard, Monitor
- Display System for All in One PCs and embedded applications

4. Block Diagram

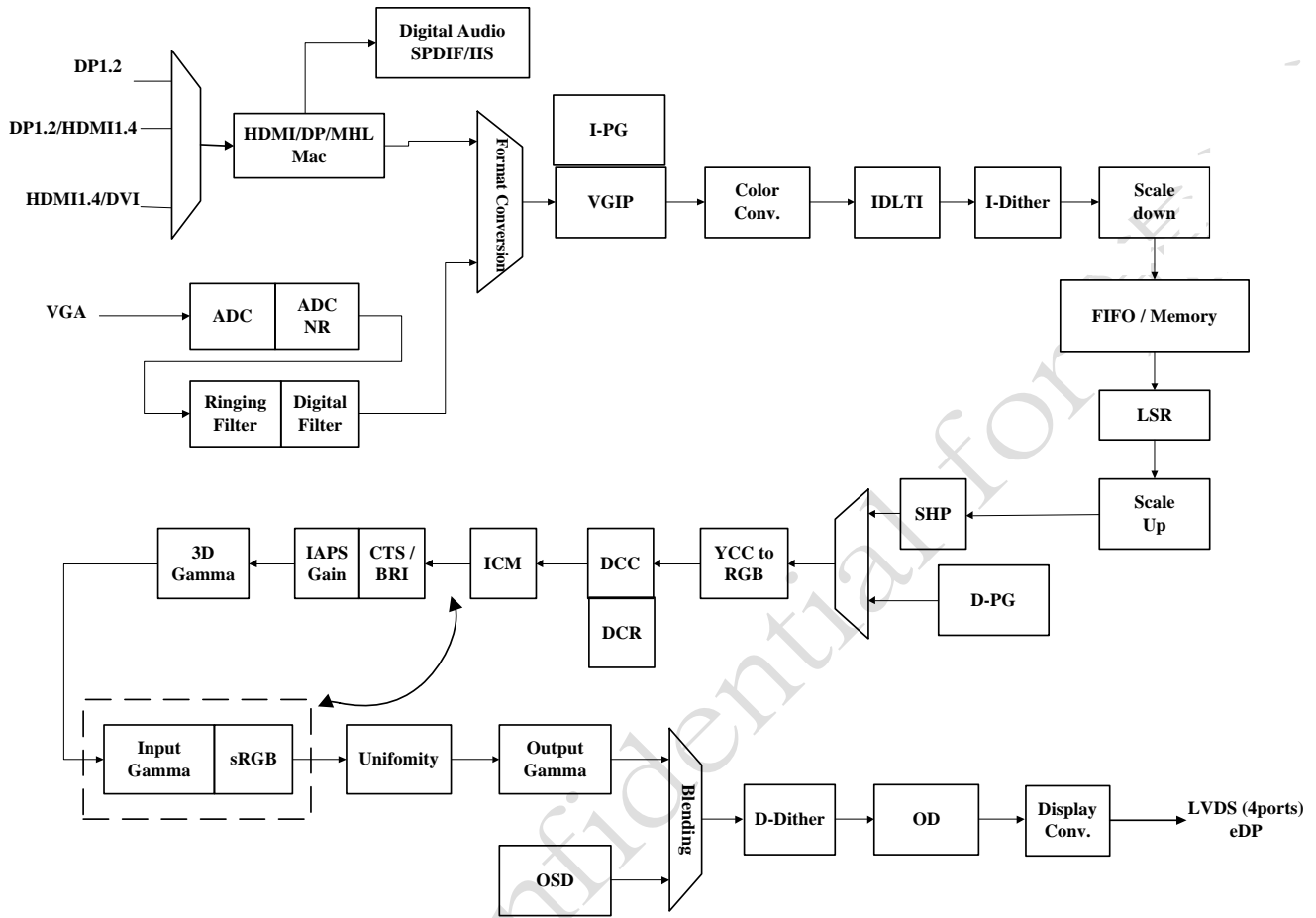


Figure 1. Block Diagram

6. Pin Assignments Table

Table 1. Signals Pin Assignment of LQFP156

(I/O Legend: A = Analog, I = Input, O = Output, P = Power, G = Ground)

Pin Name	I/O	Pin #	Description	Note
DDR1_V25	AP	1	DDR1 2.5V Power	(2.5V)
VCKK_OFF	DP	2	Core Power	(1.1V)
TXD3P_8b	AO	3	LVDS	3.3V Tolerance
TXD3N_8b	AO	4	LVDS	3.3V Tolerance
TXD2P_8b	AO	5	LVDS	3.3V Tolerance
TXD2N_8b	AO	6	LVDS	3.3V Tolerance
TXD1P_8b/ DPTX_LANE_P<3>	AO	7	LVDS/eDP TX	3.3V Tolerance
TXD1N_8b/ DPTX_LANE_N<3>	AO	8	LVDS/eDP TX	3.3V Tolerance
LVDS_VDD11	AP	9	LVDS 1.1V Power	(1.1V)
TXD0P_8b/ DPTX_LANE_P<2>	AO	10	LVDS/eDP TX	3.3V Tolerance
TXD0N_8b/ DPTX_LANE_N<2>	AO	11	LVDS/eDP TX	3.3V Tolerance
LVDS_VDD33	AP	12	LVDS 3.3V Power	(3.3V)
DPTX_LANE_P<1>	AO	13	eDPTX	3.3V Tolerance
DPTX_LANE_N<1>	AO	14	eDPTX	3.3V Tolerance
LVDS_VDD11	AP	15	LVDS 1.1V Power	(1.1V)
TXC3P_8b/ DPTX_LANE_P<0>	AO	16	LVDS/eDP TX	3.3V Tolerance
TXC3N_8b/ DPTX_LANE_N<0>	AO	17	LVDS/eDP TX	3.3V Tolerance
TXCCP_8b	AO	18	LVDS	3.3V Tolerance
TXCCN_8b	AO	19	LVDS	3.3V Tolerance
TXC2P_8b	AO	20	LVDS	3.3V Tolerance
TXC2N_8b	AO	21	LVDS	3.3V Tolerance
TXC1P_8b	AO	22	LVDS	3.3V Tolerance
TXC1N_8b	AO	23	LVDS	3.3V Tolerance
TXC0P_8b	AO	24	LVDS	3.3V Tolerance
TXC0N_8b	AO	25	LVDS	3.3V Tolerance
TXB3P_8b	AIO	26	LVDS	3.3V Tolerance
TXB3N_8b	AIO	27	LVDS	3.3V Tolerance
TXB2P_8b	AIO	28	LVDS	3.3V Tolerance
TXB2N_8b	AIO	29	LVDS	3.3V Tolerance
TXB1P_8b	AIO	30	LVDS	3.3V Tolerance
TXB1N_8b	AIO	31	LVDS	3.3V Tolerance

TXB0P_8b	AIO	32	LVDS	3.3V Tolerance
TXB0N_8b	AIO	33	LVDS	3.3V Tolerance
PVCC	DP	34	Pad Power	(3.3V)
TXA3P_8b	AIO	35	LVDS	3.3V Tolerance
TXA3N_8b	AIO	36	LVDS	3.3V Tolerance
TXACP_8b	AIO	37	LVDS	3.3V Tolerance
TXACN_8b	AIO	38	LVDS	3.3V Tolerance
TXA2P_8b	AIO	39	LVDS	3.3V Tolerance
TXA2N_8b	AIO	40	LVDS	3.3V Tolerance
TXA1P_8b	AIO	41	LVDS	3.3V Tolerance
TXA1N_8b	AIO	42	LVDS	3.3V Tolerance
TXA0P_8b	AIO	43	LVDS	3.3V Tolerance
TXA0N_8b	AIO	44	LVDS	3.3V Tolerance
VCCK_OFF	DP	45	Core Power	(1.1V)
PVCC	DP	46	Pad Power	(3.3V)
USB_SPI_SO/ INT1 / GPIO / T2	IO	47	SPI Serial Data Output / MCU EXINT / MCU GPIO / Timer	5V Tolerance when power off
USB_SPI_CEB0 / IRQB / GPIO / DVS	IO	48	SPI Chip Enable / IRQB / MCU GPIO / DVS	5V Tolerance when power off
USB_SPI_CEB1 / T2EX / GPIO	IO	49	SPI Chip Enable / T2EX / MCU GPIO	5V Tolerance when power off
eDPTX_HPD1 / TCON[8] / GPIO	IO	50	eDPTX_HPD / TCON / MCU GPIO	5V Tolerance when power off
PWM3 / eDPTX_AUX_CH_P_1 / TCON[6] / GPIO	IO	51	PWM / eDPTX_AUX / TCON / MCU GPIO	5V Tolerance when power off
PWM1_0 / eDPTX_AUX_CH_N_1 / TCON[7] / GPIO	IO	52	PWM / eDPTX_AUX / TCON / MCU GPIO	5V Tolerance when power off
DDR1_V25	AP	53	DDR1 2.5V Power	(2.5V)
PWM5 / TCON[2] / GPIO / Test4b	IO	54	PWM / TCON / MCU GPIO / Test4b	5V Tolerance when power off
VCCK_OFF	DP	55	Core Power	(1.1V)
DDR1_V25	AP	56	DDR1 2.5V Power	(2.5V)
SPI_CLK	IO	57	SPI flash serial clock	3.3V Tolerance
SPI_SI	IO	58	SPI flash serial Data Input	3.3V Tolerance
SPI_SO	IO	59	SPI flash serial Data Output	3.3V Tolerance
SPI_CEB	IO	60	SPI flash Chip Enable	3.3V Tolerance
FLASH_WP / GPIO	IO	61	FLASH Write Protect / MCU GPIO	3.3V Tolerance

VCCK_ON	DP	62	Core Power	(1.1V)
PWM2_1 / TCON[1] / IR_RECEIVER / GPIO	IO	63	PWM / TCON / IR Receiver / MCU GPIO	5V Tolerance when power off
TCON[5] / pwm_out / GPIO / Test4b	IO	64	TCON / PWM_OUT / MCU GPIO / Test4b	5V Tolerance when power off
TCON[4] / pwm_in / GPIO / Test4b	IO	65	TCON / PWM_IN / MCU GPIO / Test4b	5V Tolerance when power off
PWM5 / TCON[11] / GPIO	IO	66	PWM / TCON / MCU GPIO	5V Tolerance when power off
IIC_SCL_2 / PWM4 / TCON[11] / GPIO	IO	67	IIC BUS / PWM / TCON / MCU GPIO	5V Tolerance when power off
PWM3 / IIC_SDA_2 / TCON[0] / GPIO	IO	68	PWM / IIC BUS / TCON / MCU GPIO	5V Tolerance when power off
int1 / UART_RX / GPIO / Test4b	IO	69	MCU EXINT / UART RX / MCU GPIO / Test4b	5V Tolerance when power off
int0 / UART_TX / GPIO / Test4b	IO	70	MCU EXINT / UART TX / MCU GPIO / Test4b	5V Tolerance when power off
TCON[13] / GPIO / Test4b / SD0	IO	71	TCON / MCU GPIO / Test4b / I2S	5V Tolerance when power off
TCON[12] / GPIO / Test4b / MCK	IO	72	TCON / MCU GPIO / Test4b / I2S	5V Tolerance when power off
TCON[10] / GPIO / Test4b / SCK	IO	73	TCON / MCU GPIO / Test4b / I2S	5V Tolerance when power off
TCON[9] / GPIO / Test4b / WS	IO	74	TCON / MCU GPIO / Test4b / I2S	5V Tolerance when power off
PVCC	DP	75	Pad Power	(3.3V)
PWM2 / TCON[3] / GPIO	IO	76	PWM / TCON / MCU GPIO	3.3V Tolerance
EI2CSCL / PWM0 / TCON[1] / GPIO	IO	77	EEPROM IIC BUS / PWM / TCON / MCU GPIO	3.3V Tolerance
EI2CSDA / PWM1 / TCON[2] / GPIO	IO	78	EEPROM IIC BUS / PWM / TCON / MCU GPIO	3.3V Tolerance
DDCSCL3 / GPIO	IO	79	DDC Channel (Open drain I/O) / MCU GPIO	5V Tolerance when power off
DDCSDA3 / GPIO	IO	80	DDC Channel (Open drain I/O) / MCU GPIO	5V Tolerance when power off
GPIO / Test4b	IO	81	MCU GPIO / Test4b	5V Tolerance when power off
GPIO / Test4b	IO	82	MCU_GPIO / Test4b	5V Tolerance when power off
TMDS REXT	AI	83	Impedance Match	12K ohm

			Resistor	Reference to GND
GPIO / HDMI_HPD	AIO	84	MCU_GPIO / HDMI Hot-plug	5V Tolerance when power off
RX_33V	AP	85	GDI 3.3V Power	(3.3V)
RXCP_3	-	86	TMDS Differential Signal Input	
RXCN_3	-	87	TMDS Differential Signal Input	
RX2P_3	-	88	TMDS Differential Signal Input	
RX2N_3	-	89	TMDS Differential Signal Input	
TMDS_GND	AG	90	TMDS Ground	
RX1P_3	-	91	TMDS Differential Signal Input	
RX1N_3	-	92	TMDS Differential Signal Input	
RX0P_3	-	93	TMDS Differential Signal Input	
RX0N_3	-	94	TMDS Differential Signal Input	
GDI_11V	AP	95	GDI 1.1V Power	(1.1V)
RX_33V	AP	96	GDI 3.3V Power	(3.3V)
LANE0P_1/RX2P_1	AI	97	DP Differential Signal Input /TMDS Differential Signal Input	
LANE0N_1/RX2N_1	AI	98	DP Differential Signal Input /TMDS Differential Signal Input	
LANE1P_1/RX1P_1	AI	99	DP Differential Signal Input /TMDS Differential Signal Input	
LANE1N_1/RX1N_1	AI	100	DP Differential Signal Input /TMDS Differential Signal Input	
LANE2P_1/RX0P_1	AI	101	DP Differential Signal Input /TMDS Differential Signal Input	
LANE2N_1/RX0N_1	AI	102	DP Differential Signal Input /TMDS Differential Signal Input	
LANE3P_1/RXCP_1	AI	103	DP Differential Signal Input /TMDS Differential Signal Input	

LANE3N_1/RXCN_1	AI	104	DP Differential Signal Input /TMSD Differential Signal Input	
GDI_11V	AP	105	GDI 1.1V Power	(1.1V)
LANE0P_0	AI	106	DP Differential Signal Input	
LANE0N_0	AI	107	DP Differential Signal Input	
DP_GND	AG	108	DP Ground	
LANE1P_0	AI	109	DP Differential Signal Input	
LANE1N_0	AI	110	DP Differential Signal Input	
DP_GND	AG	111	DP Ground	
LANE2P_0	AI	112	DP Differential Signal Input	
LANE2N_0	AI	113	DP Differential Signal Input	
DP_GND	AG	114	DP Ground	
LANE3P_0	AI	115	DP Differential Signal Input	
LANE3N_0	AI	116	DP Differential Signal Input	
GDI_11V	AP	117	GDI 1.1V Power	(1.1V)
TCON[0] / GPIO / Test4b	IO	118	TCON / MCU_GPIO / Test4b	5V Tolerance when power off
TCON[8] / GPIO / Test4b	IO	119	TCON / MCU_GPIO / Test4b	5V Tolerance when power off
ADC_VDD33	AP	120	ADC 3.3V Power	(3.3V)
AVS	AI	121	ADC Vertical Sync Input	5V Tolerance when power off
AHS	AI	122	ADC Horizontal Sync Input	5V Tolerance when power off
B-	AI	123	Negative Blue analog input (Pb-)	3.3V Tolerance
B+	AI	124	Positive Blue analog input (Pb+)	3.3V Tolerance
G-	AI	125	Negative Green analog input (Y-)	3.3V Tolerance
G+	AI	126	Positive Green analog input (Y+)	3.3V Tolerance
SOG	AI	127	Sync-On-Green	3.3V Tolerance
R-	AI	128	Negative RED analog input (Pr-)	3.3V Tolerance

R+	AI	129	Positive RED analog input (Pr+)	3.3V Tolerance
ADC_GND	AG	130	ADC Ground	
DDCSCL_VGA / GPIO	IO	131	DDC VGA (Open drain I/O) / MCU GPIO	5V Tolerance when power off
DDCSDA_VGA / GPIO	IO	132	DDC VGA (Open drain I/O) / MCU GPIO	5V Tolerance when power off
PWM0 / TCON[4] / GPIO / Test4b	IO	133	PWM / TCON / MCU_GPIO / Test4b	5V Tolerance when power off
VCCK_ON	DP	134	Core Power	(1.1V)
DDCSCL_AUXP_D0 / GPIO	IO	135	AUX-CH / MCU GPIO	5V Tolerance when power off
DDCSDA_AUXN_D0 / GPIO	IO	136	AUX-CH / MCU GPIO	5V Tolerance when power off
DDCSCL1 / DDCSCL_AUXP_D1 / GPIO	IO	137	DDC Channel (Open drain I/O) / DPRX AUX-CH / MCU GPIO	5V Tolerance when power off
DDCSDA1 / DDCSDA_AUXN_D1 / GPIO	IO	138	DDC Channel (Open drain I/O) / DPRX AUX-CH / MCU GPIO	5V Tolerance when power off
PVCC	AP	139	3.3V Power	(3.3V)
XI	AI	140	Crystal Input	3.3V Tolerance
XO	AO	141	Crystal Output	3.3V Tolerance
DDR1_V25	AP	142	DDR1 2.5V Power	(2.5V)
A-ADC0/ INT0 / GPIO / Test4b	AIO	143	5bits MCU ADC Input / MCU EXINT / MCU GPIO / Test4b	3.3 V tolerance when using ADC Input; 5V Tolerance power on when using GPIO
A-ADC1 / INT1 / GPIO / Test4b	AIO	144	5bits MCU ADC Input / MCU EXINT / MCU GPIO / Test4b	3.3 V tolerance when using ADC Input; 5V Tolerance power on when using GPIO
PVCC	DP	145	Pad Power	(3.3V)
VCCK_ON	DP	146	Core Power	(1.1V)
AUDIO_HOUTL / SD2 / SPDIF2 / GPIO	AIO	147	AUDIO_HOUTL / I2S / SPDIF / MCU GPIO	3.3V Tolerance
AUDIO_HOUTR / SD3 / SPDIF3 / GPIO	AIO	148	AUDIO_HOUTL / I2S / SPDIF / MCU GPIO	3.3V Tolerance
AUDIO_HP_GND	AG	149	AUDIO HP Ground	
AUDIO_HP_AVDD33	AP	150	AUDIO HP 3.3V Power	(3.3V)
LINE_INL / WS / GPIO	AIO	151	LINE_INL / I2S / MCU	3.3V Tolerance

			GPIO	
LINE_INR / SCK / GPIO	AIO	152	LINE_INR / I2S / MCU GPIO	3.3V Tolerance
AUDIO_REF / MCK / GPIO	AIO	153	AUDIO_REF / I2S / MCU GPIO	3.3V Tolerance
AUDIO_SOUTL / SD0 / SPDIF0 / GPIO	AIO	154	AUDIO_SOUTL / I2S / SPDIF / MCU GPIO	3.3V Tolerance
AUDIO_SOUTR / SD1 / SPDIF1 / GPIO	AIO	155	AUDIO_SOUTR / I2S / SPDIF / MCU GPIO	3.3V
AUDIO_VDD33	AP	156	Audio DAC 3.3V Power	(3.3V

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7. Electrical Specifications

Electrical Specifications

LQFP156 DC Characteristics (RTD2256QR-VL-CG Series)

7.1. Recommended Operating Conditions

Table 2. Recommended Operating Conditions of LQFP156

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Voltage on Input (5V tolerance)	V _{IN}	-1		5.3	V
Supply Voltage	PVCC	3.14	3.30	3.47	V
DDR Voltage	2.5V_DDR	2.38	2.5	2.63	V
Core Power On Voltage	VCCK_ON	1.05	1.1	1.16	V
Core Power Off Voltage	VCCK_OFF	1.05	1.1	1.16	V
Electrostatic Discharge	V _{ESD}			±2.5	kV
Latch-Up	I _{LA}			±100	mA
Ambient Operating Temperature	T _A	0		70	°C
Storage Temperature (plastic)	T _{STG}	-55		125	°C
Thermal Resistance (Junction to Air)	θ _{JA}		25.2		°C/W
Thermal Resistance (Junction to Case)	θ _{JC}		11.7		°C/W
Junction Acceptable Temperature	T _j			125	°C

7.2. Absolute Maximum Ratings

Table 3. Absolute Maximum Ratings of LQFP156

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Supply Voltage	PVCC			3.6	V
Supply Voltage	VCCK			1.21	V
Storage Temperature (plastic)	T _{STG}			150	°C
Junction Acceptable Temperature	T _j			150	°C

Note : Operation under the absolute maximum ratings does not imply well-functioning. Long-term stress to the absolute maximum ratings would probably affect the device reliability or further cause permanent damage.

7.3. Reset Period

Table 4. Reset Period of LQFP156

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Reset Pulse Period	Trst-en ¹	1120			ns
Power-on-Reset Period	Tpor-rst ²	145	146.5	148	ms

1. $16 * Xtal_cycle(1/14.3Mhz)$

2. $65536*16*2*Xtal_cycle(1/14.3Mhz)$

Table 5. Mechanical Specification of LQFP156 Leads

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A ₁	0.05	—	0.15	0.002	—	0.006
A ₂	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
D	21.90	22.00	22.10	0.862	0.866	0.870
E	15.90	16.00	16.10	0.626	0.630	0.634
D ₁	19.90	20.00	20.10	0.783	0.787	0.791
E ₁	13.90	14.00	14.10	0.547	0.551	0.555
D ₂	7.85	8.10	8.35	0.309	0.319	0.329
E ₂	7.30	7.55	7.80	0.287	0.297	0.307
e	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		

Notes :

1. CONTROLLING DIMENSION : MILLIMETER(mm).
2. REFERENCE DOCUMENTL : JEDEC MS-26.

9. Ordering Information

Table 6. Ordering Information

Part No.	Max. Resolution	Input : VGA	Input : DP1.2	Input : DP1.2/ HDMI1.4	Input : HDMI1.4/ DVI	Output : LVDS	FRC	OD	PKG
RTD2556QR -VL-CG	2560x1600 @60Hz	•	1 Ports	1 Ports	1 Ports	•	N/A	•	LQFP156

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