REALTEK

RTL8201FI-VC-CG

SINGLE-CHIP/PORT 10/100M ETHERNET PHYCEIVER WITH AUTO MDIX

DATASHEET

(CONFIDENTIAL: Development Partners Only)

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REALTEK

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2011/12/06	First release.
1.1	2015/03/11	Corrected Figure 3 Pin Assignments, page 5 (Corrected the package marking from RTL8201FI to 8201FI.)

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1. General Description

The RTL8201FI-VC-CG is a single-chip/single-port 10/100Mbps Ethernet PHYceiver that supports:

- MII (Media Independent Interface)
- RMII (Reduced Media Independent Interface)

The RTL8201FI-VC implements all 10/100M Ethernet Physical-layer functions including the Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA), Twisted Pair Physical Medium Dependent Sublayer (TP-PMD), 10Base-TX Encoder/Decoder, and Twisted-Pair Media Access Unit (TPMAU). The RTL8201FI-VC also supports auto MDIX.

A PECL (Pseudo Emitter Coupled Logic) interface is supported to connect with an external 100Base-FX fiber optical transceiver. The chip utilizes an advanced CMOS process to meet low voltage and low power requirements. With on-chip DSP (Digital Signal Processing) technology, the chip provides excellent performance under all operating conditions.

2. Features

- Supports IEEE 802.3az-2010 (EEE)
- 100Base-TX IEEE 802.3u Compliant
- 10Base-T IEEE 802.3 Compliant
- Supports MII mode
- Supports RMII mode
- Full/half duplex operation
- Twisted pair or fiber mode output
- Supports Auto-Negotiation
- Supports power down mode
- Supports Link Down Power Saving
- Supports Base Line Wander (BLW) compensation
- Supports auto MDIX
- Supports Interrupt function
- Supports Wake-On-LAN (WOL)
- Adaptive Equalization
- Automatic Polarity Correction
- Provides two network status LEDs
- Supports 25MHz external crystal or OSC
- Supports 50MHz external OSC Clock input
- Provides 50MHz clock source for MAC
- Low power supply 1.1V and 3.3V; 1.1V is generated by an internal regulator
- 0.11µm CMOS process
- 32-pin MII/RMII QFN 'Green' package

3. Applications

- DTV (Digital TV)
- MAU (Media Access Unit)
- CNR (Communication and Network Riser)
- Game Console
- Printer and Office Machine
- DVD Player and Recorder
- Ethernet Hub
- Ethernet Switch

In addition, the RTL8201FI-VC can be used in any embedded system with an Ethernet MAC that needs a UTP physical connection or Fiber PECL interface to an external 100Base-FX optical transceiver module.

3.1. Application Diagram

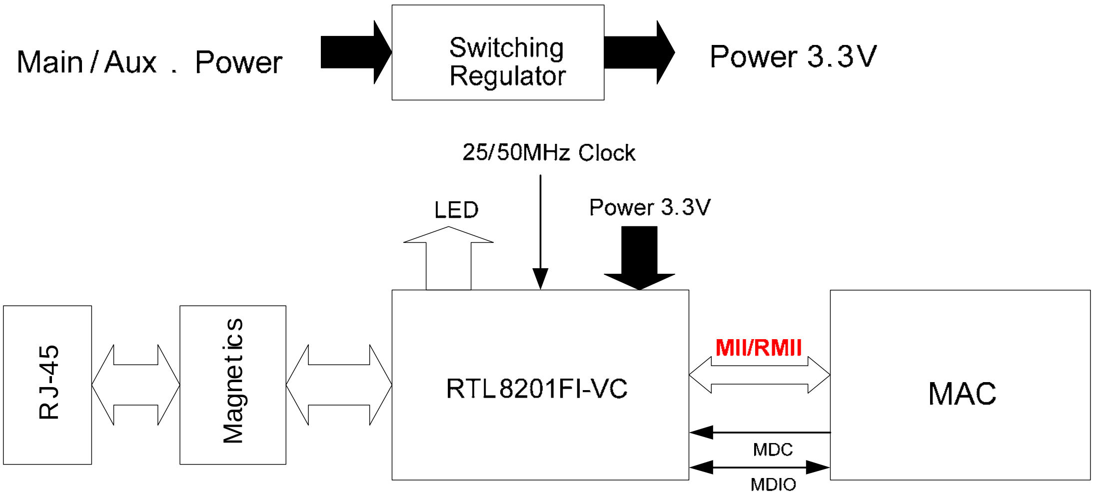


Figure 1. Application Diagram

4. Block Diagram

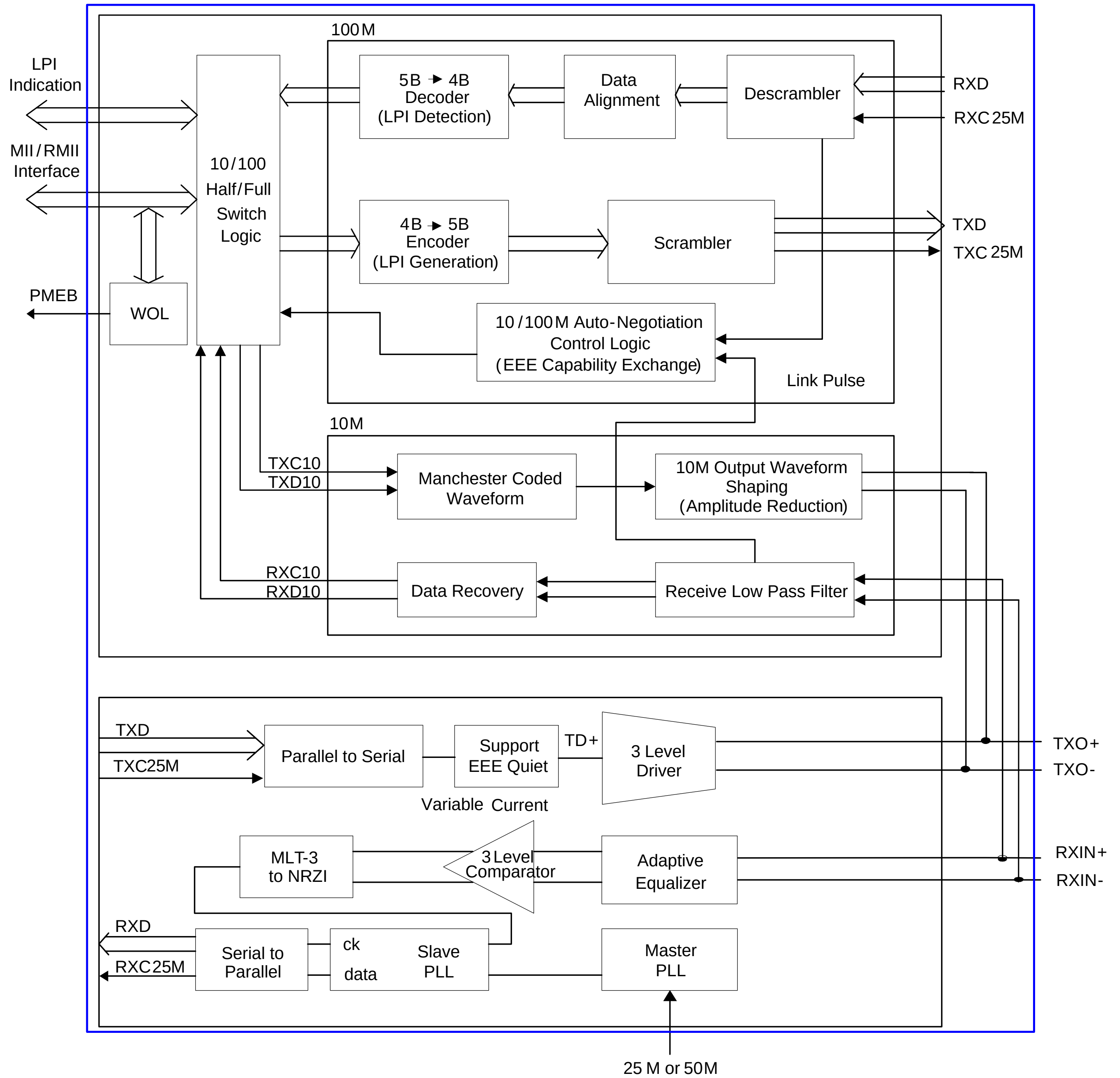


Figure 2. Block Diagram

5. Pin Assignments

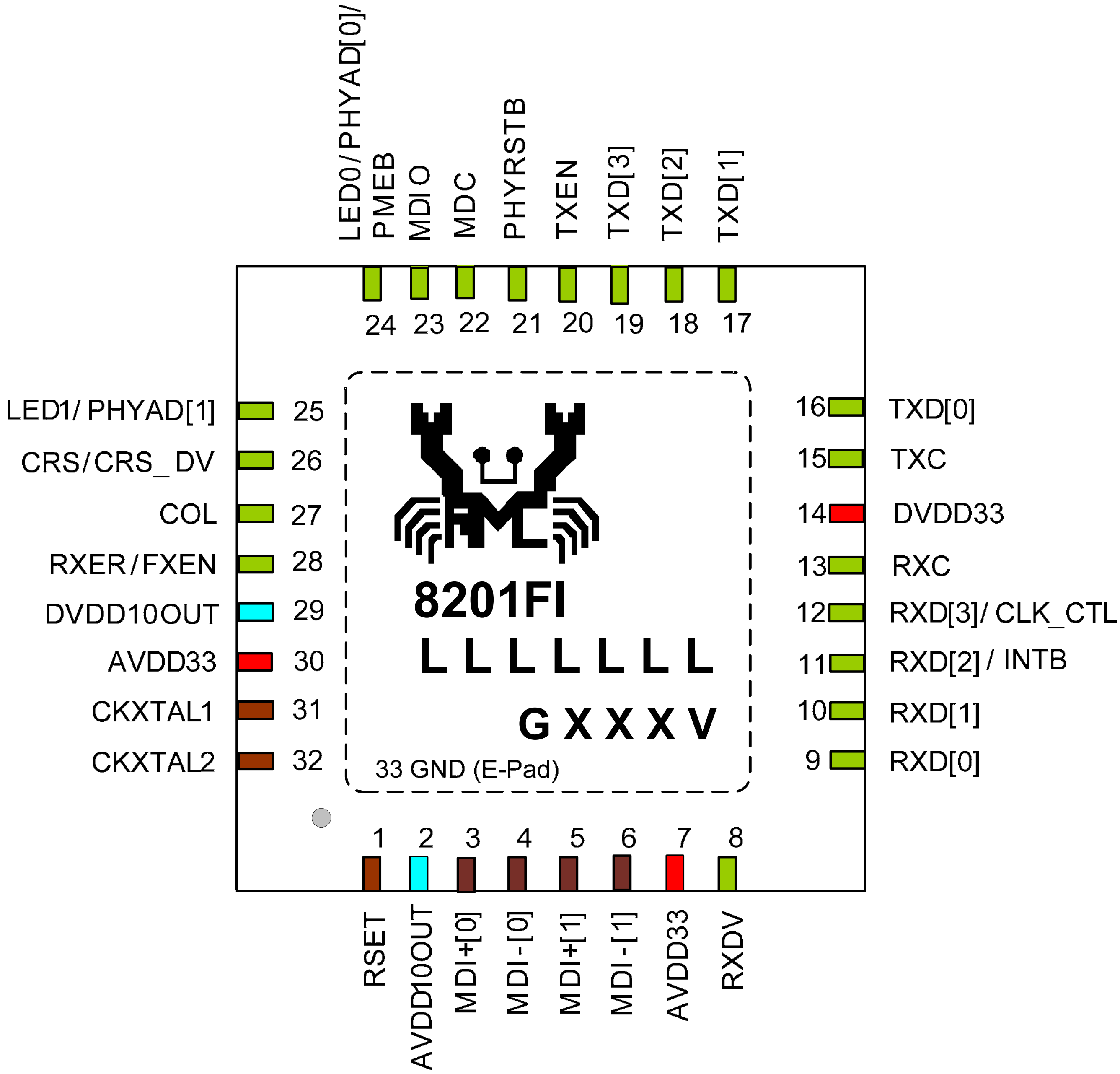


Figure 3. Pin Assignments

5.1. Green Package and Version Identification

Green package is indicated by the 'G' in GXXXV (Figure 3). The version is shown in the location marked 'V'.

6. Pin Descriptions

I:	Input	LI:	Latched Input during Power up or Reset
O:	Output	IO:	Bi-directional Input and Output
P:	Power	HZ:	High Impedance During Power On Reset
PU:	Internal Pull Up During Power On Reset	PD:	Internal Pull Down During Power On Reset
OD:	Open Drain Output		

6.1. MII Interface

Table 1. MII Interface

Name	Type	Pin No.	Description
TXC	O/PD	15	Transmit Clock. This pin provides a continuous clock as a timing reference for TXD [3:0] and TXEN signals. TXC is 25MHz in 100Mbps mode and 2.5MHz in 10Mbps mode.
TXEN	I/PD	20	Transmit Enable. The input signal indicates the presence of valid nibble data on TXD [3:0]. An internal weakly pulled low resistor prevents the bus floating.
TXD[0] TXD[1] TXD[2] TXD[3]	I/PD I/PD I/PD I/PD	16 17 18 19	Transmit Data. The MAC will source TXD [0:3] synchronous with TXC when TXEN is asserted. An internal weakly pulled low resistor prevents the bus floating.
RXC	O/PD	13	Receive Clock. This pin provides a continuous clock reference for RXDV and RXD [0:3] signals. RXC is 25MHz in 100Mbps mode and 2.5MHz in 10Mbps mode.
COL	O/PD	27	Collision Detect. COL is asserted high when a collision is detected on the media.
CRS/ CRS_DV	O/PD	26	Carrier Sense. This pin's signal is asserted high if the media is not in Idle state.
RXDV	LI/O/PD	8	Receive Data Valid. This pin's signal is asserted high when received data is present on the RXD[3:0] lines. The signal is de-asserted at the end of the packet. The signal is valid on the rising edge of the RXC. This pin should be pulled low when operating in MII mode. 0: MII mode 1: RMII mode An internal weakly pulled low resistor sets this to the default of MII mode. It is possible to use an external 4.7KΩ pulled high resistor to enable RMII mode. After power on, the pin operates as the Receive Data Valid pin.

Name	Type	Pin No.	Description
RXD[0] RXD[1] RXD[2]/ INTB	O/PD LI/O/PD O/PD	9 10 11	Receive Data. These are the four parallel receive data lines aligned on the nibble boundaries driven synchronously to the RXC for reception by the external physical unit (PHY). *Note 1: An internal weakly pulled low resistor sets RXD[1] to the LED function (default). Use an external 4.7KΩ pulled high resistor to enable the WOL function.* *Note 2: The Pin11 is named RXD[2]/INTB. When in RMII mode, this pin is used for the interrupt function. See Table 9, page 11 for INTB descriptions.*
RXD[3]/ CLK_CTL	LI/O/PD	12	Receive Data. This is the parallel receive data line aligned on the nibble boundaries driven synchronously to the RXC for reception by the external physical unit (PHY). RXD[3]/CLK_CTL pin is the Hardware strap in RMII Mode. 1: REF_CLK input mode 0: REF_CLK output mode *Note: An internal weakly pulled low resistor sets RXD[3]/CLK_CTL to REF_CLK output mode (default).*
RXER/ FXEN	LI/O/PD	28	Receive Error. If a 5B decode error occurs, such as invalid /J/K/, invalid /T/R/, or invalid symbol, this pin will go high. Fiber/UTP Enable. This pin's status is latched at power on reset to determine the media mode to operate in. 1: Fiber mode 0: UTP mode An internal weakly pulled low resistor sets this to the default of UTP mode. It is possible to use an external 4.7KΩ pulled high resistor to enable fiber mode. After power on, the pin operates as the Receive Error pin.

6.2. Serial Management Interface

Table 2. Serial Management Interface

Name	Type	Pin No.	Description
MDC	I/PU	22	Management Data Clock. This pin provides a clock synchronous to MDIO, which may be asynchronous to the transmit TXC and receive RXC clocks. The clock rate can be up to 2.5MHz. Use an internal weakly pulled high resistor to prevent the bus floating.
MDIO	IO/PU	23	Management Data Input/Output. This pin provides the bi-directional signal used to transfer management information.

6.3. RMII Interface

Table 3. RMII Interface

Name	Type	Pin No.	Description
TXC	IO/PD	15	Synchronous 50MHz Clock Reference for Receive, Transmit, and Control Interface. The direction is decided by Page 7, Register 16. The default direction is reference clock output mode if RXD[3]/CLK_CTL pin floating.
CRS/CRS_DV	O/PD	26	Carrier Sense/Receive Data Valid. CRS_DV shall be asserted by the PHY when the receive medium is non-idle.
TXEN	I/PD	20	Transmit Enable.
TXD[0:1]	I/PD	16, 17	Transmit Data.
RXD[0:1]	O/PD	9, 10	Receive Data.
RXER/FXEN	LI/O/PD	28	Receive Error. RX_ER is a required output of the PHY, but is an optional input for the MAC.

6.4. Clock Interface

Table 4. Clock Interface

Name	Type	Pin No.	Description
CKXTAL2	IO	32	25MHz Crystal Output. This pin provides the 25MHz crystal output. If an external 25MHz/50MHz oscillator or clock is used, connect CKXTAL2 to the oscillator or clock output (see section 9.4 Oscillator Requirements, page 50).
CKXTAL1	I	31	25MHz Crystal Input. This pin provides the 25MHz crystal input. Must be shorted to GND when an external 25MHz/50MHz oscillator or clock drives CKXTAL2.

6.5. 10Mbps/100Mbps Network Interface

Table 5. 10Mbps/100Mbps Network Interface

Name	Type	Pin No.	Description
MDI+[0] MDI-[0]	IO	3 4	Transmit Output. Differential transmit output pair shared by 100Base-TX, 100Base-FX, and 10Base-T modes. When configured as 100Base-TX, output is an MLT-3 encoded waveform. When configured as 100Base-FX, the output is pseudo-ECL level.
MDI+[1] MDI-[1]	IO	5 6	Receive Input. Differential receive input pair shared by 100Base-TX, 100Base-FX, and 10Base-T modes.

6.6. *Transmit Bias Reference*

Table 6. Transmit Bias Reference

Name	Type	Pin No.	Description
RSET	I	1	Transmit Bias Resistor Connection. This pin should be pulled to GND by a 2.49KΩ (1%) resistor to define driving current for the transmit DAC.

6.7. *Device Configuration Interface*

Table 7. Device Configuration Interface

<table>
<tr><th>Name</th><th>Type</th><th>Pin No.</th><th>Description</th></tr>
<tr><td>RXDV</td><td>LI/O/PD</td><td>8</td><td>Receive Data Valid.
This pin’s signal is asserted high when received data is present on the RXD [3:0] lines. The signal is de-asserted at the end of the packet. The signal is valid on the rising edge of the RXC.
This pin should be pulled low when operating in MII mode.
0: MII mode
1: RMII mode
An internal weakly pulled low resistor sets this to the default of MII mode. It is possible to use an external 4.7KΩ pulled high resistor to enable RMII mode.
After power on, the pin operates as the Receive Data Valid pin.</td></tr>
<tr><td>RXD[1]</td><td>LI/O/PD</td><td>10</td><td>An internal weakly pulled low resistor sets RXD[1] to the LED function (default). Use an external 4.7KΩ pulled high resistor to enable the WOL function for the RTL8201FI-VC.</td></tr>
<tr><td>LED0/
PHYAD[0]/
PMEB

LED1/
PHYAD[1]</td><td>LI/O/PU

LI/O/PD</td><td>24

25</td><td>PHY Address and Customized LED Settings.
The default available PHY addresses is 00000~00011.
Traditional LED Function Selection
<table>
<tr><th>LED_Sel</th><th>00</th><th>01</th><th>10</th><th>11</th></tr>
<tr><td>LED0</td><td>ACT$_{ALL}$</td><td>Link$_{ALL}$/ACT$_{ALL}$</td><td>Link$_{10}$/ACT$_{ALL}$</td><td>LINK$_{10}$/ACT$_{10}$</td></tr>
<tr><td>LED1</td><td>LINK$_{100}$</td><td>LINK$_{100}$</td><td>LINK$_{100}$</td><td>LINK$_{100}$/ACT$_{100}$</td></tr>
</table>
Note 1: For Customized LED Settings, see section 7.17, page 20.
Note 2: LED_Sel default is 11. Refer to section 7.19, page 21.

An internal weakly pulled low resistor sets RXD[1] to the LED function (default).
Use an external 4.7KΩ pulled high resistor to enable the WOL function.
Traditional LED Function Selection with WOL Enabled
With the WOL function enabled, the PHY address must be 00001 or 00011.
<table>
<tr><th>LED_Sel</th><th>00</th><th>01</th><th>10</th><th>11</th></tr>
<tr><td>LED1</td><td>LINK$_{100}$</td><td>LINK$_{100}$</td><td>LINK$_{100}$</td><td>LINK$_{100}$/ACT$_{100}$</td></tr>
</table></td></tr>
</table>

Name	Type	Pin No.	Description
RXD[3]/ CLK_CTL	LI/O/PD	12	Receive Data. This is the parallel receive data line aligned on the nibble boundaries driven synchronously to the RXC for reception by the external physical unit (PHY). RXD [3]/CLK_CTL pin is the Hardware strap in RMII Mode. 1: REF_CLK input mode 0: REF_CLK output mode *Note: An internal weakly pulled low resistor sets RXD[3]/CLK_CTL to REF_CLK output mode (default).*
RXER/ FXEN	LI/O/PD	28	Fiber/UTP Interface. This pin's status is latched at power on reset to determine the media mode to operate in. 1: Fiber mode 0: UTP mode An internal weakly pulled low resistor sets this to the default of UTP mode. It is possible to use an external 4.7KΩ pulled high resistor to enable fiber mode.

6.8. Power and Ground Pins

Table 8. Power and Ground Pins

Name	Type	Pin No.	Description
AVDD33	P	7, 30	3.3V Analog Power Input. 3.3V power supply for analog circuit; should be well decoupled.
DVDD33	P	14	3.3V Digital Power Input. 3.3V power supply for digital circuit.
AVDD10OUT	O	2	Power Output. Be sure to connect a 0.1µF ceramic capacitor for decoupling purposes. The connection method is outlined in section 8.8 3.3V Power Supply and Voltage Conversion Circuit, page 35.
DVDD10OUT	O	29	Power Output. Be sure to connect a 0.1µF ceramic capacitor for decoupling purposes. The connection method is outlined in 8.8 3.3V Power Supply and Voltage Conversion Circuit, page 35.
GND	P	E-PAD	Ground. Should be connected to a larger GND plane. Exposed Pad (E-Pad) is Analog and Digital Ground.

6.9. Reset and Other Pins

Table 9. Reset and Other Pins

Name	Type	Pin No.	Description
PHYRSTB	I/HZ	21	RESETB. Set low to reset the chip. For a complete reset, this pin must be asserted low for at least 10ms. *Note: When the WOL function is enabled, keep the pin high.*
RXD[2]/INTB	O/PD	11	Interrupt. Set low if link status changed, duplex changed, or auto negotiation failed. Active Low. This pin is an open-drain design and should be pulled high by an external 4.7KΩ. If not used, keep floating. *Note: This pin is used for the interrupt function only when in the RMII mode.*
PMEB	O/OD	24	Power Management Enable. Set low if received a magic packet or wake up frame; active low.

7. Register Descriptions

This section describes the functions and usage of the registers available in this file. In this section the following abbreviations are used.

RW:	Read/Write	RW/EFUS:	Read/Write/eFUSE Burnable
RO:	Read Only	RW/LI:	Read/Write/Latch In
RC:	Read Clear	RW/SC:	Read/Write/Self-Clearing
SC:	Self-Clear		

Note: RW/EFUS and RW/LI types will return to default values after a software reset (set Reg.0 Bit15 to 1).

7.1. Register 0 Basic Mode Control Register

Table 10. Register 0 Basic Mode Control Register

Address	Name	Description	Mode	Default
0:15	Reset	This bit sets the status and control registers of the PHY in the default state. This bit is self-clearing. 1: Software reset 0: Normal operation Register 0 and register 1 will return to default values after a software reset (set Bit15 to 1). This action may change the internal PHY state and the state of the physical link associated with the PHY.	RW/ SC	0
0:14	Loopback	This bit enables loopback of transmit data nibbles TXD3:0 to the receive data path. 1: Enable loopback 0: Normal operation	RW	0
0:13	Speed Selection	This bit sets the network speed. 1: 100Mbps 0: 10Mbps After completing auto negotiation, this bit will reflect the speed status. 1: 100Base-T 0: 10Base-T When 100Base-FX mode is enabled, this bit=1 and is read only.	RW	1
0:12	Auto Negotiation Enable	This bit enables/disables the NWay auto-negotiation function. 1: Enable auto-negotiation; bits 0:13 and 0:8 will be ignored 0: Disable auto-negotiation; bits 0:13 and 0:8 will determine the link speed and the data transfer mode, respectively When 100Base-FX mode is enabled, this bit=0 and is read only.	RW	1
0:11	Power Down	This bit turns down the power of the PHY chip, including the internal crystal oscillator circuit. The MDC, MDIO is still alive for accessing the MAC. 1: Power down 0: Normal operation	RW	0
0:10	Isolate	1: Electrically isolate the PHY from MII/GMII/RGMII/RSGMII. PHY is still able to respond to MDC/MDIO. 0: Normal operation	RW	0

Address	Name	Description	Mode	Default
0:9	Restart Auto Negotiation	This bit allows the NWay auto-negotiation function to be reset. 1: Re-start auto-negotiation 0: Normal operation	RW/ SC	0
0:8	Duplex Mode	This bit sets the duplex mode if auto-negotiation is disabled (bit 0:12=0). 1: Full duplex 0: Half duplex After completing auto-negotiation, this bit will reflect the duplex status. 1: Full duplex 0: Half duplex	RW	1
0:7	Collision Test	Collision Test. 1: Collision test enabled 0: Normal operation When set, this bit will cause the COL signal to be asserted in response to the TXEN assertion within 512-bit times. The COL signal will be de-asserted within 4-bit times in response to the TXEN de-assertion.	RW	0
0:6	Speed Selection[1]	Speed Select Bit 1. Refer to bit 0.13.	RW	0
0:5~0	Reserved	Reserved.	-	-

7.2. Register 1 Basic Mode Status Register

Table 11. Register 1 Basic Mode Status Register

Address	Name	Description	Mode	Default
1:15	100Base-T4	1: Enable 100Base-T4 support 0: Suppress 100Base-T4 support	RO	0
1:14	100Base_TX_FD	1: Enable 100Base-TX full duplex support 0: Suppress 100Base-TX full duplex support	RO	1
1:13	100Base_TX_HD	1: Enable 100Base-TX half duplex support 0: Suppress 100Base-TX half duplex support	RO	1
1:12	10Base_T_FD	1: Enable 10Base-T full duplex support 0: Suppress 10Base-T full duplex support	RO	1
1:11	10_Base_T_HD	1: Enable 10Base-T half duplex support 0: Suppress 10Base-T half duplex support	RO	1
1:10~7	Reserved	Reserved.	-	-
1:6	MF Preamble Suppression	The RTL8201FI-VC will accept management frames with preamble suppressed. A minimum of 32 preamble bits are required for the first management interface read/write transaction after reset. One idle bit is required between any two management transactions as per IEEE 802.3u specifications.	RO	1
1:5	Auto Negotiation Complete	1: Auto-negotiation process completed 0: Auto-negotiation process not completed	RO	0
1:4	Remote Fault	1: Remote fault condition detected (cleared on read) 0: No remote fault condition detected When in 100Base-FX mode, this bit means an in-band signal Far-End-Fault has been detected (see 8.10 Far End Fault Indication, page 36).	RC	0

Address	Name	Description	Mode	Default
1:3	Auto-Negotiation Ability	1: PHY is able to perform auto-negotiation 0: PHY is not able to perform auto-negotiation	RO	1
1:2	Link Status	1: Valid link established 0: No valid link established This bit indicates whether the link was lost since the last read. For the current link status, read this register twice.	RO	0
1:1	Jabber Detect	1: Jabber condition detected 0: No jabber condition detected	RO	0
1:0	Extended Capability	1: Extended register capable (permanently=1) 0: Not extended register capable	RO	1

7.3. Register 2 PHY Identifier Register 1

Table 12. Register 2 PHY Identifier Register 1

Address	Name	Description	Mode	Default
2:15~0	OUI	Composed of the 6th to 21st bits of the Organizationally Unique Identifier (OUI), respectively.	RO	001Ch

7.4. Register 3 PHY Identifier Register 2

Table 13. Register 3 PHY Identifier Register 2

Address	Name	Description	Mode	Default
3:15~10	OUI_LSB	Assigned to the 0 through 5th bits of the OUI.	RO	110010
3:9~4	Model Number	Model Number	RO	000001
3:3~0	Revision Number	Revision Number	RO	0110

7.5. Register 4 Auto-Negotiation Advertisement Register (ANAR)

This register contains the advertised abilities of this device as they will be transmitted to its link partner during auto-negotiation.

Table 14. Register 4 Auto-Negotiation Advertisement Register (ANAR)

Address	Name	Description	Mode	Default
4:15	Next Page	Next Page Bit. 0: Transmitting the primary capability data page 1: Transmitting the protocol specific data page	RW	0
4:14	Acknowledge	1: Acknowledge reception of link partner capability data word 0: Do not acknowledge reception	RO	0
4:13	Remote Fault	1: Advertise remote fault detection capability 0: Do not advertise remote fault detection capability	RW	0
4:12	Reserved	Reserved.	-	-
4:11	Asymmetric PAUSE	1: Advertise asymmetric pause support 0: No support of asymmetric pause	RW	0
4:10	Pause	Reserved.	RW	0

Address	Name	Description	Mode	Default
4:9	100Base-T4	1: 100Base-T4 is supported by local node 0: 100Base-T4 not supported by local node	RO	0
4:8	100Base-TX-FD	1: 100Base-TX full duplex is supported by local node 0: 100Base-TX full duplex not supported by local node	RW	1
4:7	100Base-TX	1: 100Base-TX is supported by local node 0: 100Base-TX not supported by local node	RW	1
4:6	10Base-T-FD	1: 10Base-T full duplex supported by local node 0: 10Base-T full duplex not supported by local node	RW	1
4:5	10Base-T	1: 10Base-T is supported by local node 0: 10Base-T not supported by local node	RW	1
4:4~0	Selector Field	Binary Encoded Selector Supported by This Node. Currently only CSMA/CD 00001 is specified. No other protocols are supported.	RO	00001

7.6. Register 5 Auto-Negotiation Link Partner Ability Register (ANLPAR)

This register contains the advertised abilities of the Link Partner as received during auto-negotiation. The content changes after a successful auto-negotiation if Next-pages are supported.

Table 15. Register 5 Auto-Negotiation Link Partner Ability Register (ANLPAR)

Address	Name	Description	Mode	Default
5:15	Next Page	Next Page Bit. 0: Transmitting the primary capability data page 1: Transmitting the protocol specific data page	RO	0
5:14	Acknowledge	1: Link partner acknowledges reception of local node's capability data word 0: No acknowledgement	RO	0
5:13	Remote Fault	1: Link partner is indicating a remote fault 0: Link partner is not indicating a remote fault	RO	0
5:12	Reserved	Reserved.	-	-
5:11	Asymmetric Pause	1: Asymmetric Flow control supported by Link Partner 0: No Asymmetric flow control supported by Link Partner When auto-negotiation is enabled, this bit reflects Link Partner ability.	RO	0
5:10	Pause	1: Flow control supported by Link Partner 0: No flow control supported by Link Partner When auto-negotiation is enabled, this bit reflects Link Partner ability (read only).	RO	0
5:9	100Base-T4	1: 100Base-T4 is supported by link partner 0: 100Base-T4 not supported by link partner	RO	0
5:8	100Base-TX-FD	1: 100Base-TX full duplex is supported by link partner 0: 100Base-TX full duplex not supported by link partner	RO	0

Address	Name	Description	Mode	Default
5:7	100Base-TX	1: 100Base-TX is supported by link partner 0: 100Base-TX not supported by link partner This bit will also be set if the link in 100Base-TX is established by parallel detection.	RO	0
5:6	10Base-T-FD	1: 10Base-T full duplex is supported by link partner 0: 10Base-T full duplex not supported by link partner	RO	0
5:5	10Base-T	1: 10Base-T is supported by link partner 0: 10Base-T not supported by link partner This bit will also be set if the link in 10Base-T is established by parallel detection.	RO	0
5:4~0	Selector Field	Link Partner's Binary Encoded Node Selector. Currently only CSMA/CD 00001 is specified.	RO	00001

7.7. Register 6 Auto-Negotiation Expansion Register (ANER)

This register contains additional status for NWay auto-negotiation.

Table 16. Register 6 Auto-Negotiation Expansion Register (ANER)

Address	Name	Description	Mode	Default
6:15~5	Reserved	Reserved.	-	-
6:4	Parallel Detection Fault	1: A fault has been detected via the Parallel Detection function 0: No fault has been detected via the Parallel Detection function	RC	0
6:3	Link Partner Next Page Ability	1: Link Partner is Next Page able 0: Link Partner is not Next Page able	RO	0
6:2	Local Next Page Ability	1: Next Page is able 0: Not Next Page able	RO	0
6:1	Page Received	1: A New Page has been received 0: A New Page has not been received	RC	0
6:0	Link Partner Auto-Negotiation Ability	If Auto-Negotiation is Enabled, This Bit Means: 1: Link Partner is Auto-Negotiation able 0: Link Partner is not Auto-Negotiation able	RO	0

7.8. Page 0 Register 13 MACR (MMD Access Control Register; Address 0x0D)

Table 17. Page 0 Register 13 MACR (MMD Access Control Register; Address 0x0D)

Bit	Name	RW	Default	Description
13.15:14	Function	WO	0	00: Address 01: Data; no post increment 10: Data; post increment on reads and writes 11: Data; post increment on writes only
13.13:5	RSVD	RO	000000000	Reserved.
13.4:0	DEVAD	WO	0	Device Address.

Note 1: Used in conjunction with the MAADR (Register 14) to provide access to the MMD address space.
Note 2: If the access of MAADR is for address (Function=00) then it is directed to the address register within the MMD associated with the value in the DEVAD field.
Note 3: If the access of MAADR is for data (Function=00) then both the DEVAD field and the MMD address register direct the MAADR data accesses to the appropriate registers within the MMD.

7.9. Page 0 Register 14 MAADR (MMD Access Address Data Register; Address 0x0E)

Table 18. Page 0 Register 14 MAADR (MMD Access Address Data Register; Address 0x0E)

Bit	Name	RW	Default	Description
14.15:0	Address Data	RW	0x0000	13.15:14=00 → MMD DEVAD's address register 13.15:14=01, 10, or 11 → MMD DEVAD's data register as indicated by the contents of its address register

Note: Used in conjunction with the MACR (Register 13) to provide access to the MMD address space.

7.10. Register 24 Power Saving Mode Register (PSMR)

Table 19. Register 24 Power Saving Mode Register (PSMR)

Address	Name	Description	Mode	Default
24:15	Enpwrsave	Enable Power Saving Mode. The bit will return to default value by software reset.	RW	1
24:14~0	Reserved	Reserved.	-	-

Note: If the REF_CLK output is needed in RMII output mode, LDPS (Link Down Power Saving) must be disabled (see Table 42, page 33).

7.11. Register 28 Fiber Mode and Loopback Register

Table 20. Register 28 Fiber Mode and Loopback Register

Address	Name	Description	Mode	Default
28:15~6	Reserved	Reserved.	-	-
28:5	Fxmode	Enable Fiber Mode.	RW	0
28:4~3	Reserved	Reserved.	-	-
28:2	En_autoMDIX	Enable Auto MDIX Function.	RW	1
28:1	Force_MDI	Force MDI/MDIX Mode. If enable auto MDIX function is disabled: 1: Force MDI 0: Force MDIX	RW	1
28:0	Reserved	Reserved.	-	-

7.12. Register 30 Interrupt Indicators and SNR Display Register

Table 21. Register 30 Interrupt Indicators and SNR Display Register

Address	Name	Description	Mode	Default
30:15	Anerr	Auto-Negotiation Error Interrupt. 1: Enable 0: Disable	RC	0
30:14	Spdchg	Speed Mode Change Interrupt. 1: Enable 0: Disable	RC	0
30:13	Duplexchg	Duplex Mode Change Interrupt. 1: Enable 0: Disable	RC	0
30:12	Reserved	Reserved.	-	-
30:11	Linkstatuschg	Link Status Change Interrupt. 1: Enable 0: Disable	RC	0
30:10~4	Reserved	Reserved.	-	-
30:3~0	SNR_O	These 4-Bits Show the Signal to Noise Ratio Value.	RO	0000

7.13. Register 31 Page Select Register

Table 22. Register 31 Page Select Register

Address	Name	Description	Mode	Default
31:15~8	Reserved	Reserved for Internal Testing.	-	-
31:7~0	PAGE SEL	Select Page Address: 00000000~11111111.	RW	00000000

7.14. Page 4 Register 16 EEE Capability Enable Register

Table 23. Page4 Register 16 EEE Capability Enable Register

Address	Name	Description	Mode	Default
16:15~14	Reserved	Reserved.	-	-
16:13	EEE_10_cap	Enable EEE 10M Capability.	RW	1
16:12	EEE_nway_en	Enable Next Page Exchange in NWay for EEE 100M.	RW/ EFUS	1
16:11~10	Reserved	Reserved.	-	-
16:9	Tx_quiet_en	Enable Ability to Turn Off Power 100TX when TX in Quiet State. This bit is recommended to be set to 1 when EEE is enabled.	RW/ EFUS	1
16:8	Rx_quiet_en	Enable Ability to Turn Off Power 100RX when RX in Quiet state. This bit is recommended to be set to 1 when EEE is enabled.	RW/ EFUS	1
16:7:0	Reserved	Reserved.	-	-

7.15. Page 4 Register 21 EEE Capability Register

Table 24. Page4 Register 21 EEE Capability Register

Address	Name	Description	Mode	Default
21:15~13	Reserved	Reserved.	-	-
21:12	Rg_dis_ldvt	Set to 1 to Disable the Line Driver of the Analog Circuit.	RW	0
21:11~1	Reserved	Reserved.	-	-
21:0	EEE_100_cap	NWay Result to Indicate Link Partner Supports EEE 100M.	RO	0

7.16. Page 7 Register 16 RMII Mode Setting Register (RMSR)

Table 25. Page7 Register 16 RMII Mode Setting Register (RMSR)

Address	Name	Description	Mode	Default
16:15~13	Reserved	Reserved.	-	-
16:12	Rg_rmii_clkdir	This Bit Sets the Type of TXC in RMII Mode. 0: Output 1: Input	RW/LI	0
16:11~8	Rg_rmii_tx_offset	Adjust RMII TX Interface Timing.	RW/EFUS	1111
16:7~4	Rg_rmii_rx_offset	Adjust RMII RX Interface Timing.	RW/EFUS	1111
16:3	RMII Mode	0: MII Mode 1: RMII Mode	RW/LI	0
16:2	Rg_rmii_rxdv_sel	0: CRS/CRS_DV pin is CRS_DV signal 1: CRS/CRS_DV pin is RXDV signal	RW/EFUS	0
16:1	Rg_rmii_rxdsel	0: RMII data only 1: RMII data with SSD Error	RW/EFUS	1
16:0	Reserved	Reserved.	-	-

Note: Set Page7, Register 16 to '7FFB' when an external clock (25MHz and 50MHz) inputs to the CKXTAL2 pin.

7.17. Page 7 Register 17 Customized LEDs Setting Register

This register is for setting customized LEDs. Table 26 shows the customized LED matrix table.

Table 26. Customized LED Matrix Table

	LINK		ACT
	10M	100M	
LED0	Bit0	Bit1	Bit3
LED1	Bit4	Bit5	Bit7

LED Pin	ACT=0	ACT=1
LINK=0	Floating	All Speed ACT
LINK>0	Selected Speed LINK	Selected Speed LINK+ACT

Table 27. Page7 Register 17 Customized LEDs Setting Register

Address	Name	Description	Mode	Default
17:15~8	Reserved	Reserved.	-	-
17:7~4	LED_sel1	Customized LED1 Setting. Set Bit3 (Page7 Register 19; Table 29, page 21) to 1 to enable customized LED function.	RW/ EFUS	0000
17:3~0	LED_sel0	Customized LED0 Setting. Set Bit3 (Page7 Register 19; Table 29, page 21) to 1 to enable customized LED function.	RW/ EFUS	0000

7.18. Page 7 Register 18 EEE LEDs Enable Register

Table 28. Page7 Register 18 EEE LEDs Enable Register

Address	Name	Description	Mode	Default
18:15~2	Reserved	Reserved.	-	-
18:1	EEE_LED_en1	Enable LED1 in EEE/LPI Mode.	RW	0
18:0	EEE_LED_en0	Enable LED0 in EEE/LPI Mode.	RW	0

7.19. Page 7 Register 19 Interrupt, WOL Enable, and LEDs Function Registers

Table 29. Page7 Register 19 Interrupt, WOL Enable, and LEDs Function Registers

<table>
<tr><th>Address</th><th>Name</th><th>Description</th><th>Mode</th><th>Default</th></tr>
<tr><td>19:15~14</td><td>Reserved</td><td>Reserved.</td><td>-</td><td>-</td></tr>
<tr><td>19:13</td><td>Int_linkchg</td><td>Link Change Interrupt Mask.
1: Interrupt pin Enable
0: Interrupt pin Disable
This bit set to 0 only masks the link change interrupt event in the INTB pin. Reg30 Bit11 always reflects the link change interrupt behavior (see Table 21, page 18).</td><td>RW</td><td>0</td></tr>
<tr><td>19:12</td><td>Int_dupchg</td><td>Duplex Change Interrupt Mask.
1: Interrupt pin Enable
0: Interrupt pin Disable
This bit set to 0 only masks the duplex change interrupt event in the INTB pin. Reg30 Bit13 always reflects the duplex change interrupt behavior (see Table 21, page 18).</td><td>RW</td><td>0</td></tr>
<tr><td>19:11</td><td>Int_anerr</td><td>NWay Error Interrupt Mask.
1: Interrupt pin Enable
0: Interrupt pin Disable
This bit set to 0 only masks the NWay Error interrupt event in the INTB pin.Reg30 Bit15 always reflects the NWay Error interrupt behavior (see Table 21, page 18).</td><td>RW</td><td>0</td></tr>
<tr><td>19:10</td><td>Rg_led0_wol_sel</td><td>LED and Wake-On-LAN Function Selection.
1: Wake-On-LAN Function Enable
0: LED Function Enable
An internal weakly pulled low resistor sets RXD[1] to the LED function (default). Use an external 4.7KΩ pulled high resistor to enable the WOL function for the RTL8201FI-VC.</td><td>RW/LI</td><td>0</td></tr>
<tr><td>19:9~6</td><td>Reserved</td><td>Reserved.</td><td>-</td><td>-</td></tr>
<tr><td>19:5~4</td><td>LED_sel[1:0]</td><td>Traditional LED Function Selection.
<table>
<tr><th>LED_sel</th><th>00</th><th>01</th><th>10</th><th>11</th></tr>
<tr><td>LED0</td><td>ACT_{ALL}</td><td>$Link_{ALL}$/
ACT_{ALL}</td><td>$Link_{10}$/
ACT_{ALL}</td><td>$LINK_{10}$/
ACT_{10}</td></tr>
<tr><td>LED1</td><td>$LINK_{100}$</td><td>$LINK_{100}$</td><td>$LINK_{100}$</td><td>$LINK_{100}$/
ACT_{100}</td></tr>
</table></td><td>RW/
EFUS</td><td>11</td></tr>
<tr><td>19:3</td><td>Customized_LED</td><td>Customized LED Enable.
1: Customized LED function enable
0: Customized LED function disable
See the section 8.4.7 Customized LED, page 32 for detail.</td><td>RW/
EFUS</td><td>0</td></tr>
<tr><td>19:2~1</td><td>Reserved</td><td>Reserved.</td><td>-</td><td>-</td></tr>
<tr><td>19:0</td><td>En10mlpi</td><td>Enable 10M LPI LED Function.</td><td>RW</td><td>0</td></tr>
</table>

7.20. Page 7 Register 20 MII TX Isolate Register

Table 30. Page7 Register 20 MII TX Isolate Register

Address	Name	Description	Mode	Default
20:15	Rg_tx_isolate_en	Isolate MII TX Path Signals when TX Idle.	RW	0
20:14~0	Reserved	Reserved.	-	-

7.21. Page 7 Register 24 Spread Spectrum Clock Register

Table 31. Page7 Register 24 Spread Spectrum Clock Register

Address	Name	Description	Mode	Default
24:15~1	Reserved	Reserved.	-	-
24:0	Rg_dis_ssc	0: SSC function is enabled 1: SSC function is disabled	RW	0

7.22. MMD Register Mapping and Definition

Note: MMD registers are placed at Page 0 Register 13 and Register 14.

Table 32. MMD Register Mapping and Definition

Device	Offset	Access	Name	Description
3	0	RW	EEEPC1R	EEE PCS Control 1 Register
3	1	RO/ RO, LH	EEEPS1R	EEE PCS Status Control 1 Register
3	20	RO	EEECR	EEE Capability Register
3	22	RC	EEEWER	EEE Wake Error Register
7	60	RW	EEEAR	EEE Advertisement Register
7	61	RO	EEELPAR	EEE Link Partner Ability Register

Note: LH: Latching High.

7.22.1. EEEPC1R (PCS Control 1 Register, MMD Device 3, Address 0x00)

Table 33. EEEPC1R (PCS Control 1 Register, MMD Device 3, Address 0x00)

Bit	Name	RW	Default	Description
3.0.15:11	RSVD	RW	0	Reserved.
3.0.10	Clock Stop Enable	RW	0	1: PHY stops RXC in LPI 0: RXC not stoppable
3.0.9:0	RSVD	RW	0	Reserved.

7.22.2. EEEPS1R (PCS Status 1 Register, MMD Device 3, Address 0x01)

Table 34. EEEPS1R (PCS Status 1 Register, MMD Device 3, Address 0x01)

Bit	Name	RW	Default	Description
3.1.15:12	RSVD	RO	0	Reserved.
3.1.11	TX LPI Received	RO, LH	0	1: TX PCS has received LPI 0: LPI not received
3.1.10	RX LPI Received	RO, LH	0	1: RX PCS has received LPI 0: LPI not received
3.1.9	TX LPI Indication	RO	0	1: TX PCS is currently receiving LPI 0: TX PCS is not currently receiving LPI
3.1.8	RX LPI Indication	RO	0	1: RX PCS is currently receiving LPI 0: RX PCS is not currently receiving LPI
3.1.7	RSVD	RO	0	Reserved.
3.1.6	Clock Stop Capable	RO	1	1: MAC stops TXC in LPI 0: TXC not stoppable
3.1.5:0	RSVD	RO	0	Reserved.

7.22.3. EEECR (EEE Capability Register, MMD Device 3; Address 0x14)

Table 35. EEECR (EEE Capability Register, MMD Device 3; Address 0x14)

Bit	Name	RW	Default	Description
3.20.15:2	RSVD	RO	0	Reserved.
3.20.1	100Base-TX EEE	RO	1	1: EEE is supported for 100Base-TX EEE 0: EEE is not supported for 100Base-TX EEE
3.20.0	RSVD	RO	1	Reserved.

7.22.4. EEEWER (EEE Wake Error Register, MMD Device 3; Address 0x16)

Table 36. EEEWER (EEE Wake Error Register, MMD Device 3; Address 0x16)

Bit	Name	RW	Default	Description
3.22.15:0	EEE Wake Error Counter	RC	0	Used by PHY types that support EEE to count wake time faults where the PHY fails to complete its normal wake sequence within the time required for the specific PHY type.

7.22.5. EEEAR (EEE Advertisement Register, MMD Device 7; Address 0x3c)

Table 37. EEEAR (EEE Advertisement Register, MMD Device 7; Address 0x3c)

Bit	Name	RW	Default	Description
7.60.15:3	RSVD	RW	0	Reserved.
7.60.1	100Base-TX EEE	RW	1	Advertise 100Base-TX EEE Capability. 1: Advertise 0: Do not advertise
7.60.0	RSVD	RW	0	Reserved.

7.22.6. EEELPAR (EEE Link Partner Ability Register, MMD Device 7; Address 0x3d)

Table 38. EEELPAR (EEE Link Partner Ability Register, MMD Device 7; Address 0x3d)

Bit	Name	RW	Default	Description
7.61.15:3	RSVD	RO	0	Reserved.
7.61.1	LP 100Base-TX EEE	RO	0	1: Link Partner is capable of 100Base-TX EEE 0: Link Partner is not capable of 100Base-TX EEE
7.61.0	RSVD	RO	0	Reserved.

8. Functional Description

The RTL8201FI-VC PHYceiver is a physical layer device that integrates 10Base-T and 100Base-TX/100Base-FX functions, and some extra power management features. This device supports the following functions:

- MII interface with MDC/MDIO management interface to communicate with the MAC
- IEEE 802.3u clause 28 Auto-Negotiation ability
- Speed, duplex, auto-negotiation ability configurable by hard wire or MDC/MDIO
- Power Down mode support
- 4B/5B transform
- Scrambling/De-scrambling
- NRZ to NRZI, NRZI to MLT-3
- Manchester Encode and Decode for 10Base-T operation
- Clock and Data recovery
- Adaptive Equalization
- Automatic Polarity Correction
- Far End Fault Indication (FEFI) in fiber mode
- Network status LEDs
- Wake-On-LAN (WOL)
- Energy Efficient Ethernet (EEE)
- Spread Spectrum Clock (SSC) for RMII REF_CLK output mode

8.1. MII and Management Interface

8.1.1. Data Transition

The MII (Media Independent Interface) is an 18-signal interface (as described in IEEE 802.3u) supplying a standard interface between the PHY and MAC layer.

This interface operates at two frequencies, 25MHz and 2.5MHz, to support 100Mbps/10Mbps bandwidth for both transmit and receive functions.

Transmission

The MAC asserts the TXEN signal. It then changes byte data into 4-bit nibbles and passes them to the PHY via TXD[3:0]. The PHY will sample TXD[3:0] synchronously with TXC – the transmit clock signal supplied by the PHY – during the interval TXEN is asserted.

Reception

The PHY asserts the RXDV signal. It passes the received nibble data RXD[3:0] clocked by RXC. CRS and COL signals are used for collision detection and handling.

In 100Base-TX mode, when the decoded signal in 5B is not IDLE, the CRS signal will assert. When 5B is recognized as IDLE it will be de-asserted. In 10Base-T mode, CRS will assert when the 10M preamble has been confirmed and will be de-asserted when the IDLE pattern has been confirmed.

The RXDV signal will be asserted when decoded 5B are /J/K/ and will be de-asserted if the 5B are /T/R/ or IDLE in 100Mbps mode. In 10Mbps mode, the RXDV signal is the same as the CRS signal.

The RXER (Receive Error) signal will be asserted if any 5B decode errors occur, e.g., an invalid J/K, invalid T/R, or invalid symbol. This pin will go high for one or more clock periods to indicate to the reconciliation sublayer that an error was detected somewhere in the frame.

8.1.2. Serial Management Interface

The MAC layer device can use the MDC/MDIO management interface to control a maximum of four devices, configured with different PHY addresses (00b to 11b without WOL). Frames transmitted on the MDC/MDIO Management Interface should have the frame structure shown in Table 39.

Table 39. Management Frame Format

	Management Frame Fields							
	Preamble	**ST**	**OP**	**PHYAD**	**REGAD**	**TA**	**DATA**	**IDLE**
Read	1…1	01	10	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDD	Z
Write	1…1	01	01	AAAAA	RRRRR	10	DDDDDDDDDDDDDDDD	Z

During a hardware reset, the logic levels of pins 24 and 25 are latched to be set as the PHY address for management communication via the serial interface. The read and write frame structure for the management interface is illustrated in Figure 4 and Figure 5, page 27.

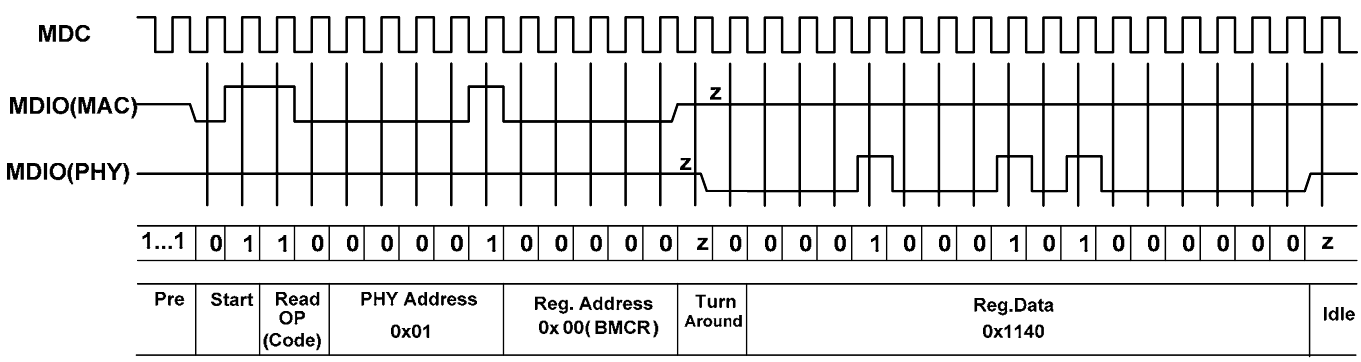


Figure 4. Read Cycle

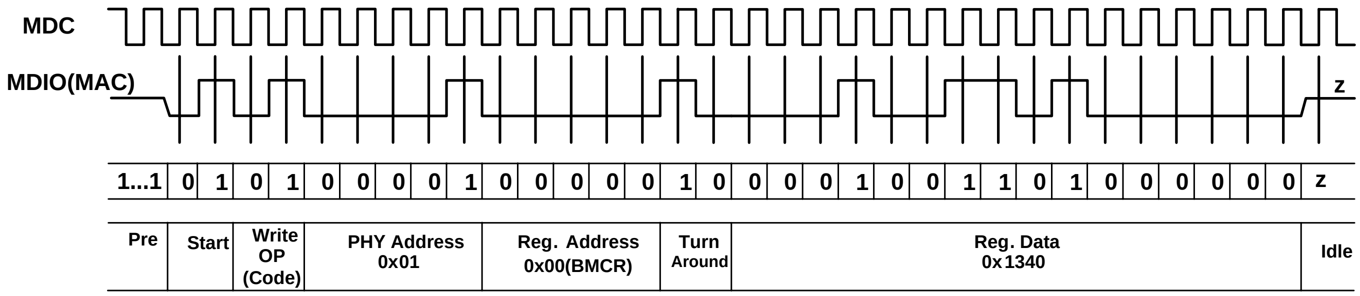


Figure 5. Write Cycle

Table 40. Serial Management

Name	Description
Preamble	32 Contiguous Logical 1's sent by the MAC on MDIO, along with 32 Corresponding Cycles on MDC. This provides synchronization for the PHY.
ST	Start of Frame. Indicated by a 01 pattern.
OP	Operation Code. Read: 10 Write: 01
PHYAD	PHY Address. Up to 4 PHYs can be connected to one MAC. This 2-bit field selects which PHY the frame is directed to.
REGAD	Register Address. This is a 5-bit field that sets which of the 32 registers of the PHY this operation refers to.
TA	Turnaround. This is a 2-bit-time spacing between the register address and the data field of a frame to avoid contention during a read transaction. For a read transaction, both the STA and the PHY remain in a high-impedance state for the first bit time of the turnaround. The PHY drives a zero bit during the second bit time of the turnaround of a read transaction.
DATA	Data. These are the 16 bits of data.
IDLE	Idle Condition. Not truly part of the management frame. This is a high impedance state. Electrically, the PHY's pull-up resistor will pull the MDIO line to a logical '1'.

8.2. Interrupt

Whenever there is a status change on the media detected by the RTL8201FI-VC, they will drive the interrupt pin (INTB) low to issue an interrupt event. The MAC senses the status change and accesses the page0 register30 through the MDC/MDIO interface in response.

Once these status registers page0 register30 have been read by the MAC through the MDC/MDIO, the INTB is de-asserted.

Note 1: The RXD[2]/INTB pin (Pin11) is used for the interrupt function only when in the RMII mode.
Note 2: The Interrupt function is disabled by default. To enable this function, refer to Table 29, page 21 (Page7 Register 19 Bit[13:11]).

8.3. Auto-Negotiation and Parallel Detection

The RTL8201FI-VC supports IEEE 802.3u clause 28 Auto-negotiation for operation with other transceivers supporting auto-negotiation. The RTL8201FI-VC can auto-detect the link partner's abilities and determine the highest speed/duplex configuration possible between the two devices. If the link partner does not support auto-negotiation, then the RTL8201FI-VC will enable half-duplex mode and enter parallel detection mode. The RTL8201FI-VC will default to transmitting FLP (Fast Link Pulse) and wait for the link partner to respond. If the RTL8201FI-VC receives a FLP, then the auto-negotiation process will continue. If it receives an NLP (Normal Link Pulse), then the RTL8201FI-VC will change to 10Mbps and half-duplex mode. If it receives a 100Mbps IDLE pattern, it will change to 100Mbps and half-duplex mode.

8.3.1. Setting the Medium Type and Interface Mode to MAC

Table 41. Setting the Medium Type and Interface Mode to MAC

FXEN	RXDV	Operation Mode
H	L	Fiber Mode and MII Mode
H	H	Fiber Mode and RMII Mode
H	X	Fiber Mode and MII Mode
L	L	UTP Mode and MII Mode
L	H	UTP Mode and RMII Mode
L	X	UTP Mode and MII Mode

8.4. LED Functions

The RTL8201FI-VC supports two LED signals in four configurable operation modes. The following sections describe the various LED actions.

8.4.1. LED and PHY Address

As the PHYAD strap options share the LED output pins, the external combinations required for strapping and LED usage must be considered in order to avoid contention. Specifically, when the LED outputs are used to drive LEDs directly, the active state of each output driver is dependent on the logic level sampled by the corresponding PHYAD input upon power-up/reset.

For example, as Figure 6 (left-side) shows, if a given PHYAD input is resistively pulled high then the corresponding output will be configured as an active low driver. On the right side, we can see that if a given PHYAD input is resistively pulled low then the corresponding output will be configured as an active high driver. The PHY address configuration pins should not be connected to GND or VCC directly, but must be pulled high or low through a resistor (e.g., 4.7KΩ). If no LED indications are needed, the components of the LED path (LED+510Ω) can be removed.

PHY Address[:] = Logical 1 PHY Address[:] = Logical 0

LED Indication = Active low LED Indication = Active high

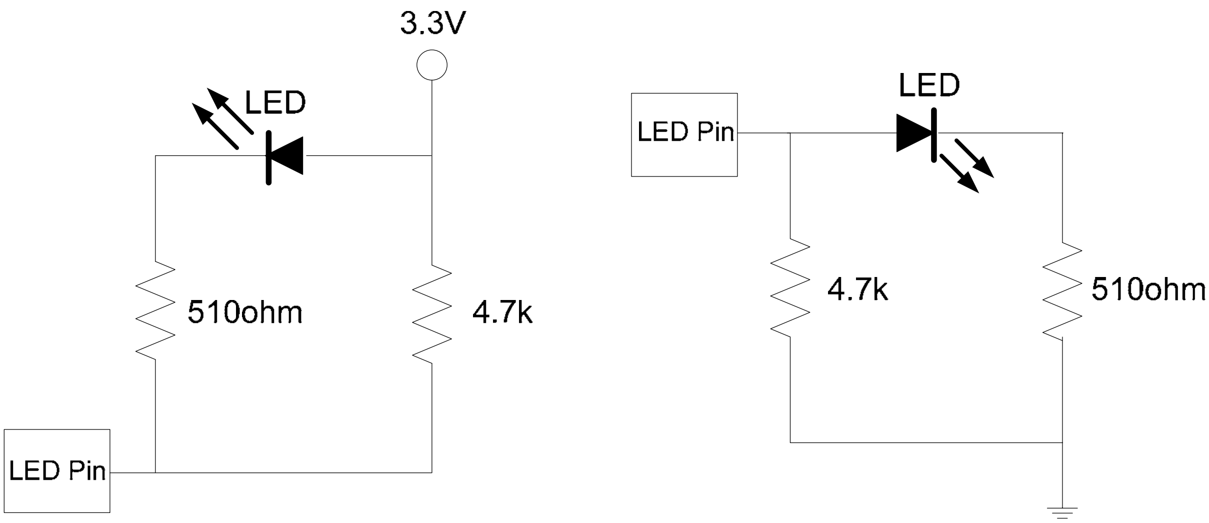


Figure 6. LED and PHY Address Configuration

8.4.2. Link Monitor

The Link Monitor senses link integrity, such as $LINK_{10}$, $LINK_{100}$, $LINK_{10}$/ACT, or $LINK_{100}$/ACT. Whenever link status is established, the specific link LED pin is driven low. Once a cable is disconnected, the link LED pin is driven high, indicating that no network connection exists.

8.4.3. RX LED

In 10/100M mode, blinking of the RX LED indicates that receive activity is occurring.

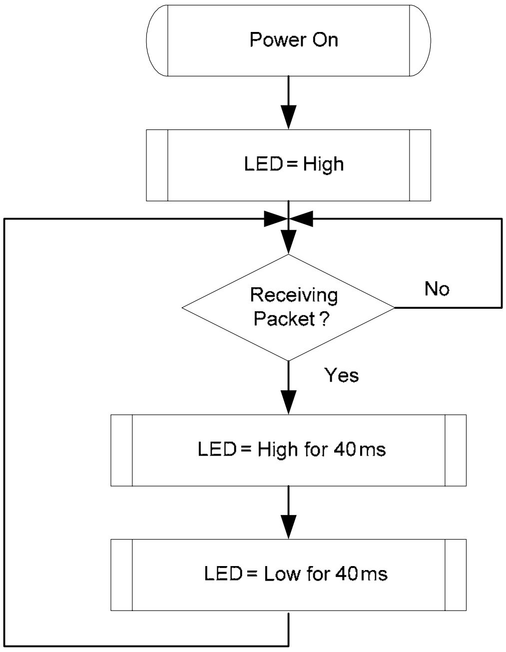


Figure 7. RX LED

8.4.4. TX LED

In 10/100M mode, blinking of the TX LED indicates that transmit activity is occurring.

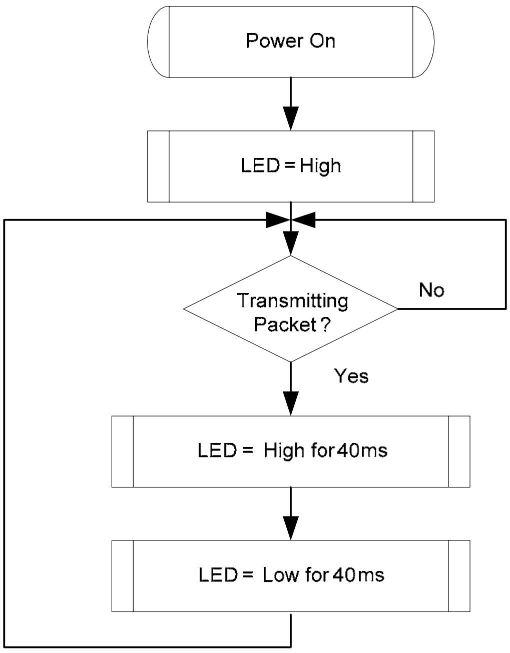


Figure 8. TX LED

8.4.5. TX/RX LED

In 10/100M mode, blinking of the TX/RX LED indicates that both transmit and receive activity is occurring.

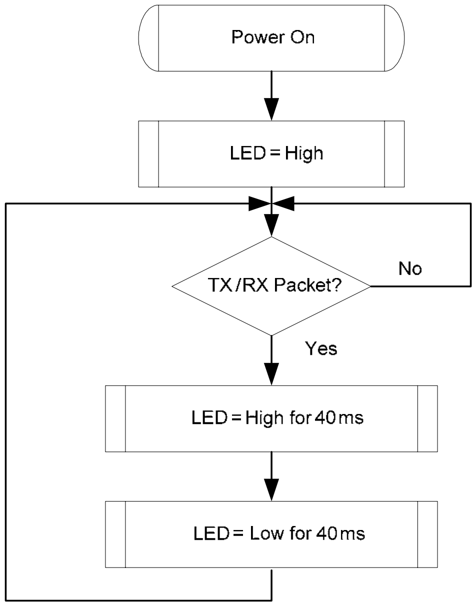


Figure 9. TX/RX LED

8.4.6. LINK/ACT LED

In 10/100M mode, blinking of the LINK/ACT LED indicates that the RTL8201FI-VC is linked and operating properly. When this LED is high for extended periods, it indicates that a link problem exists.

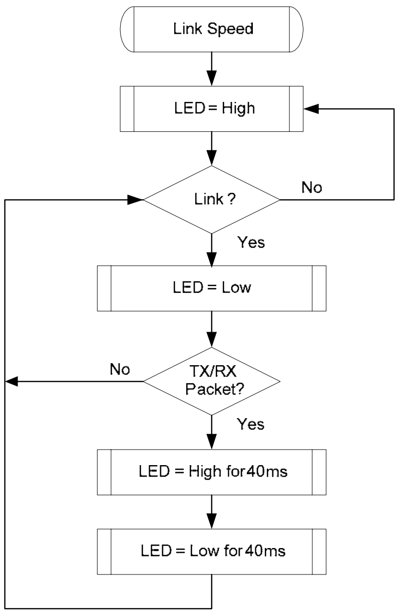


Figure 10. LINK/ACT LED

8.4.7. Customized LED

The RTL8201FI-VC supports programmable LEDs in 10/100Mbps mode. This function can be enabled/disabled via page7, reg19[3] register (Figure 11).

Refer to section 7.17, page 20 for customized LED register setting.

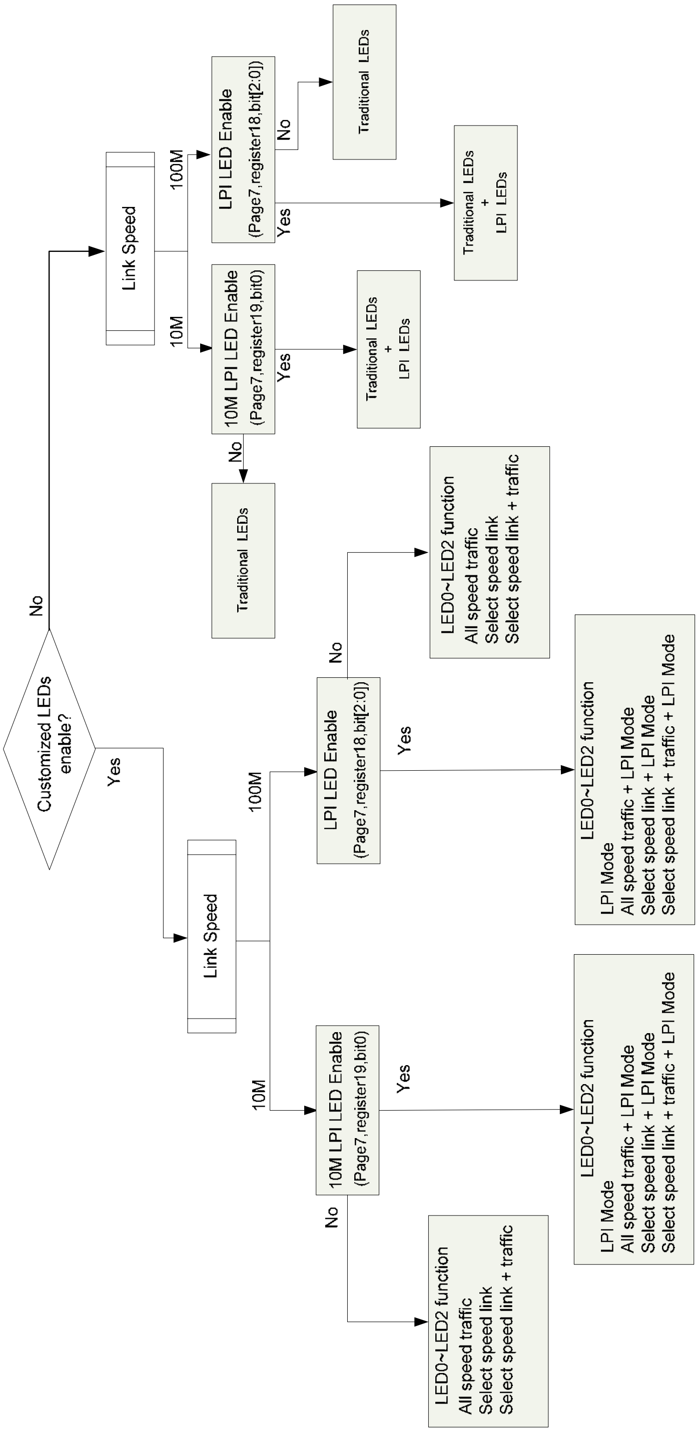


Figure 11. Customized LED with/without LPI LED Mode

8.4.8. EEE LED Behavior

EEE Idle mode: LED continuous slow blinking.

EEE Active mode: LED fast and slow blinking (on packet transmission and reception).

Refer to Table 28, page 20 for EEE LED enable setting.

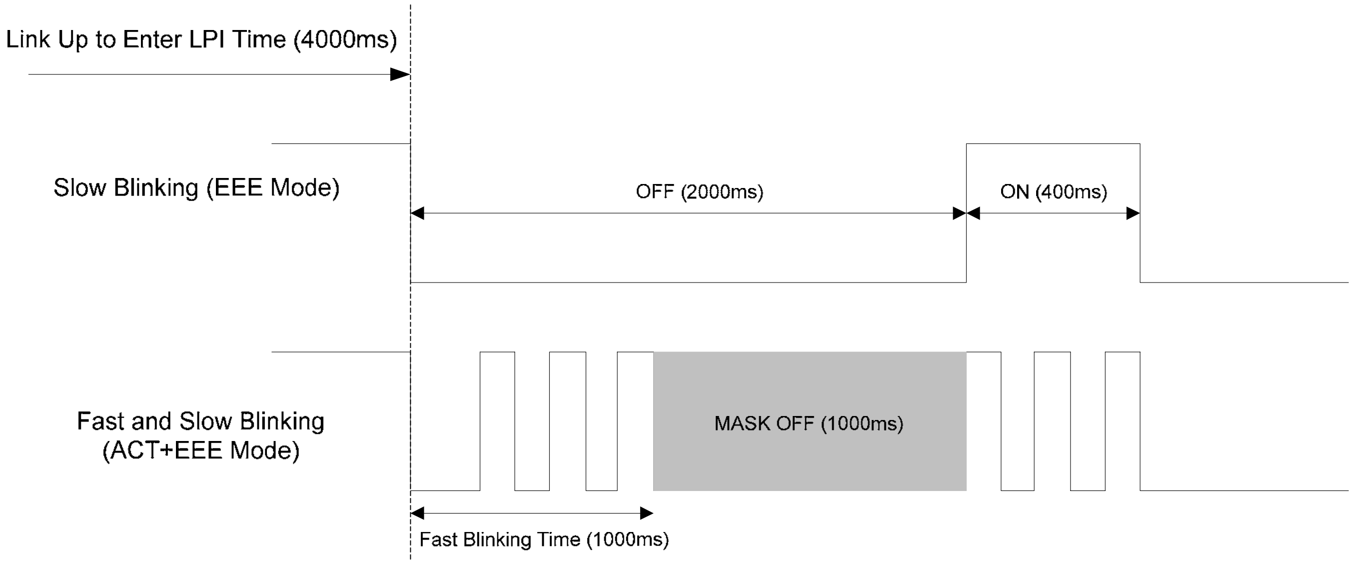


Figure 12. EEE LED Behavior

8.5. Power Down and Link Down Power Saving Modes

Two types of Power Saving mode operation are supported. This section describes how to implement each mode through software.

Table 42. Power Saving Mode Pin Settings

Mode	Description
PWD	Setting bit 11 of register 0 to 1 puts the RTL8201FI-VC into Power Down Mode (PWD). This is the maximum power saving mode while the RTL8201FI-VC is still 'live'. In PWD mode, the RTL8201FI-VC will turn off all analog/digital functions except the MDC/MDIO management interface. Therefore, if the RTL8201FI-VC is put into PWD mode and the MAC wants to recall the PHY, it must create the MDC/MDIO timing by itself (this is done by software).
LDPS	Setting bit 15 of register 24 to 1 will put the RTL8201FI-VC into LDPS (Link Down Power Saving) mode. In LDPS mode, the RTL8201FI-VC will detect the link status to decide whether or not to turn off the transmit function. If the link is off, FLP or 100Mbps IDLE/10Mbps NLP will not be transmitted. However, some signals similar to NLP will be transmitted. Once the receiver detects leveled signals, it will stop the signal and transmit FLP or 100Mbps IDLE/10Mbps NLP again. This can cut power used by 60%~80% when the link is down.

8.6. 10M/100M Transmit and Receive

8.6.1. 100Base-TX Transmit and Receive Operation

100Base-TX Transmit

Transmit data in 4-bit nibbles (TXD[3:0]) clocked at 25MHz (TXC) is transformed into 5B symbol code (4B/5B encoding). Scrambling, serializing, and conversion to 125MHz, and NRZ to NRZI then takes place. After this process, the NRZI signal is passed to the MLT-3 encoder, then to the transmit line driver. The transmitter will first assert TXEN. Before transmitting the data pattern, it will send a /J/K/ symbol (Start-of-frame delimiter), the data symbol, and finally a /T/R/ symbol known as the End-Of-Frame delimiter. For better EMI performance, the seed of the scrambler is based on the PHY address. In a hub/switch environment, each RTL8201FI-VC will have different scrambler seeds and so spread the output of the MLT-3 signals.

100Base-TX Receive

The received signal is compensated by the adaptive equalizer to make up for signal loss due to cable attenuation and Inter Symbol Interference (ISI). Baseline Wander Correction monitors the process and dynamically applies corrections to the process of signal equalization. The Phase Locked Loop (PLL) then recovers the timing information from the signals and from the receive clock. With this, the received signal is sampled to form NRZI (Non-Return-to-Zero Inverted) data. The next steps are the NRZI to NRZ (Non-Return-to-Zero) process, unscrambling of the data, serial to parallel and 5B to 4B conversion, and passing of the 4B nibble to the MII interface.

8.6.2. 100Base-FX Fiber Transmit and Receive Operation

The RTL8201FI-VC can be configured to 100Base-FX mode via hardware configuration. The hardware 100Base-FX setting takes priority over NWay settings. A scrambler is not required in 100Base-FX.

100Base-FX Transmit

Di-bits of TXD are processed as 100Base-TX except without a scrambler before the NRZI stage. Instead of converting to MLT-3 signals, as in 100Base-TX, the serial data stream is driven out as NRZI PECL signals, which enter the fiber transceiver in differential-pair form.

100Base-FX Receive

The signal is received through PECL receiver inputs from the fiber transceiver and directly passed to the clock recovery circuit for data/clock recovery. The scrambler/de-scrambler is bypassed in 100Base-FX.

8.6.3. 10Base-T Transmit and Receive Operation

10Base-T Transmit

Transmit data in 4-bit nibbles (TXD[3:0]) clocked at 2.5MHz (TXC) is first fed to a parallel-to-serial converter, then the 10Mbps NRZ signal is sent to a Manchester encoder. The Manchester encoder converts the 10Mbps NRZ data into a Manchester Encoded data stream for the TP transmitter and adds a Start of Idle pulse (SOI) at the end of the packet as specified in IEEE 802.3. Finally, the encoded data stream is shaped by a band-limited filter embedded in the RTL8201FI-VC and then transmitted.

10Base-T Receive

In 10Base-T receive mode, the Manchester decoder in the RTL8201FI-VC converts the Manchester encoded data stream into NRZ data by decoding the data and stripping off the SOI pulse. The serial NRZ data stream is then converted to a parallel 4-bit nibble signal (RXD[0:3]).

8.7. Reset and Transmit Bias

There are two RTL8201FI-VC reset types:

1. Hardware Reset: Pull the PHYRSTB pin high for at least 150ms to access the RTL8201FI-VC registers. Pull the PHYRSTB pin low for at least 10ms and then pull high. All registers will return to default values after a hardware reset. The media interface will disconnect and restart the auto-negotiation/parallel detection process.

2. Software Reset: Set register 0 bit 15 to 1 for at least 20ms to access the RTL8201FI-VC registers. A Software reset will only partially reset the registers, and will reset the chip status to ‘initializing’.

The RSET pin must be pulled low by a 2.49KΩ resistor with 1% accuracy for reference. Keep its circuitry away from other clock traces and transmit/receive paths to avoid signal interference.

8.8. 3.3V Power Supply and Voltage Conversion Circuit

The RTL8201FI-VC is fabricated in a 0.11µm process. The core circuit needs to be powered by 1.1V, however, the digital IO and DAC circuits need a 3.3V power supply. Regulators are embedded in the RTL8201FI-VC to convert 3.3V to 1.1V.

Note: The internal linear regulator output voltage is 1.1V.

As with many commercial voltage conversion devices, the 1.1V output pin of this circuit requires the use of an output capacitor (0.1µF X7R low-ESR ceramic capacitor) as part of the device frequency compensation.

The analog and digital ground planes should be as large and intact as possible. If the ground plane is large enough, the analog and digital grounds can be separated, which is the ideal configuration. However, if the total ground plane is not sufficiently large, partition of the ground plane is not a good idea. In this case, all the ground pins can be connected together to a larger single and intact ground plane.

Note: The embedded 1.1V LDO is designed for PHYceiver device internal use only. Do not provide this power to other devices.

8.9. Automatic Polarity Correction

The RTL8201FI-VC automatically corrects polarity errors on the receive pairs in 10Base-T mode (polarity is irrelevant in 100Base-TX mode). In 10Base-T mode, polarity errors are corrected based on the detection of validly spaced link pulses. Detection begins during the MDI crossover detection phase and locks when the 10Base-T link is up. The polarity becomes unlocked when the link goes down.

8.10. Far End Fault Indication

The MII Reg.1.4 (Remote Fault) is the Far End Fault Indication (FEFI) bit when 100FX mode is enabled, and indicates when a FEFI has been detected. FEFI is an alternative in-band signaling method that is composed of 84 consecutive '1's followed by one '0'. When the RTL8201FI-VC detects this pattern three times, Reg.1.4 is set, which means the transmit path (the Remote side's receive path) has a problem. On the other hand, if an incoming signal fails to cause a 'Link OK', the RTL8201FI-VC will start sending this pattern, which in turn causes the remote side to detect a Far End Fault. This means that the receive path has a problem from the point of view of the RTL8201FI-VC. The FEFI mechanism is used only in 100Base-FX mode.

8.11. Wake-On-LAN (WOL)

8.11.1. Magic Packet and Wake-Up Frame Format

The RTL8201FI-VC can monitor the network for a Wake-Up Frame or a Magic Packet, and notify the system via the LED0/PHYAD[0]/PMEB (Power Management Event; 'B' means low active) pin when such a packet or event occurs. The system can then be restored to a normal state to process incoming jobs. The LED0/PHYAD[0]/PMEB pin must be connected with a 4.7k-ohm resistor and pulled up to 3.3V when using the WOL function. When the Wake-Up Frame or a Magic Packet is sent to the PHY, the LED0/PHYAD[0]/PMEB pin will be set low to notify the system to wake up. Refer to the WOL application note for details.

Magic Packet Wake-Up occurs only when the following conditions are met:

- The destination address of the received Magic Packet is acceptable to the RTL8201FI-VC, e.g., a broadcast, multicast, or unicast packet addressed to the current RTL8201FI-VC.
- The received Magic Packet does not contain a CRC error.
- The Magic Packet pattern matches; i.e., 6 * FFh + MISC (can be none) + 16 * DID (Destination ID) in any part of a valid Ethernet packet.

A Wake-Up Frame event occurs only when the following conditions are met:

- The destination address of the received Wake-Up Frame is acceptable to the RTL8201FI-VC, e.g., a broadcast, multicast, or unicast address to the current RTL8201FI-VC.
- The received Wake-Up Frame does not contain a CRC error.

- The 16-bit CRC of the received Wake-Up Frame matches the 16-bit CRC of the sample Wake-Up Frame pattern given by the local machine's OS. Or, the RTL8201FI-VC is configured to allow direct packet wake up, e.g., a broadcast, multicast, or unicast network packet.

Note 1: 16-bit CRC: The RTL8201FI-VC supports eight long Wake-Up frames (covering 128 mask bytes from offset 0 to 127 of any incoming network packet). CRC16 polynomial=$x^{16}+x^{12}+x^5+1$.
Note 2: Refer to the WOL Application Note for detailed Wake-On-LAN register settings and waveform timings.

8.11.2. Active Low Wake-On-LAN

When the PHY receives a Wake-Up Frame or a Magic Packet from the link partner, the LED0/PHYAD[0]/PMEB pin will go low and the MAC will wake up after a T cycle. The PMEB pin will be reset to high via the system or MAC (Figure 13 and Figure 14).

Refer to the WOL Application Note for details.

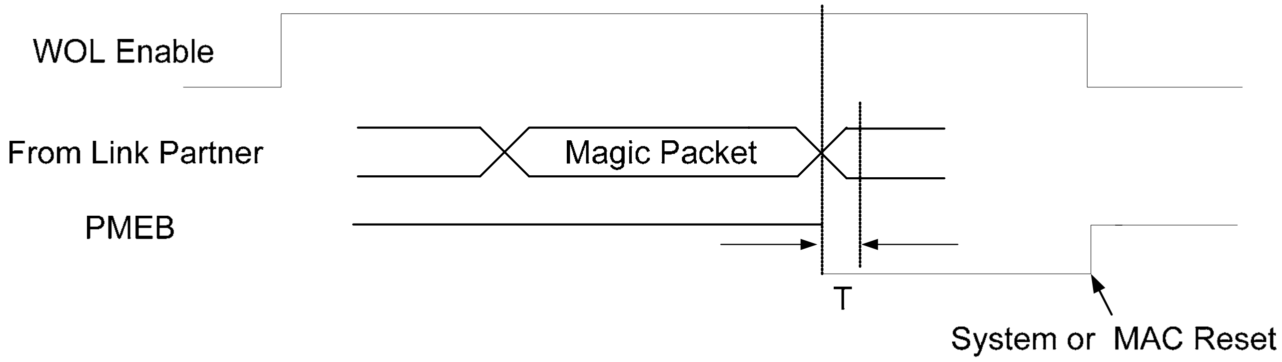


Figure 13. Active Low When Receiving a Magic Packet

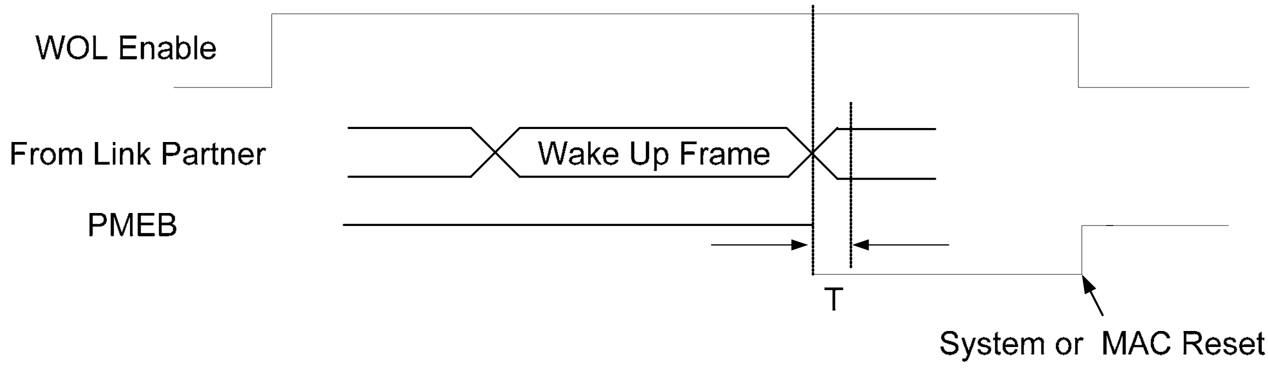


Figure 14. Active Low When Receiving a Wake-Up Frame

8.11.3. Pulse Low Wake-On-LAN

When the PHY receives a Wake-Up Frame or a Magic Packet from the link partner, the LED0/PHYAD[0]/PMEB pin will go low for a period (84ms, 168ms (default), 336ms, or 672ms; set through the MDC/MDIO), and will wake up after a T cycle (Figure 15 and Figure 16).

Refer to the WOL Application Note for details.

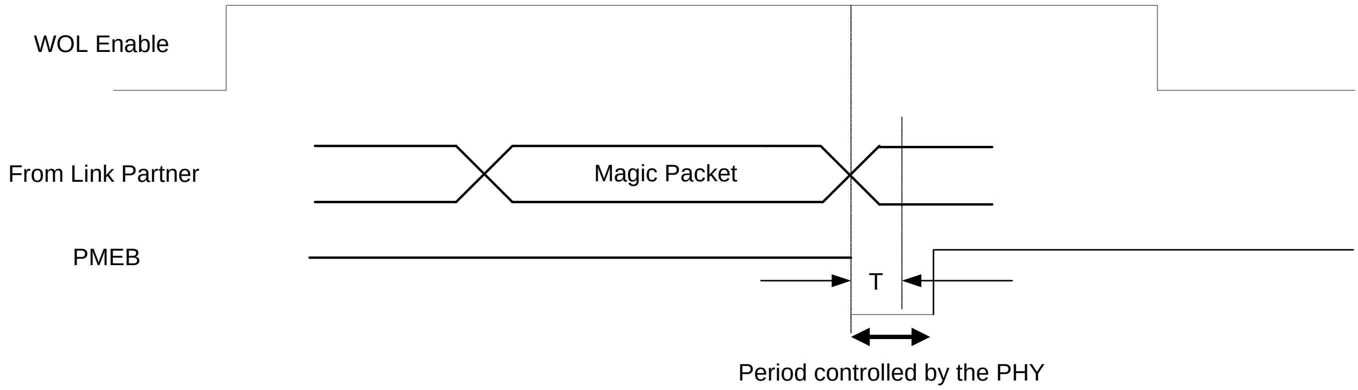


Figure 15. Pulse Low When Receiving a Magic Packet

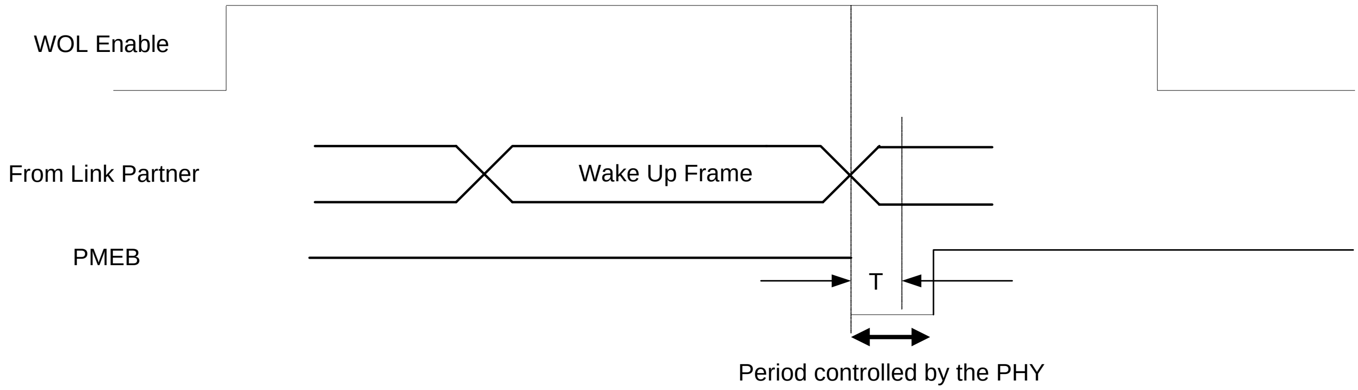


Figure 16. Pulse Low When Receiving a Wake-Up Frame

8.11.4. Wake-On-LAN Pin Types (MII Mode)

Table 43. Wake-On-LAN Pin Types (MII Mode)

Name	Type	Normal			WOL Enable
		100M	10M	Idle	
TXC	O/PD	25M CLK Output	2.5M CLK Output	2.5M CLK Output	O (2.5M/25M)/L/PD[1]
TXEN	I/PD	I	I	I	I/PD
TXD[0:3]	I/PD	I	I	I	I/PD
RXC	O/PD	25M CLK Output	2.5M CLK Output	2.5M CLK Output	O (2.5M/25M)/PD[2]
COL	LI/O/PD	O	O	O	O or PD[2]
CRS	LI/O/PD	O	O	O	O or PD[2]
RXDV	LI/O/PD	O	O	O	O or PD[2]
RXD[0:2]	O/PD	O	O	O	O or PD[2]
RXD[3]	LI/O/PD	O	O	O	O or PD[2]
RXER	LI/O/PD	O	O	O	O or PD[2]
MDC	I/PU	I	I	I	I/PU
MDIO	IO/PU	IO	IO	IO	IO/PU

Note 1: If TX Isolate=1, the TXC is halted and the pin type is 'L'.
Set page0, register0, and bit10=1 to change the TXC pin type to 'PD'.
Note 2: If RX Isolate=1, all the MII RX interfaces are halted and the pin types are 'PD'.

8.11.5. Wake-On-LAN Pin Types (RMII Mode)

Table 44. Wake-On-LAN Pin Types (RMII Mode)

Name	Type	Normal			WOL Enable
		100M	10M	Idle	
TXC (REF_CLK)[1]	IO/PD	50M CLK Input/Output	50M CLK Input/Output	50M CLK Input/Output	I/O (50M)[2]
TXEN	I/PD	I	I	I	I/PD
TXD[0:1]	I/PD	I	I	I	I/PD
CRS_DV	LI/O/PD	O	O	O	O or PD[3]
RXD[0:1]	O/PD	O	O	O	O or PD[3]
RXER	LI/O/PD	O	O	O	O or PD[3]
MDC	I/PU	I	I	I	I/PU
MDIO	IO/PU	IO	IO	IO	IO/PU

Note 1: If TXC (REF_CLK) is in input mode (MAC to PHY), the REF_CLK cannot halt at WOL Enable.
Note 2: When REF_CLK is in output mode (PHY to MAC), the REF_CLK cannot halt (always toggles 50MHz out). To set the TXC pin type to 'PD', set page0, register0, bit10=1.
Note 3: If RX Isolate=1, all RMII RX interfaces are halted and the pin types are 'PD'.

8.12. Energy Efficient Ethernet (EEE)

The RTL8201FI-VC supports IEEE 802.3az-2010, also known as Energy Efficient Ethernet (EEE), at 10Mbps and 100Mbps. It provides a protocol to coordinate transitions to/from a lower power consumption level (Low Power Idle mode) based on link utilization. When no packets are being transmitted, the system goes to Low Power Idle mode to save power. When packets need to be transmitted, the system returns to normal mode, and does this without changing the link status and without dropping/corrupting frames.

To save power, when the system is in Low Power Idle mode, most of the circuits are disabled; however, the transition time to/from Low Power Idle mode is kept small enough to be transparent to upper layer protocols and applications.

EEE also specifies a negotiation method to enable link partners to determine whether EEE is supported.

Refer to http://www.ieee802.org/3/az/index.html for more details.

8.13. Spread Spectrum Clock (SSC)

The RMII REF_CLK path can be a source of EMI noise. Spread Spectrum Clock (SSC) spreads the REF_CLK signal across a wider bandwidth, reducing the peak radiated energy at any one frequency, and lowering unwanted EMI noise.

The SSC function is enabled by default when using RMII REF_CLK output mode (see section 7.21 Page 7 Register 24 Spread Spectrum Clock Register, page 22).

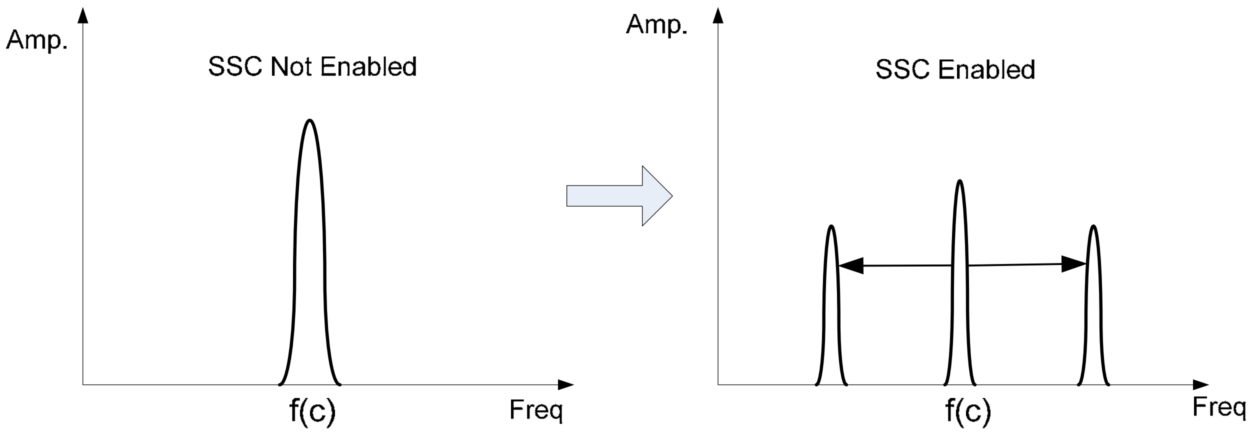


Figure 17. Spectrum Spread Clock

9. Characteristics

9.1. DC Characteristics

9.1.1. Absolute Maximum Ratings

Table 45. Absolute Maximum Ratings

Symbol	Description	Minimum	Maximum	Unit
DVDD33, AVDD33	Supply Voltage 3.3V	-0.4	+3.7	V
DVDD10, DVDD10OUT, AVDD10OUT	Supply Voltage 1.05V*	-0.1	+1.26	V
DC Input	Input Voltage	-0.3	Corresponding Supply Voltage +0.5V	V
DC Output	Output Voltage	-0.3	Corresponding Supply Voltage +0.5V	V
N/A	Storage Temperature	-55	+125	°C

Note: The internal linear regulator output voltage is 1.1V.

9.1.2. Recommended Operating Conditions

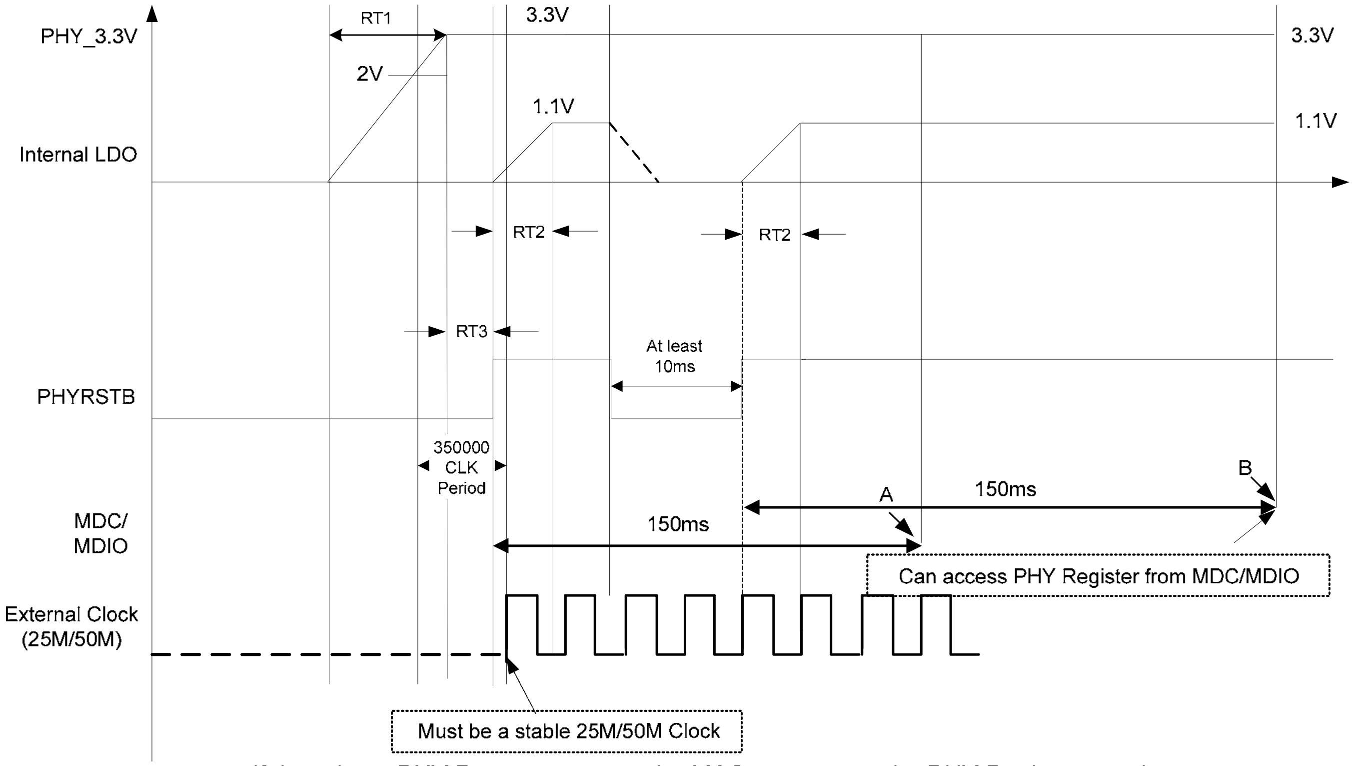
Table 46. Recommended Operating Conditions

Description	Pins	Minimum	Typical	Maximum	Unit
Supply Voltage VDD	DVDD33, AVDD33	2.97	3.30	3.63	V
	DVDD10, DVDD10OUT, AVDD10OUT	1.00	1.05*	1.16	V
Ambient Operating Temperature T_A	-	-40	-	85	°C
Maximum Junction Temperature	-	-	-	125	°C

Note: The internal linear regulator output voltage is 1.1V.

9.1.3. Power On and PHY Reset Sequence

The RTL8201FI-VC needs 150ms power on time. After 150ms it can access the PHY register from MDC/MDIO.



Note1: If there is no PHY Reset sequence, the MAC can access the PHY Register at point A.
Note2: If there is a PHY Reset sequence, the MAC can access the PHY Register at point B.
Note3: The Internal LDO (Linear Regulator) output voltage is 1.1V.

Figure 18. Power On and PHY Reset Sequence

Table 47. Power On and PHY Reset Sequence

Symbol	Description	Minimum	Maximum
Rt1	3.3V Rise Time@ Power On Sequence	100µs	-
Rt2	1.05V Rise Time@ Power On and PHY Reset Sequence	100µs	-
Rt3	PHYRSTB De-Assert after PHY_3.3V Stable	80µs	-

Note: Rt2 requires 100µs Rise Time only when using an external 1.05V power supply.

9.1.4. RMII Input Mode Power Dissipation

The whole system power dissipation (including regulator loss) is shown in Table 48.

Table 48. RMII Input Mode Power Dissipation (Whole System)

Symbol	Condition	RTL8201FI-VC	Unit
P_{10IDLE}	10Base-T Idle	29.7	mW
P_{10F}	10Base-T Full Duplex (EEE not Enabled)	122.1	mW
P_{10FEEE}	10Base-T Full Duplex with EEE	112.2	mW
$P_{100IDLE}$	100Base-T Idle (EEE not Enabled)	141.9	mW
$P_{100IDLEEEE}$	100Base-T Idle with EEE	33	mW
P_{100F}	100Base-T Full Duplex	165	mW
P_{LDPS}	Link Down Power Saving	13.2	mW
P_{PHYRST}	PHY Reset	3.3	mW

9.1.5. Input Voltage: Vcc

Table 49. Input Voltage: Vcc

Symbol	Condition		Minimum	Maximum
TTL V_{IH}	Input High Voltage	-	0.5*Vcc	Vcc+0.5V
TTL V_{IL}	Input Low Voltage	-	-0.5V	0.7V
TTL V_{OH}	Output High Voltage	IOH=-8mA	0.65*Vcc	Vcc
TTL V_{OL}	Output Low Voltage	IOL=8mA	-	0.7V
TTL I_{OZ}	Tri-State Leakage	Vout=Vcc or GND	-110µA	10µA
I_{IN}	Input Current	Vin=Vcc or GND	-1µA	10µA
I_{PL}	Input Current with Internal Weakly Pulled Low Resistor	Vin=Vcc or GND	-1µA	100µA
I_{PH}	Input Current with Internal Weakly Pulled High Resistor	Vin=Vcc or GND	-110µA	10µA
PECL V_{IH}	PECL Input High Voltage	-	Vdd-1.16V	Vdd-0.88V
PECL V_{IL}	PECL Input Low Voltage	-	Vdd-1.81V	Vdd-1.47V
PECL V_{OH}	PECL Output High Voltage	-	Vdd-1.02V	-
PECL V_{OL}	PECL Output Low Voltage	-	-	Vdd-1.62V

9.2. AC Characteristics

All output timing assumes equivalent loading between 10pF and 25pF that includes PCB layout traces and other connected devices (e.g., MAC).

9.2.1. MII Transmission Cycle Timing

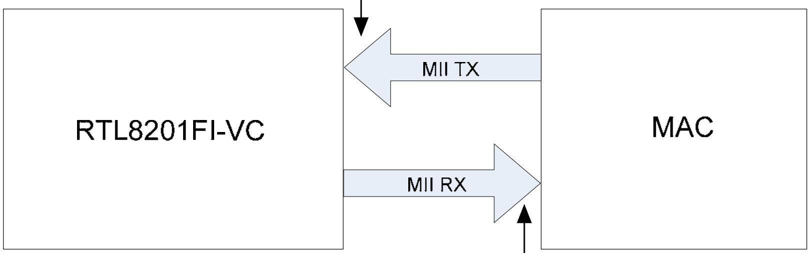


Figure 19. MII Interface Setup/Hold Time Definitions

Figure 20 and Figure 21 and show an example of a packet transfer from MAC to PHY on the MII interface.

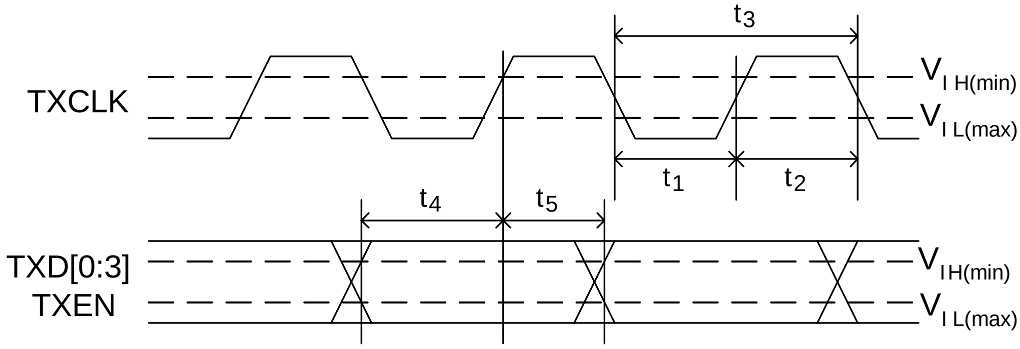


Figure 20. MII Transmission Cycle Timing-1

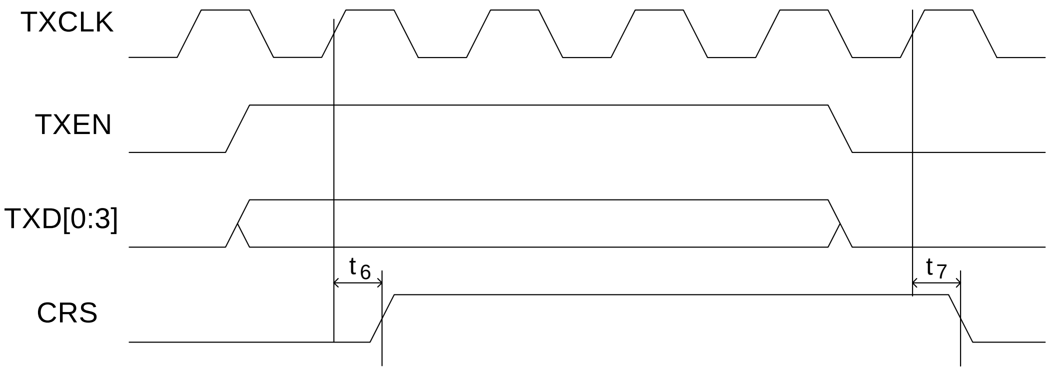


Figure 21. MII Transmission Cycle Timing-2

Table 50. MII Transmission Cycle Timing

Symbol	Description		Minimum	Typical	Maximum	Unit
t_1	TXCLK High Pulse Width	100Mbps	14	20	26	ns
		10Mbps	140	200	260	ns
t_2	TXCLK Low Pulse Width	100Mbps	14	20	26	ns
		10Mbps	140	200	260	ns
t_3	TXCLK Period	100Mbps	-	40	-	ns
		10Mbps	-	400	-	ns
t_4	TXEN, TXD[0:3] Setup to TXCLK Rising Edge	100Mbps	10	-	-	ns
		10Mbps	5	-	-	ns
t_5	TXEN, TXD[0:3] Hold After TXCLK Rising Edge	100Mbps	0	-	-	ns
		10Mbps	0	-	-	ns
t_6	TXEN Sampled to CRS High	100Mbps	-	-	40	ns
		10Mbps	-	-	400	ns
t_7	TXEN Sampled to CRS Low	100Mbps	-	-	160	ns
		10Mbps	-	-	2000	ns

9.2.2. MII Reception Cycle Timing

Figure 22 and Figure 23 show an example of a packet transfer from PHY to MAC on the MII interface.

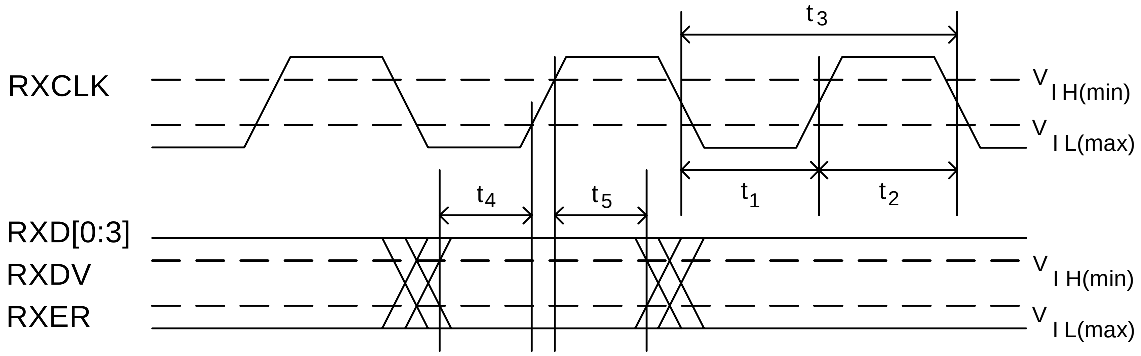


Figure 22. MII Reception Cycle Timing-1

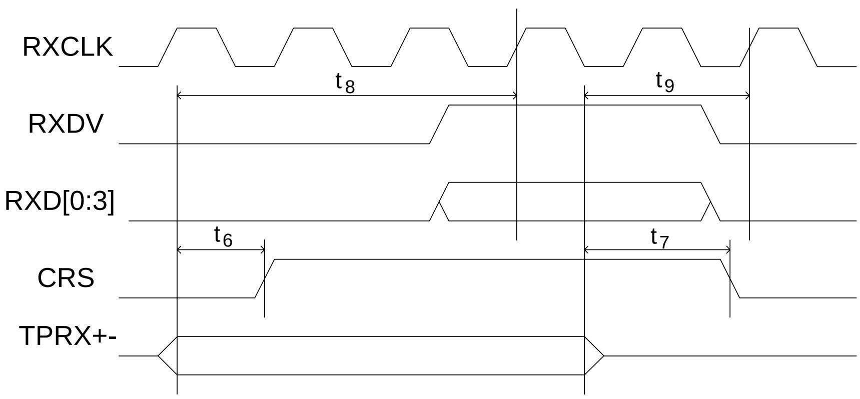


Figure 23. MII Reception Cycle Timing-2

Table 51. MII Reception Cycle Timing

Symbol	Description		Minimum	Typical	Maximum	Unit
t_1	RXCLK High Pulse Width	100Mbps	14	20	26	ns
		10Mbps	140	200	260	ns
t_2	RXCLK Low Pulse Width	100Mbps	14	20	26	ns
		10Mbps	140	200	260	ns
t_3	RXCLK Period	100Mbps	-	40	-	ns
		10Mbps	-	400	-	ns
t_4	RXER, RXDV, RXD[0:3] Setup to RXCLK Rising Edge	100Mbps	10	-	-	ns
		10Mbps	10	-	-	ns
t_5	RXER, RXDV, RXD[0:3] Hold After RXCLK Rising Edge	100Mbps	10	-	-	ns
		10Mbps	10	-	-	ns
t_6	Receive Frame to CRS High	100Mbps	-	-	130	ns
		10Mbps	-	-	2000	ns
t_7	End of Receive Frame to CRS Low	100Mbps	-	-	240	ns
		10Mbps	-	-	1000	ns
t_8	Receive Frame to Sampled Edge of RXDV	100Mbps	-	-	150	ns
		10Mbps	-	-	3200	ns
t_9	End of Receive Frame to Sampled Edge of RXDV	100Mbps	-	-	120	ns
		10Mbps	-	-	1000	ns

9.2.3. RMII Transmission and Reception Cycle Timing

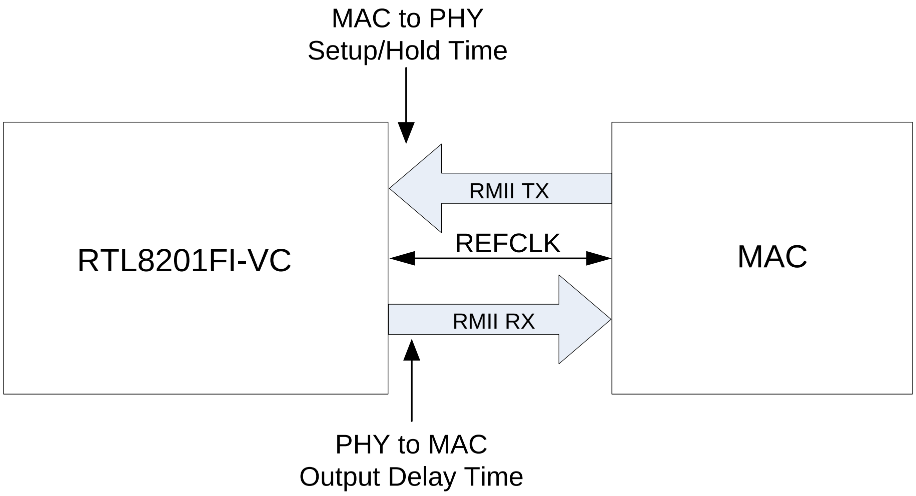


Figure 24. RMII Interface Setup, Hold Time, and Output Delay Time Definitions

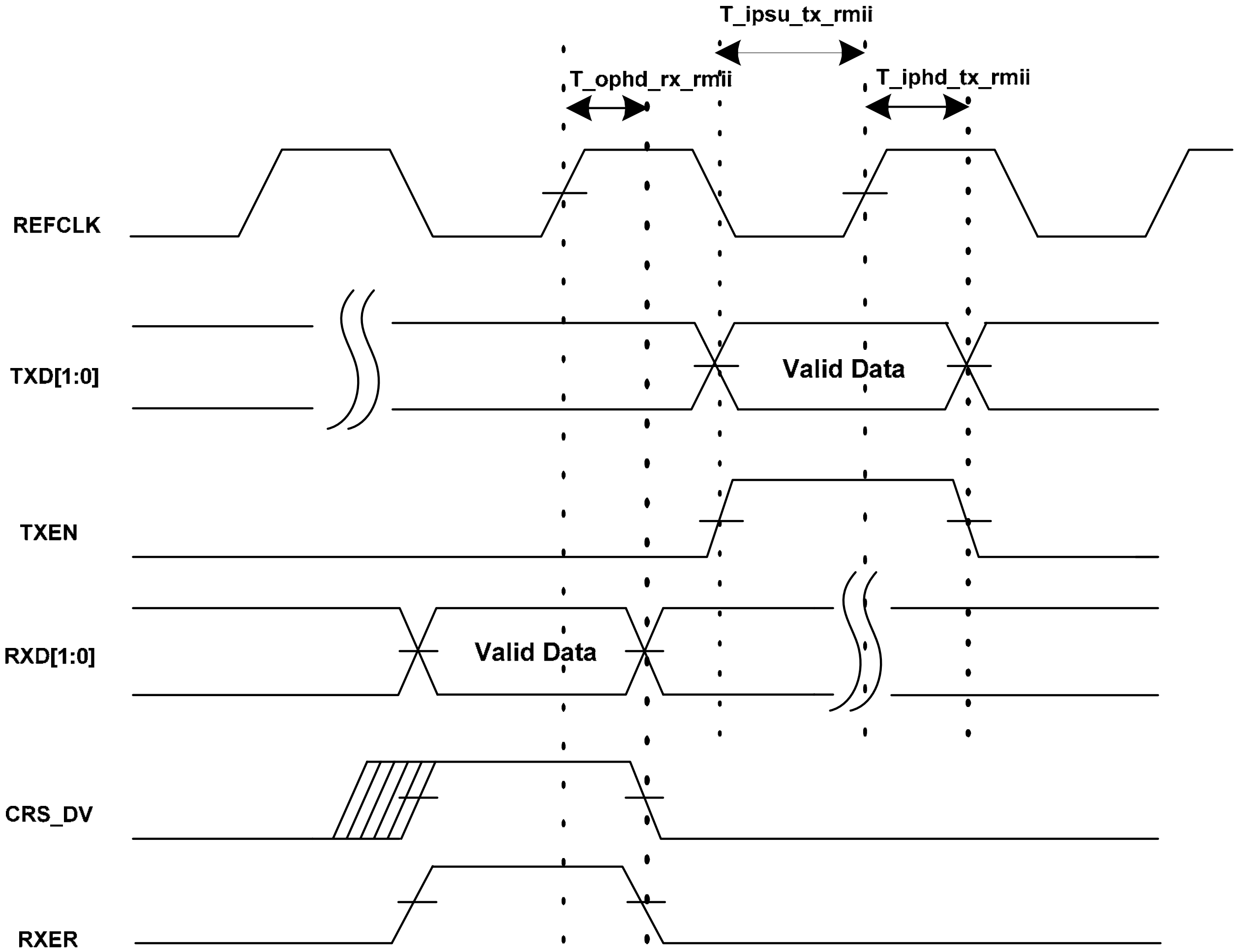


Figure 25. RMII Transmission and Reception Cycle Timing

Table 52. RMII Transmission and Reception Cycle Timing

Symbol	Description	Minimum	Typical	Maximum	Unit
REFCLK Frequency	Frequency of Reference Clock	-	50	-	MHz
REFCLK Duty Cycle	Duty Cycle of Reference Clock	35	-	65	%
T_ipsu_tx_rmii	TXD[1:0]/TXEN Setup Time to REFCLK	4	-	-	ns
T_iphd_tx_rmii	TXD[1:0]/TXEN Hold Time from REFCLK	2	-	-	ns
T_ophd_rx_rmii	RXD[1:0]/CRS_DV/RXER Output Delay Time from REFCLK	2	-	-	ns

Note 1: RMII TX timing can be adjusted by setting page7, register16[11:8]; the minimum adjustable resolution is 2ns. Any changes for these bits are not recommended as the default value is the optimum setting.

Note 2: RMII RX timing can be adjusted by setting page7, register16[7:4]; the minimum adjustable resolution is 2ns. Any changes for these bits are not recommended as the default value is the optimum setting.

9.2.4. MDC/MDIO Timing

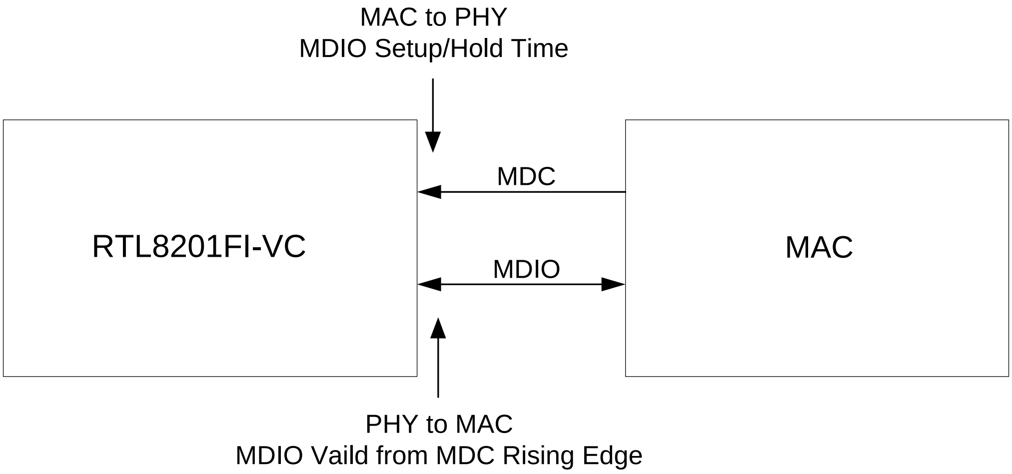


Figure 26. MDC/MDIO Interface Setup, Hold Time, and Valid from MDC Rising Edge Time Definitions

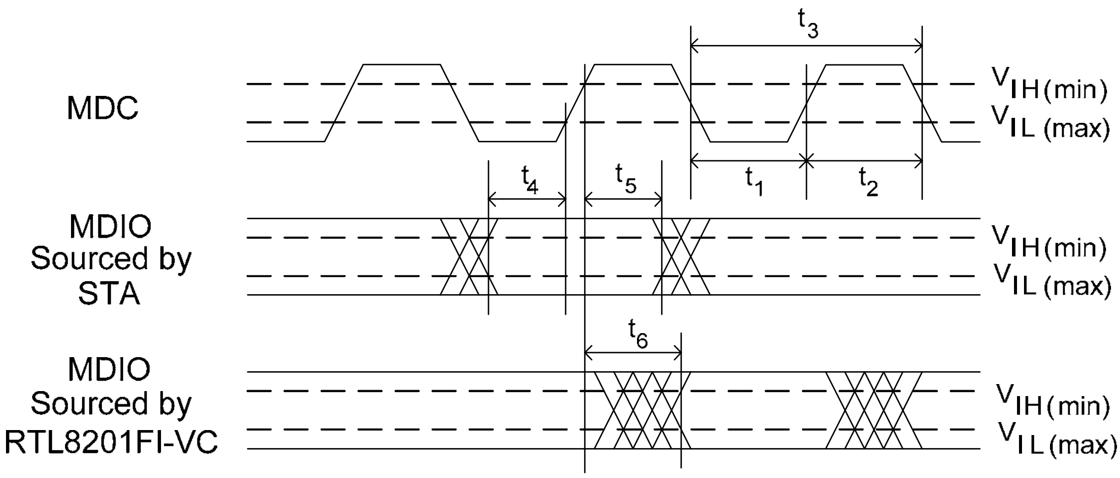


Figure 27. MDC/MDIO Timing

Table 53. MDC/MDIO Timing

Symbol	Description	Minimum	Maximum	Unit
t_1	MDC High Pulse Width	160	-	ns
t_2	MDC Low Pulse Width	160	-	ns
t_3	MDC Period	400	-	ns
t_4	MDIO Setup to MDC Rising Edge	10	-	ns
t_5	MDIO Hold Time from MDC Rising Edge	10	-	ns
t_6	MDIO Valid from MDC Rising Edge	0	300	ns

9.2.5. Transmission without Collision

Figure 28 shows an example of a packet transfer from MAC to PHY.

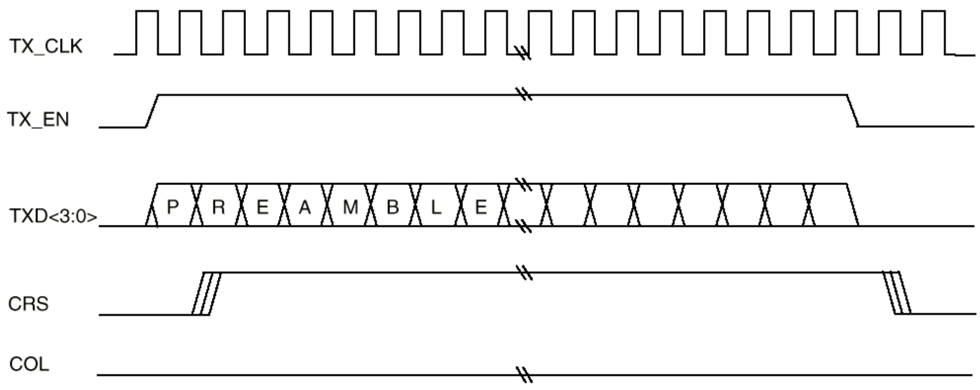


Figure 28. MAC to PHY Transmission without Collision

9.2.6. Reception without Error

Figure 29 shows an example of a packet transfer from PHY to MAC.

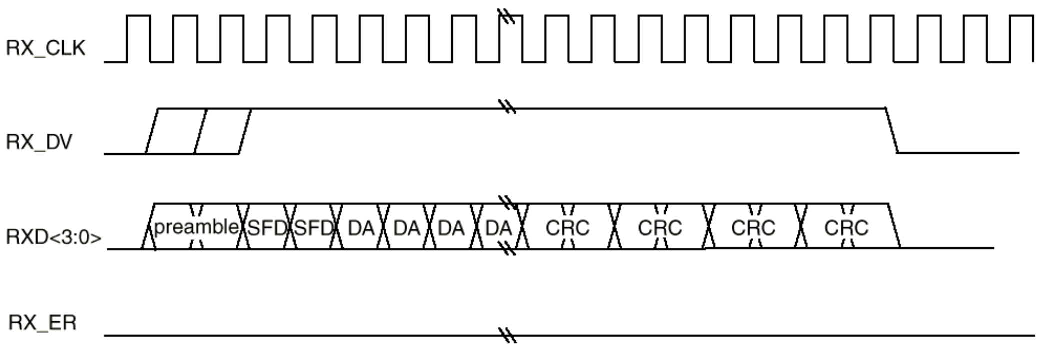


Figure 29. PHY to MAC Reception Without Error

9.3. Crystal Characteristics

Table 54. Crystal Characteristics

Symbol	Description/Condition	Minimum	Typical	Maximum	Unit
To	Operating Temperature Range	-40	-	85	°C
F_{ref}	Parallel Resonant Crystal Reference Frequency, Fundamental Mode, AT-Cut Type.	-	25	-	MHz
F_{ref} Stability	Parallel Resonant Crystal Frequency Stability, Fundamental Mode, AT-Cut Type. T_a=-40°C~85°C.	-30	-	+30	ppm
F_{ref} Tolerance	Parallel Resonant Crystal Frequency Tolerance, Fundamental Mode, AT-Cut Type. T_a=25°C.	-50	-	+50	ppm
F_{ref} Duty Cycle	Reference Clock Input Duty Cycle.	40	-	60	%
ESR	Equivalent Series Resistance.	-	-	30	Ω
DL	Drive Level.	-	-	0.3	mW
Jitter	Broadband Peak-to-Peak Jitter[1, 2]	-	-	500	ps

Note 1: 25KHz to 25MHz RMS < 3ps.
Note 2: Broadband RMS < 9ps.

9.4. Oscillator Requirements

Table 55. Oscillator Requirements

Parameter	Condition	Minimum	Typical	Maximum	Unit
Operating Temperature Range	-	-40	-	85	°C
Frequency	-	-	25/50	-	MHz
Frequency Stability	Ta=-40°C~85°C	-30	-	30	ppm
Frequency Tolerance	Ta=25°C	-50	-	50	ppm
Duty Cycle	-	40	-	60	%
Broadband Peak-to-Peak Jitter[1, 2]	-	-	-	500	ps
Vpeak-to-peak	-	3.15	3.3	3.45	V
Rise Time (10%~90%)	-	-	-	10	ns
Fall Time (10%~90%)	-	-	-	10	ns

Note 1: 25KHz to 25MHz RMS < 3ps.
Note 2: Broadband RMS < 9ps.

9.5. Clock Requirements

Table 56. Clock Requirements

Parameter	Minimum	Typical	Maximum	Unit
Frequency	-	25/50	-	MHz
Frequency Stability	-30	-	30	ppm
Frequency Tolerance	-50	-	50	ppm
Duty Cycle	40	-	60	%
Broadband Peak-to-Peak Jitter[1, 2]	-	-	500	ps
Vpeak-to-peak	3.15	3.3	3.45	V
Rise Time (10%~90%)	-	-	10	ns
Fall Time (10%~90%)	-	-	10	ns

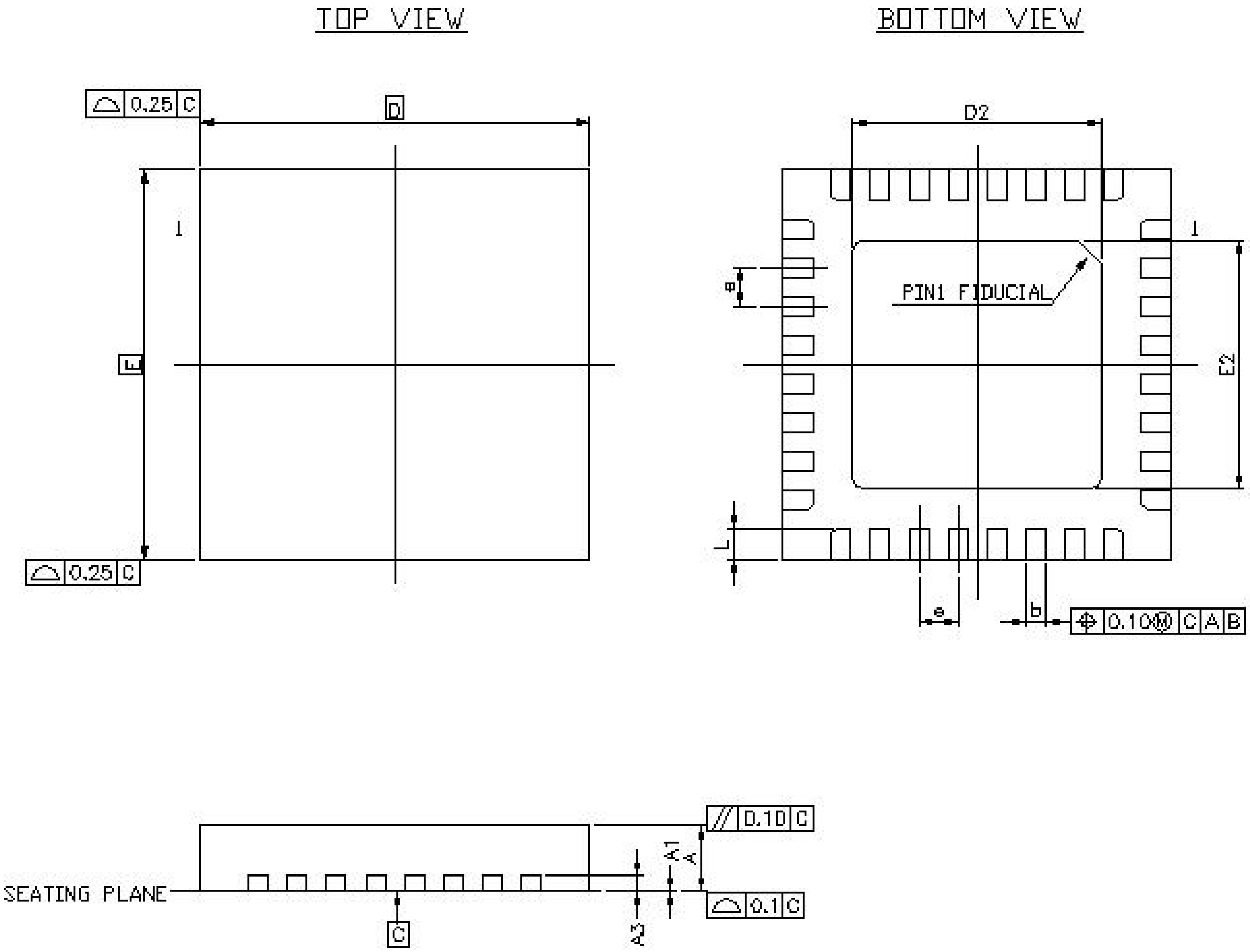
Note 1: 25KHz to 25MHz RMS < 3ps.
Note 2: Broadband RMS < 9ps.

9.6. Transformer Characteristics

Table 57. Transformer Characteristics

Parameter	Transmit End	Receive End
Turn Ratio	1:1 CT	1:1 CT
Inductance (min.)	350µH @ 8mA	350µH @ 8mA

10. Mechanical Dimensions



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.75	0.85	1.00	0.030	0.034	0.039
A_1	0.00	0.02	0.05	0.000	0.001	0.002
A_3	0.20REF			0.008REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
c	-	-	0.6	-	-	0.024
D/E	5.00BSC			0.197BSC		
D_2/E_2	3.10	3.35	3.60	0.122	0.132	0.142
e	0.50BSC			0.020BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020

Note 1: CONTROLLING DIMENSION: MILLIMETER (mm).
Note 2: REFERENCE DOCUMENT: JEDEC MO-220.

11. Ordering Information

Table 58. Ordering Information

Part Number	Package	Status
RTL8201FI-VC-CG	32-Pin QFN 'Green' Package	

Note: See page 5 for package identification.

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