RTL8211FS-CG RTL8211FS-VS-CG
RTL8211FSI-CG RTL8211FSI-VS-CG

INTEGRATED 10/100/1000M ETHERNET PRECISION TRANSCEIVER

DATASHEET

(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2014/04/09	First release.
1.1	2014/07/13	Corrected minor typing errors. Revised section 2 Features, page 2. Revised section 7.13.4 Change Page, page 27. Revised section 7.16 LED Configuration, page 33. Revised section 7.19 PHY Reset (Hardware Reset), page 36. Revised section 8 Register Descriptions, page 37. Added section 8.5.24 FLCR (Fiber LED Control Register, Page 0xd04, Address 0x12), page 54. Revised section 9 Switching Regulator, page 75. Revised Table 97 Oscillator/External Clock Requirements, page 78. Revised section 10.8.2 RGMII Timing Modes, page 85. Revised section 12 Ordering Information, page 91.
1.2	2014/07/25	Corrected minor typing errors. Revised section 3 System Applications, page 3. Revised section 4 Block Diagram, page 7. Revised section 6 Pin Descriptions, page 10. Revised section 7.7 Interrupt, page 21. Added section 7.13.2 SGMII, page 25. Revised section 8 Register Descriptions, page 37. Added section 8.5.25 MIICR (MII Control Register, Page 0xd08, Address 0x15), page 54.

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1. General Description

The Realtek RTL8211FS-CG/RTL8211FS-VS-CG/RTL8211FSI-CG/RTL8211FSI-VS-CG is a highly integrated Ethernet transceiver that complies with 10Base-T, 100Base-TX, and 1000Base-T IEEE 802.3 standards. It provides all the necessary physical layer functions to transmit and receive Ethernet packets over CAT.5 UTP cable. The RTL8211FSI and RTL8211FSI-VS are manufactured to industrial grade standards.

The RTL8211FS(I)-VS provides full hardware support for high-precision clock synchronization based on the Precision Time Protocol (PTP) of IEEE 1588 and 802.1AS standard. The integrated PTP functionality accurately timestamps each PTP packet on the Tx/Rx path, and the upper layer software can use this timing information to determine the timing offset to the PTP master's clock. The device also provides GPIOs as PTP application interfaces.

The RTL8211FS(I)(-VS) uses state-of-the-art DSP technology and an Analog Front End (AFE) to enable high-speed data transmission and reception over UTP cable. Functions such as Crossover Detection & Auto-Correction, polarity correction, adaptive equalization, cross-talk cancellation, echo cancellation, timing recovery, and error correction are implemented in the RTL8211FS(I)(-VS) to provide robust transmission and reception capabilities at 10Mbps, 100Mbps, or 1000Mbps.

Data transfer between MAC and PHY is via the Reduced Gigabit Media Independent Interface (RGMII), or Serial Gigabit Media Independent Interface (SGMII) for 1000Base-T, 10Base-T, and 100Base-TX. The RTL8211FS(I)(-VS) supports various RGMII signaling voltages, including 3.3, 2.5, 1.8, and 1.5V.

The RTL8211FS(I)(-VS) also supports a SerDes interface that can be configured as SGMII, 1000Base-X, or 100Base-FX.

2. Features

- 1000Base-T IEEE 802.3ab Compliant
- 100Base-TX IEEE 802.3u Compliant
- 10Base-T IEEE 802.3 Compliant
- Supports RGMII
- Supports IEEE 802.3az-2010 (Energy Efficient Ethernet)
- Built-in Wake-on-LAN (WOL) over UTP/Fiber
- Supports Interrupt function over UTP/Fiber
- Supports Parallel Detection
- Crossover Detection & Auto-Correction
- Automatic polarity correction
- Supports PHYRSTB core power Turn-Off
- Baseline Wander Correction
- Supports 120m for CAT.5 cable in 1000Base-T
- Selectable 3.3/2.5/1.8/1.5V signaling for RGMII
- Supports 25MHz external crystal or OSC
- Provides 125MHz clock source for MAC
- Provides 3 network status LEDs
- Supports Link Down power saving
- Green Ethernet (1000/100Mbps mode only)
- Built-in Switching Regulator and LDO
- 48-pin QFN Green Package
- 55 nm process with ultra-low power consumption
- Industrial grade manufacturing process (RTL8211FSI(-VS))
- Supports SERDES (SGMII/Fiber)
- Supports Fiber-to-UTP Media Convertor mode or SGMII-to-RGMII Bridge mode
- Supports UTP/Fiber Auto Detection
- Complete hardware support for Synchronous Ethernet and Precision Time Protocol (PTP) including IEEE 1588v1, v2, and 802.1AS (RTL8211FS(I)-VS only)
- PTP Packet parser supports Layer 2 Ethernet, IPv4/UDP, IPv6/UDP packets (RTL8211FS(I)-VS only)
- PTP One-Step operation supported (RTL8211FS(I)-VS only)
- PTP clock synchronization (RTL8211FS(I)-VS only)
- PTP timestamp with 8ns resolution (RTL8211FS(I)-VS only)
- Deterministic and low transmission latency for PTP mechanism (RTL8211FS(I)-VS only)
- Adjustable PTP clock (RTL8211FS(I)-VS only)
- Two PTP GPIOs as programmable Time Application Interfaces (RTL8211FS(I)-VS only)
- Low-jitter synchronized PTP clock output (RTL8211FS(I)-VS only)
- Selectable PTP clock input from the external reference clock source (RTL8211FS(I)-VS only)

3. System Applications

- DTV (Digital TV)
- MAU (Media Access Unit)
- CNR (Communication and Network Riser)
- Game Console
- Printer and Office Machine
- DVD Player and Recorder
- Ethernet Hub
- Ethernet Switch
- PTP-featured Equipment with Ethernet Ports
- Base Stations and Controllers
- Routers, DSLAMs, PON Equipment
- Test and Measurement Systems
- Industrial and Factory Automation Equipment
- Multimedia synchronization and Real Time Networking

In addition, the RTL8211FS(I)(-VS) can be used in any embedded system with an Ethernet MAC that needs a UTP physical connection.

3.1. UTP (UTP←→RGMII; UTP←→SGMII) Application Diagram

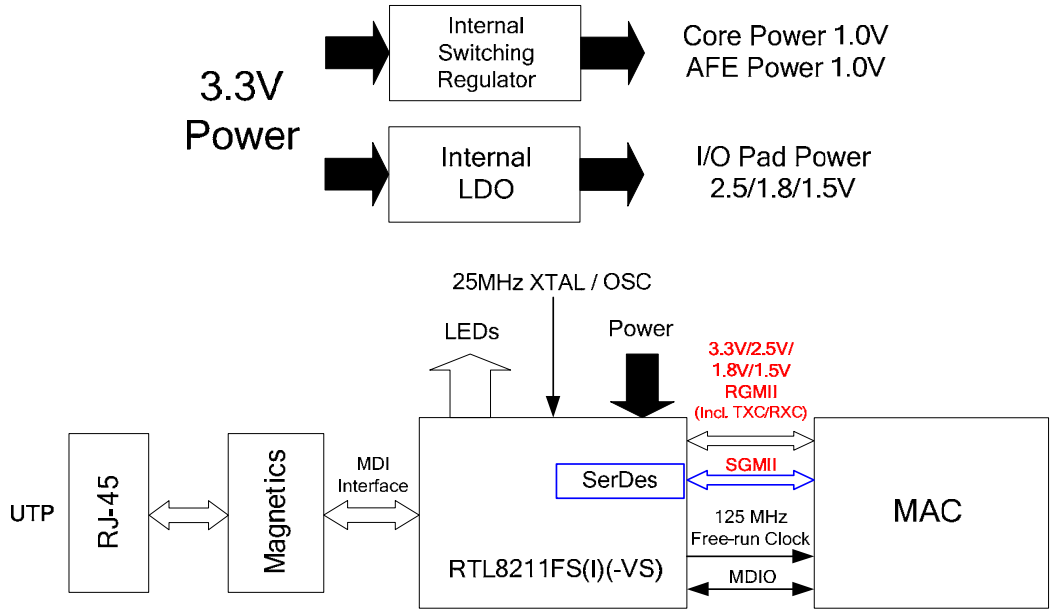


Figure 1. UTP (UTP←→RGMII; UTP←→SGMII) Application Diagram

3.2. Fiber (FIBER←→RGMII) Application Diagram

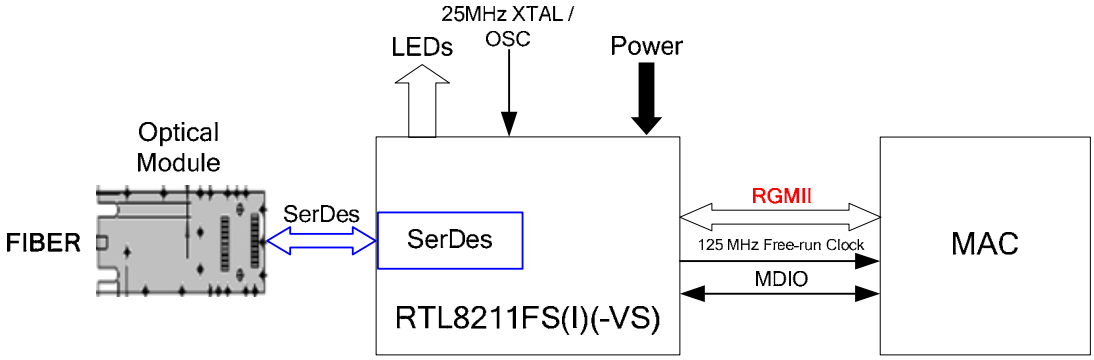


Figure 2. Fiber (FIBER←→RGMII) Application Diagram

3.3. UTP/Fiber to RGMII (UTP/FIBER Media Auto Detection ←→RGMII) Application Diagram

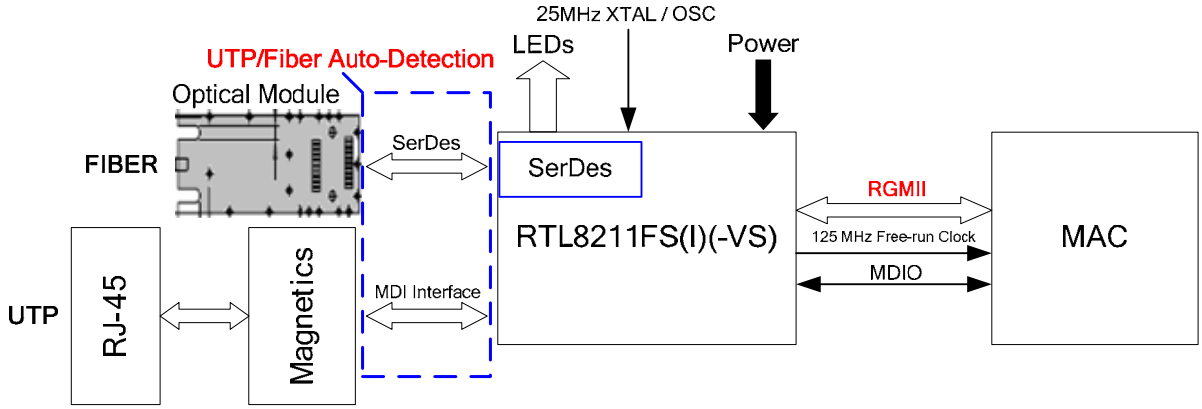


Figure 3. UTP/Fiber to RGMII (UTP/FIBER Media Auto Detection←→RGMII) Application Diagram

3.4. SGMII to RGMII (SGMII←→RGMII Bridge Mode) Application Diagram

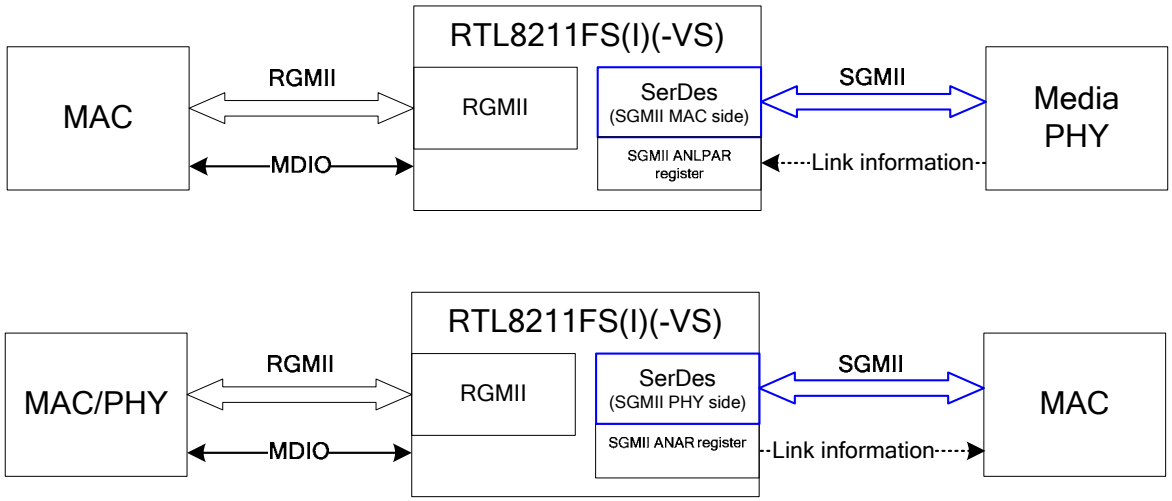


Figure 4. SGMII to RGMII (SGMII←→RGMII Bridge Mode) Application Diagram

3.5. Fiber to UTP (UTP←→FIBER Media Converter) Application Diagram

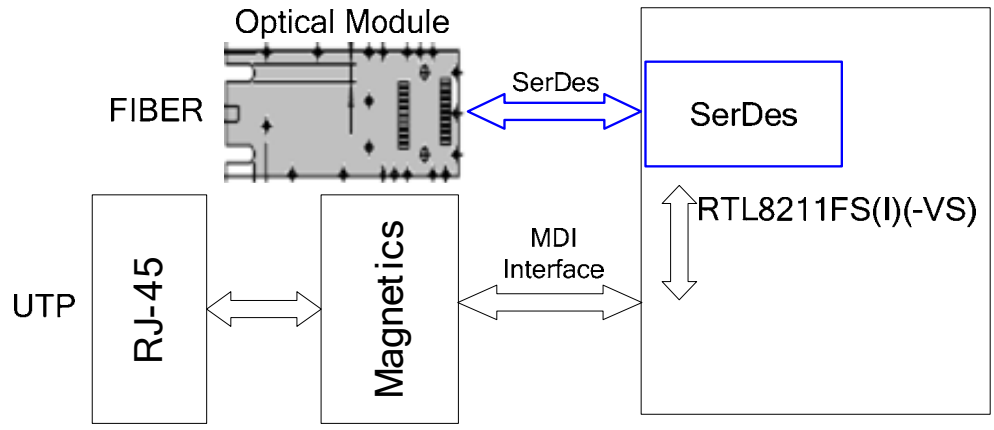


Figure 5. Fiber to UTP (UTP←→FIBER Media Converter) Application Diagram

3.6. PTP and Sync Ethernet Application Diagram (RTL8211FS(I)-VS Only)

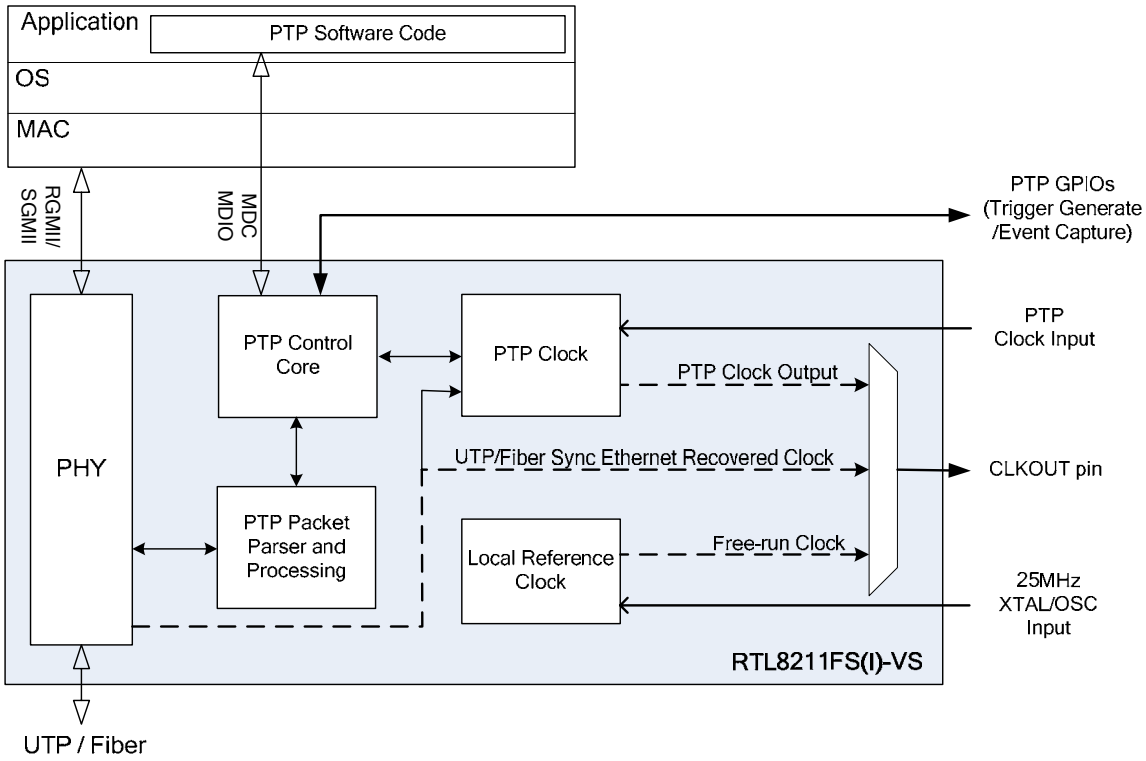


Figure 6. PTP and Sync Ethernet Application Diagram

4. Block Diagram

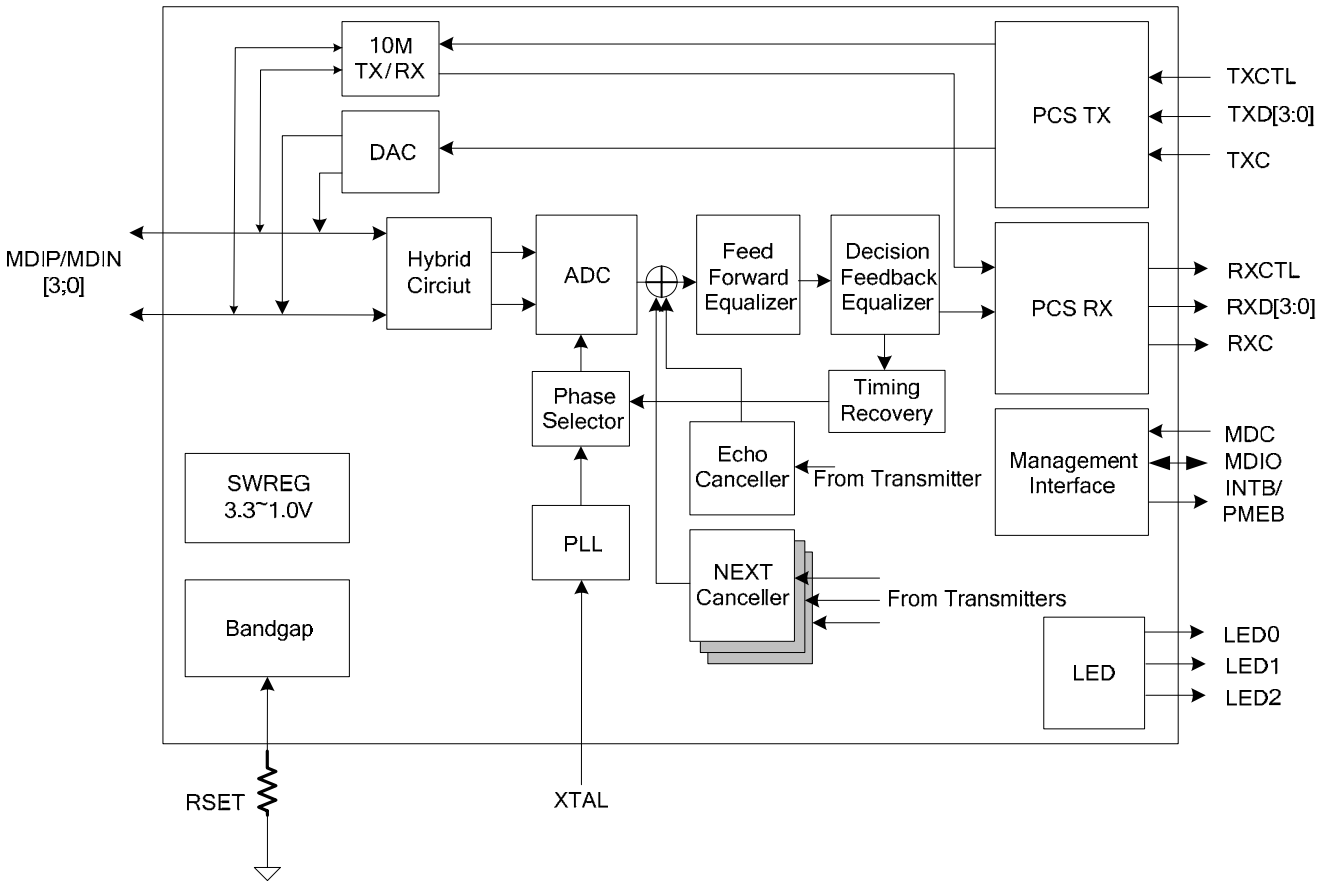


Figure 7. Block Diagram

5. Pin Assignments

5.1. RTL8211FS(I) Pin Assignments

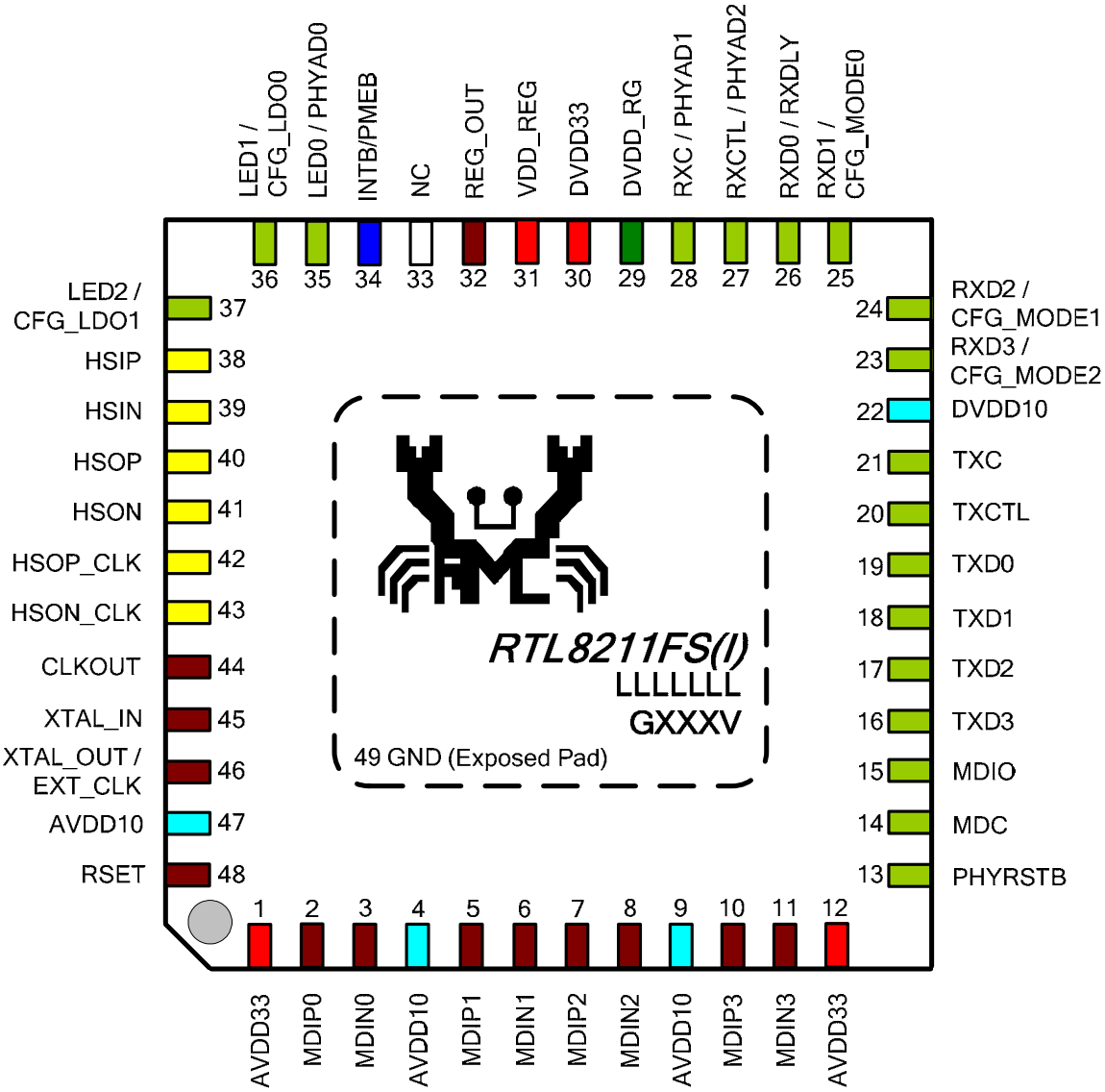


Figure 8. RTL8211FS(I) Pin Assignments (48-Pin QFN)

5.2. Package Identification

Green package is indicated by the 'G' in GXXXV (Figure 8).

5.3. RTL8211FS(I)-VS Pin Assignments

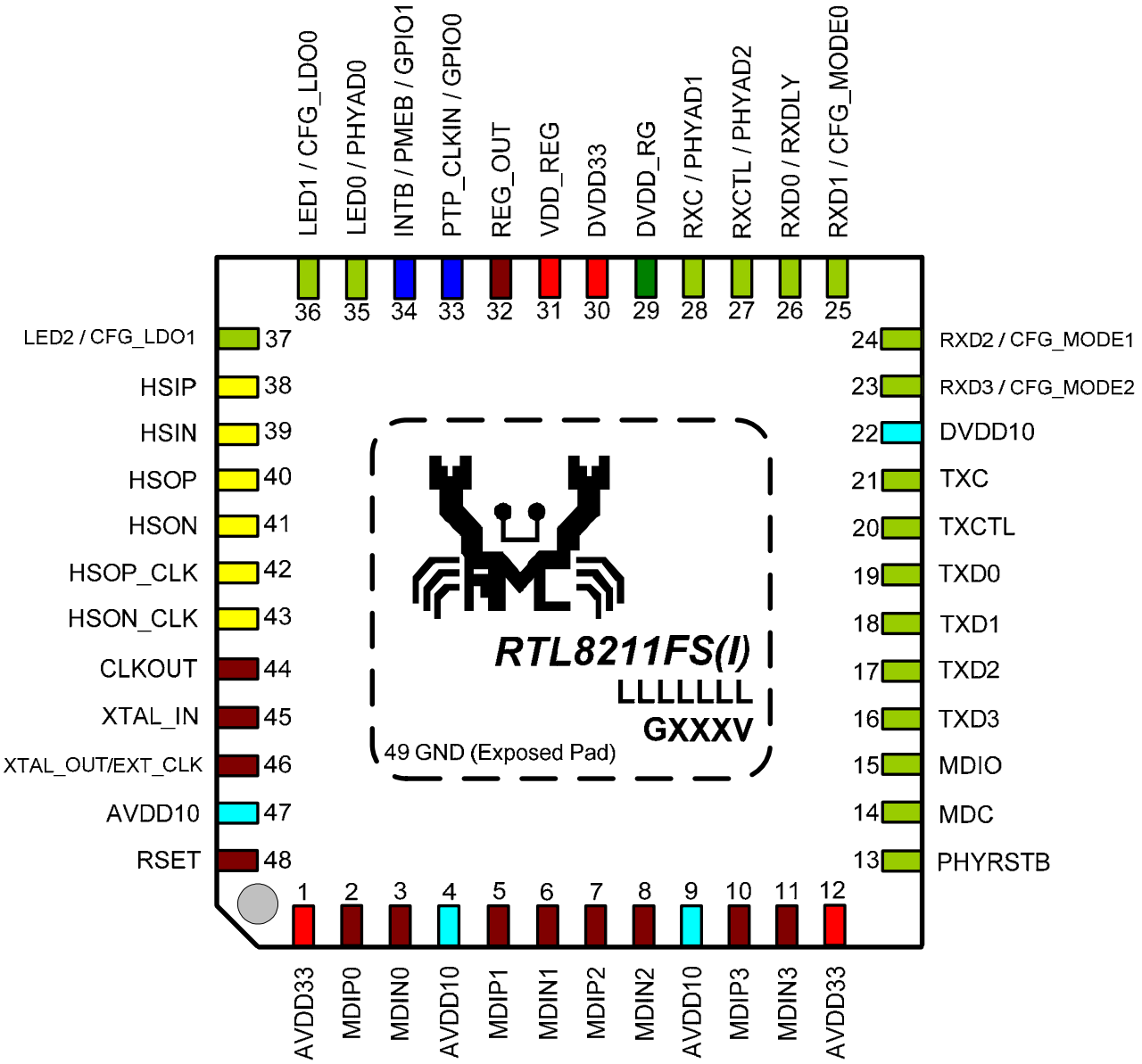


Figure 9. RTL8211FS(I)-VS Pin Assignments (48-Pin QFN)

5.4. Package Identification

Green package is indicated by the 'G' in GXXXV (Figure 9). The version number is shown in the location marked 'V'.

6. Pin Descriptions

Some pins have multiple functions. Refer to the Pin Assignment figures for a graphical representation.

I:	Input	LI:	Latched Input During Power up or Hardware Reset
O:	Output	IO:	Bi-Directional Input and Output
P:	Power	PD:	Internal Pull Down During Power On Reset
PU:	Internal Pull Up During Power On Reset	OD:	Open Drain
G:	Ground		

6.1. Transceiver Interface

Table 1. Transceiver Interface

Pin No.	Pin Name	Type	Description
2	MDIP0	IO	In MDI mode, this is the first pair in 1000Base-T, i.e., the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX.
3	MDIN0	IO	
5	MDIP1	IO	In MDI mode, this is the second pair in 1000Base-T, i.e., the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX.
6	MDIN1	IO	
7	MDIP2	IO	In MDI mode, this is the third pair in 1000Base-T, i.e., the BI_DC+/- pair. In MDI crossover mode, this pair acts as the BI_DD+/- pair.
8	MDIN2	IO	
10	MDIP3	IO	In MDI mode, this is the fourth pair in 1000Base-T, i.e., the BI_DD+/- pair. In MDI crossover mode, this pair acts as the BI_DC+/- pair.
11	MDIN3	IO	

Note: BI_DA+/-, BI_DB+/-, BI_DC+/-, BI_DD+/- means the logical wire-pairs as described in section 40.1.3 of the IEEE 802.3-2008 standard.

6.2. Clock

Table 2. Clock

Pin No.	Pin Name	Type	Description
45	XTAL_IN	I	25MHz Crystal Input. Connect to GND if an external 25MHz oscillator drives XTAL_OUT/EXT_CLK pin.
46	XTAL_OUT/ EXT_CLK	O	25MHz Crystal Output. If a 25MHz oscillator is used, connect XTAL_OUT/EXT_CLK pin to the oscillator's output (see section 10.3, page 78 for clock source specifications).
44	CLKOUT	O	1. Reference Clock Generated from Internal PLL. This pin should be kept floating if the clock is not used by the MAC. 2. UTP recovery receive clock for Sync Ethernet. 3. Fiber recovery receive clock for Sync Ethernet. 4. PTP synchronized clock output. *Note: The above sources of CLKOUT pin can be selected via Page 0xa43, Reg 25, bit[13:12], see section 8.5.17, page 51.*

6.3. RGMII

Table 3. RGMII

Pin No.	Pin Name	Type	Description
21	TXC	I	The transmit reference clock will be 125MHz, 25MHz, or 2.5MHz depending on speed.
19	TXD0	I	Transmit Data. Data is transmitted from MAC to PHY via TXD[3:0].
18	TXD1	I	
17	TXD2	I	
16	TXD3	I	
20	TXCTL	I	Transmit Control Signal from the MAC.
28	RXC	O/LI/PD	The continuous receive reference clock will be 125MHz, 25MHz, or 2.5MHz, and is derived from the received data stream.
26	RXD0	O/LI/PU	Receive Data. Data is transmitted from PHY to MAC via RXD[3:0].
25	RXD1	O/LI/PD	
24	RXD2	O/LI/PD	
23	RXD3	O/LI/PD	
27	RXCTL	O/LI/PD	Receive Control Signal to the MAC.

6.4. SerDes

Table 4. SerDes

Pin No.	Pin Name	Type	Description
38	HSIP	I	SerDes Differential Input: 1.25GHz serial interfaces to receive data from an External device that supports the SGMII interface. The differential pair has an internal 100-ohm termination resistor.
39	HSIN	I	
40	HSOP	O	SerDes Differential Output: 1.25GHz serial interfaces to transfer data to an External device that supports the SGMII interface. The differential pair has an internal 100-ohm termination resistor.
41	HSON	O	
42	HSOP_CLK	O	SerDes Receive CLK Pair. 625MHz differential serial clock output. The differential pair has an internal 100-ohm termination resistor.
43	HSON_CLK	O	

6.5. Reset

Table 5. Reset

Pin No.	Pin Name	Type	Description
13	PHYRSTB	I/PU	Hardware Reset. Active low. For a complete PHY reset, this pin must be asserted low for at least 10ms. All registers will be cleared after a hardware reset.

Note: See section 7.19, page 36 for more details.

6.6. Mode Selection (Hardware Configuration)

Table 6. Mode Selection

Pin No.	Pin Name	Type	Description
35	PHYAD0	O/LI/PU	PHYAD[2:0]: PHY Address Configuration.
28	PHYAD1	O/LI/PD	
27	PHYAD2	O/LI/PD	
26	RXDLY	O/LI/PU	RGMII Receiver Clock Timing Control. Pull up to add 2ns delay to RXC for RXD latching. *Note: Enabling of TXDLY is via register setting: Page 0xd08, Reg 17, Bit[8] = 1.*
36	CFG_LDO0	O/LI/PU	CFG_LDO[1:0]: Voltage Selection for the RGMII I/O Pad. 2'b00: 3.3V. 2'b01: 2.5V. 2'b10: 1.8V. 2'b11: 1.5V.
37	CFG_LDO1	O/LI/PD	
25	CFG_MODE0	O//LI PD	CFG_MODE[2:0]: Operation Mode Configuration. 3'b000: UTP ←→ RGMII 3'b001: FIBER ←→ RGMII 3'b010: UTP/FIBER ←→ RGMII (Media Auto Detection) 3'b011: UTP ←→ SGMII 3'b100: SGMII (PHY side) ←→ RGMII (MAC side) 3'b101: SGMII (MAC side) ←→ RGMII (PHY side) 3'b110: UTP ←→ FIBER (Media Conversion auto mode) 3'b111: UTP ←→ FIBER (Media Conversion force mode) *Note: See section 3 System Applications, page 3, for illustration.*
24	CFG_MODE1	O//LI PD	
23	CFG_MODE2	O//LI PD	

Note: For more information, see section 7.10 Hardware Configuration page 22.

6.7. LED Default Settings

Table 7. LED Default Settings

Pin No.	Pin Name	Type	Description
35	LED0	O/LI/PU	High=Link Up at 10Mbps Blinking=Transmitting or Receiving.
36	LED1	O/LI/PU	Low=Link Up at 100Mbps Blinking=Transmitting or Receiving.
37	LED2	O/LI/PD	High=Link Up at 1000Mbps Blinking=Transmitting or Receiving.

Note 1: High/Low active depends on hardware configuration pins setting (see section 7.11, page 23).
Note 2: See section 7.16 LED Configuration, page 33 for more LED setting details.

6.8. Regulator and Reference

Table 8. Regulator and Reference

Pin No.	Pin Name	Type	Description
48	RSET	O	Reference (External Resistor Reference).
32	REG_OUT	O	Switching Regulator 1.0V Output. Connect to a 2.2µH inductor.

6.9. Power and Ground

Table 9. Power and Ground

Pin No.	Pin Name	Type	Description
30	DVDD33	P	Digital non-RGMII I/O Power. 3.3V.
31	VDD_REG	P	3.3V Power for Switching Regulator.
29	DVDD_RG	P	Digital RGMII I/O Pad Power.
22	DVDD10	P	Digital Core Power. 1.0V.
1, 12	AVDD33	P	Analog Power. 3.3V.
4, 9,47	AVDD10	P	Analog Power. 1.0V.
49	GND	G	Ground. Exposed Pad (E-Pad) is Analog and Digital Ground (see section 11 Mechanical Dimensions, page 90).

6.10. Management and PTP Application Interface

**Note: The definitions of pin 33 and 34 depend on the products, i.e. RTL8211FS(I) or RTL8211FS(I)-VS.*

Table 10. Management Interface

Pin No.	Product	Pin Name	Type	Description
14	All	MDC	I	Management Data Clock.
15	All	MDIO	IO/PU	Input/Output of Management Data. Pull up 3.3/2.5/1.8/1.5V for 3.3/2.5/1.8/1.5V I/O, respectively.
33	RTL8211FS(I)	NC	-	Not Connected.
	RTL8211FS(I)-VS	PTP_CLKIN/ GPIO0	I/O	1. PTP clock input from the external reference clock source. *Note: See section 8.5.31, page 57 for enabling the PTP clock input function information.* 2. PTP GPIO_0.
34	RTL8211FS(I)	INTB/PMEB	O/OD	This pin is shared by two functions, keep this pin floating if either of the functions is not used. 1. Interrupt (supports 3.3V pull up). Set low if the specified events occurred; active low. 2. Power Management Event (supports 3.3V pull up). Set low if received a magic packet, Wake-Up frame, or wake up event;; active low. *Note 1: The behavior of this pin is level-triggered.* *Note 2: The function of this pin (INTB/PMEB) can be assigned by Page 0xd40, Reg.22, bit[5]:* *1: Pin 34 functions as PMEB.* *0: Pin 34 functions as INTB (default)* *Note 3:For more detailed INTB/PMEB usage, see section 7.8, page 21.*

	RTL8211FS(I)-VS	INTB/PMEB GPIO1	O/OD I/O	This pin is shared by three functions, the default pin setting is INTB. Keep this pin floating if either of the functions is not used. The pin type depends on function selected: 1. Interrupt (supports 3.3V pull up). Set low if the specified events occurred; active low. 2. Power Management Event (supports 3.3V pull up). Set low if received a magic packet, Wake-Up frame ,or wake up event; active low. *Note 1: The behavior of INTB/PMEB is level-triggered.* *Note 2: The function of INTB/PMEB can be assigned by Page 0xd40, Reg.22, bit[5]:* *1: Pin 34 functions as PMEB.* *0: Pin 34 functions as INTB (default)* *Note 3:For more detailed INTB/PMEB usage, see* section 7.8, page 21. 3. PTP GPIO_1. *Note: Only when setting INTBCR register (Page 0xd40, Reg 22, bit[2:0] = 3'b101, see section 8.5.26, page 55) and PTP_TAI_CFG register (Page 0xe42, Reg 16, bit[4:3] = 2'b01, see section 8.5.37, page 59), this pin will function as a PTP GPIO_1,. This configuration has higher priority than the INTB/PMEB function.*

7. Function Description

7.1. Transmitter

7.1.1. 1000Mbps Mode

The RTL8211FS(I)(-VS)'s PCS layer receives data bytes from the MAC through the SGMII/RGMII interface and performs generation of continuous code-groups through 4D-PAM5 coding technology. These code groups are passed through a waveform-shaping filter to minimize EMI effect, and are transmitted onto the 4-pair CAT.5 cable at 125MBaud/s through a D/A converter.

7.1.2. 100Mbps Mode

The transmitted 4-bit nibbles (TXD[3:0]) from the MAC, clocked at 25MHz (TXCLK), are converted into 5B symbol code through 4B/5B coding technology, then through scrambling and serializing, are converted to 125MHz NRZ and NRZI signals. The NRZI signals are passed to the MLT3 encoder, then to the D/A converter and transmitted onto the media.

7.1.3. 10Mbps Mode

The transmit 4-bit nibbles (TXD[3:0]) from the MAC, clocked at 2.5MHz (TXCLK), are serialized into 10Mbps serial data. The 10Mbps serial data is converted into a Manchester-encoded data stream and is transmitted onto the media by the D/A converter.

7.2. Receiver

7.2.1. 1000Mbps Mode

Input signals from the media first pass through the on-chip sophisticated hybrid circuit to subtract the transmitted signal from the input signal for effective reduction of near-end echo. The received signal is processed with state-of-the-art technology, such as adaptive equalization, BLW (Baseline Wander) correction, cross-talk cancellation, echo cancellation, timing recovery, error correction, and 4D-PAM5 decoding. The 8-bit-wide data is recovered and is sent to the SGMII/RGMII interface at a clock speed of 125MHz. The Rx MAC retrieves the packet data from the receive SGMII/RGMII interface and sends it to the Rx Buffer Manager.

7.2.2. 100Mbps Mode

The MLT3 signal is processed with an ADC, equalizer, BLW (Baseline Wander) correction, timing recovery, MLT3 and NRZI decoder, descrambler, 4B/5B decoder, and is then presented to the SGMII/RGMII interface in 4-bit-wide nibbles at a clock speed of 25MHz.

7.2.3. 10Mbps Mode

The received differential signal is converted into a Manchester-encoded stream first. Next, the stream is processed with a Manchester decoder, and is de-serialized into 4-bit-wide nibbles. The 4-bit nibbles are presented to the SGMII/RGMII interface at a clock speed of 2.5MHz.

7.3. Precision Time Protocol (PTP) (RTL8211FS(I)-VS Only)

Precision Time Protocol (PTP) stands for a series of IEEE specifications, including IEEE 1588 Ver. 1, IEEE 1588 Ver. 2, and IEEE 802.1AS, that synchronize the time of day or a standard time across a network system. The PTP protocol is typically used in Audio Video Bridging (AVB) applications, industrial and factory automation applications, or test and measurement systems.

The fundamental concept of PTP is time-stamping specified PTP frames with high precision as close to the transmission media as possible. Time stamping in the PHY provides increased accuracy compared to time-stamping in the MAC or higher layers.

The PTP core in the RTL8211FS(I)-VS consists of three main blocks:

- Packet Time Stamping
- Synchronized PTP Clock
- Time Application Interface (TAI)

By combining the above functions, the RTL8211FS(I)-VS provides complete and accurate support for applications in a time-synchronous system.

The PTP features of the RTL8211FS(I)-VS are briefly introduced below. For more detailed configuration of PTP functions, refer to the RTL8211FS(I)-VS PTP Application Note.

7.3.1. Synchronized PTP Clock

Based on the PTP specification requirements, the integrated PTP clock of the RTL8211FS(I)-VS consists of the following time fields: seconds (48 bits), nanoseconds (30 bits), and fractional nanoseconds (in units of 2^{-32} ns).

The RTL8211FS(I)-VS provides several ways to access and update this internal PTP clock. The methods are listed below:

- Direct Read/Write
- Step Adjustment
- Rate Adjustment

A Direct Write of the time value is done by setting a new value to all time fields. This function may be used when initializing a PTP synchronization that needs an immediate setting to a time value due to the local PTP time being far different to the Master clock time.

A Step Adjustment is an alternative method for making quick compensation to the PTP clock time. Note that the adjustment can be incremented and decremented.

When the local time is close to the PTP Master, Rate Adjustment is the better way to fine-tune the time setting. The Rate Adjustment allows for correction on the order of 2^{-32} ns per clock cycle. It can correct the offset over time accurately.

Refer to section 8.5.31, page 57, for detailed register settings.

7.3.2. Packet Time Stamping

The PTP packet parser in the RTL8211FS(I)-VS continually monitors transmit/receive packet data in order to detect IEEE 1588 Ver. 1, Ver 2 or 802.1AS Event Messages. The PTP packets transported in Layer 2 Ethernet, IPv4/UDP, or IPv6/UDP packet formats can be recognized accordingly. Upon detection of a PTP Event Message, the RTL8211FS(I)-VS will capture the specific transmit/receive timestamp and provide it to the software at the upper layer through PTP_TRX_TS registers (see section 8.5.44 to 8.5.52, page 62~65). A PTP interrupt can be generated, if enabled, upon a transmit/receive timestamp ready.

In some transmission cases, the RTL8211FS(I)-VS supports One-Step operation: The egress timestamp of a Sync message is on-the-fly inserted to the Sync itself, with no need for Follow-Up messages.

A Hardware-assisted Timestamp Insertion feature is imbedded, which will insert receive timestamps directly into the next Follow-Up/Delay-Response packets via hardware; software does not need to access timestamp registers.

After gathering the timestamp information, the upper layer software can compute the difference between the local time and the PTP Master's central clock time, and use the three methods in section 7.3.1 to tune the local PTP clock, in order to match the master clock.

7.3.3. Time Application Interface (TAI)

When the end-point's PTP clock is synchronized to the PTP Master clock, its time information and local clock can be provided to peripheral time applications that need to work simultaneously with the central clock. The RTL8211FS(I)-VS features these time application interfaces in the following, via the PTP GPIOs and CLKOUT pins:

Event Capture interface:

- Monitors the selected GPIO, and records the timestamp of incoming pulses, edges, or time alignment signals, similar to a stopwatch.

Trigger Generate interface:

- Arms the selected GPIO to generate a pulse, edge, or periodic clock signal at a specific time, similar to an alarm clock. The periodic clock has configurable period and duty cycles.
- Low-jitter synchronized 1588 clock output with frequency of 25M/125 MHz via the CLKOUT pin.
- PTP clock input from the external reference clock source with 10M/25M/125MHz via GPIO0.

The related TAI configurations can be set by PTP_TAI registers (section 8.5.37, page 59).

7.4. Synchronous Ethernet (Sync-E)

The RTL8211FS(I)-VS provides Synchronous Ethernet (Sync-E) support when the device is operating in 1000Base-T, 100Base-TX, 1000Base-X, and 100Base-FX on the transmission media. The CLKOUT pin can be assigned to output the recovered clock. Refer to section 8.5.17, page 51 (PHYCR2 register) for clock output configuration details.

The recovery clock for Sync-E can be either a 125MHz or a 25MHz clock, which is also determined by the PHYCR2 register.

When the PHY is in SLAVE mode, the CLKOUT will output the recovered clock from the MDI. If the device is in MASTER mode, the CLKOUT will output the clock based on the local free run PLL.

PTP and Sync-E can be used simultaneously so as to provide better time synchronization performance.

7.5. Energy Efficient Ethernet (EEE)

The RTL8211FS(I)(-VS) supports IEEE 802.3az-2010, also known as Energy Efficient Ethernet (EEE), at 10Mbps, 100Mbps, and 1000Mbps. It provides a protocol to coordinate transitions to/from a lower power consumption level (Low Power Idle mode) based on link utilization. When no packets are being transmitted, the system goes to Low Power Idle mode to save power. Once packets need to be transmitted, the system returns to normal mode, and does this without changing the link status and without dropping/corrupting frames.

To save power, when the system is in Low Power Idle mode, most of the circuits are disabled, however, the transition time to/from Low Power Idle mode is kept small enough to be transparent to upper layer protocols and applications.

EEE also specifies a negotiation method to enable link partners to determine whether EEE is supported.

Refer to http://www.ieee802.org/3/az/index.html for more details.

7.6. Wake-On-LAN (WOL)

The RTL8211FS(I)(-VS) can monitor the network for a Wake-Up Frame or a Magic Packet, and notify the system via the PMEB (Power Management Event; 'B' means low active) pin when such a packet or event occurs[1]. The system can then be restored to a normal state to process incoming jobs. The PMEB pin needs to be connected with a 4.7k-ohm resistor and pulled up to 3.3V. When the Wake-Up Frame or a Magic Packet is sent to the PHY, the PMEB pin will be set low to notify the system to wake up. Refer to the RTL8211F_Series_WOL_App_Note for details.

Magic Packet Wake-up occurs only when the following conditions are met:

- The destination address of the received Magic Packet is acceptable to the RTL8211FS(I)(-VS), e.g., a broadcast, multicast, or unicast packet addressed to the current RTL8211FS(I)(-VS).
- The received Magic Packet does not contain a CRC error.
- The Magic Packet pattern matches; i.e., 6 * FFh + MISC (can be none) + 16 * DID (Destination ID) in any part of a valid Ethernet packet.

A Wake-Up Frame event occurs only when the following conditions are met:

- The destination address of the received Wake-Up Frame is acceptable to the RTL8211FS(I)(-VS), e.g., a broadcast, multicast, or unicast address to the current RTL8211FS(I)(-VS).
- The received Wake-Up Frame does not contain a CRC error.
- The 16-bit CRC[2] of the received Wake-Up Frame matches the 16-bit CRC of the sample Wake-Up Frame pattern given by the local machine's OS. Or, the RTL8211FS(I)(-VS) is configured to allow direct packet wakeup, e.g., a broadcast, multicast, or unicast network packet. Non-specific packets are also supported.

Note 1: The INTB and PMEB functions share the same pin (pin 34), and can be determined by Page 0xd40, Reg.22, bit[5].

Note 2: 16-bit CRC: The RTL8211FS(I)(-VS) supports eight long Wake-Up frames (covering 128 mask bytes from offset 0 to 127 of any incoming network packet). CRC16 polynomial=$x^{16}+x^{12}+x^{5}+1$.

7.7. Interrupt

The RTL8211FS(I)(-VS) provides an active low interrupt output pin (INTB) based on change of the PHY status. Every interrupt condition is represented by the read-only general interrupt status register (section 8.5.19 INSR (Interrupt Status Register, Page 0xa43, Address 0x1D), page 52), PTP interrupt status register (section 8.5.29 PTP_INSR (PTP Interrupt Status Register, Page 0xe40, Address 0x12), page 56), and SERDES interrupt status register (section 8.5.65 SERDES INSR (SERDES Interrupt Status Register, Page 0xde1, Address 0x12), page 72).

The interrupts can be individually enable or disable by setting or clearing bits in the interrupt enable register (section 8.5.15 INER (Interrupt Enable Register, Page 0xa42, Address 0x12), page 49), PTP interrupt enable register (section 8.5.28 PTP_INER (PTP Interrupt Enable Register, Page 0xe40, Address 0x11), page 56), and SERDES interrupt enable register (section 8.5.64 SERDES INER (SERDES Interrupt Enable Register, Page 0xde1, Address 0x11), page 72). When an enabled interrupt condition occurs, the interrupt pin is driven low, and the interrupts are self-cleared (INTB pin de-asserted) by reading the corresponding interrupt status registers through MDC/MDIO interface.

Note 1: The interrupt of the RTL8211FS(I)(-VS) is a level-triggered mechanism.
Note 2: The INTB and PMEB functions share the same pin (pin 34), and can be determined by Page 0xd40, Reg.22, bit[5].

7.8. INTB/PMEB Pin Usage

The INTB/PMEB pin (pin 34) of the RTL8211FS(I)(-VS) is designed to notify in cases of both interrupt and WOL events. The default mode of this pin is INTB (Page 0xd40, Reg.22, bit[5] = 0). For general use, indication of a WOL event is also integrated into one of the interrupt events (Page 0xa42, Reg 18, bit[7] which is triggered when any specified WOL event occurs. However, the 'Pulse Low' waveform format is not supported during this mode; only the Active Low, level-triggered waveform is provided. Refer to section 6.1 in the RTL8211F_Series_WOL_App_Note for more information.

If PMEB mode is selected (Page 0xd40, Reg.22, bit[5] = 1), pin 34 becomes a fully functional PMEB pin. Note that the interrupt function is disabled in this mode.

7.9. MDI Interface

This interface consists of four signal pairs; MDI0, MDI1, MDI2, and MDI3. Each signal pair consists of two bi-directional pins that can transmit and receive at the same time. The MDI interface has internal termination resistors to reduce BOM cost and PCB complexity. For 1000Base-T, all four pairs are used in both directions at the same time. For 10/100Mbps links and during auto-negotiation, only pairs MDI0 and MDI1 are used.

7.10. Hardware Configuration

The I/O pad voltage, interface mode, and PHY address can be set by the CONFIG pins. The respective value mapping of CONFIG with the configurable vector is listed in Table 11. To set the CONFIG pins, an external pull-high or pull-low via resistor is required.

Table 11. CONFIG Pins vs. Configuration Register

CONFIG Pin	Configuration
LED0	PHYAD[0]
RXC	PHYAD[1]
RXCTL	PHYAD[2]
RXD0	RXDLY
LED1	CFG_LDO[0]
LED2	CFG_LDO[1]
RXD1	CFG_MODE[0]
RXD2	CFG_MODE[1]
RXD3	CFG_MODE[2]

Table 12. Configuration Register Definitions

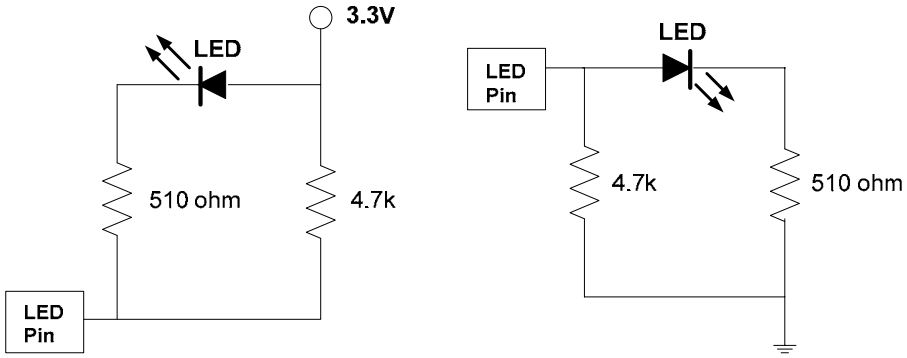
Configuration	Description
PHYAD[2:0]	PHY Address. PHYAD sets the PHY address for the device. TheRTL8211FS(I)(-VS) supports PHY addresses from 0x01 to 0x07. *Note 1: An MDIO command with PHY address=0 is a broadcast from the MAC; each PHY device should respond. This function can be disabled by setting Page 0xa43, Reg24, bit[13]=0 (see section 8.5.16, page 50).* *Note 2: The RTL8211FS(I)(-VS) with PHYAD[2:0]=000 can automatically remember the first non-zero PHY address. This function can be enabled by setting Page 0xa43, Reg24, bit[6] = 1 (see section 8.5.16, page 50).*
RXDLY	RGMII Receive Clock Timing Control. 1: Add 2ns delay to RXC for RXD latching (via 4.7k-ohm to DVDD_RG) 0: No delay (via 4.7k-ohm to GND) *Note: Enabling of TXDLY is left in the register setting: Page 0xd08, Reg 17, Bit[8] = 1.*
CFG_LDO[1:0]	Voltage Selection for I/O pad 00: 3.3V 01: 2.5V 10: 1.8V 11: 1.5V *Note: When CFG_LDO[1:0] = 00, the I/O pad power is supplied from the external 3.3V power connected to DVDD_RG pin; Otherwise, it is supplied from the internal LDO.*

Configuration	Description
CFG_MODE[2:0]	The RTL8211FS(I)(-VS) Operating Mode Selection. 000: UTP ←→ RGMII 001: FIBER ←→ RGMII 010: UTP/FIBER ←→ RGMII (Media Auto Detection) 011: UTP ←→ SGMII 100: SGMII (PHY side) ←→ RGMII (MAC side) 101: SGMII (MAC side) ←→ RGMII (PHY side) 110: UTP ←→ FIBER (Media Conversion auto mode) 111: UTP ←→ FIBER (Media Conversion force mode)

7.11. LED and PHY Address/LDO Configuration

In order to reduce the pin count on the RTL8211FS(I)(-VS), the LED pins are duplexed with the PHYAD0 and CFG_LDO[1:0] pins. As the Hardware Configuration shares the LED output pins, the external combinations required for strapping and LED usage must be considered in order to avoid contention. Specifically, when the LED outputs are used to drive LEDs directly, the active state of each output driver is dependent on the logic level sampled by the corresponding PHYAD0/CFG_LDO[1:0] inputs upon power-on/reset.

For example, as Figure 10 (left-side) shows, if a given PHYAD0/CFG_LDO inputs are resistively pulled high then the corresponding LED outputs will be configured as an active low driver. On the right side, we can see that if a given PHYAD0/CFG_LDO[1:0] input is resistively pulled low then the corresponding output will be configured as an active high driver. The Hardware Configuration pins should not be connected to GND or VCC directly, but must be pulled high or low through a resistor (e.g., 4.7KΩ). If no LED indications are needed, the components of the LED path (LED+510Ω) can be removed.



CFG_LDO[1:0] = Logical 1
PHYAD0 = Logical 1
LED Indication = Active low

CFG_LDO[1:0] = Logical 0
PHYAD0 = Logical 0
LED Indication = Active High

Figure 10. LED and PHY Address/LDO Configuration

7.12. Green Ethernet (1000/100Mbps Mode Only)

7.12.1. Cable Length Power Saving

In 1000/100Mbps mode the RTL8211FS(I)(-VS) provides dynamic detection of cable length and dynamic adjustment of power required for the detected cable length. This feature provides intermediate performance with minimum power consumption.

7.12.2. Register Setting

Follow the register settings below to DISABLE Green Ethernet (Default is 'Enabled')

Write Page 0xa43, Reg 27, Data=0x8011

Write Page 0xa43, Reg 28, Data=0x573f

Follow the register settings below to ENABLE Green Ethernet (Default is 'Enabled')

Write Page 0xa43, Reg 27, Data=0x8011

Write Page 0xa43, Reg 28, Data=0xd73f

7.13. MAC/PHY Interface

The RTL8211FS(I)(-VS) supports industry standards and is suitable for most off-the-shelf MACs with an SGMII/RGMII interface.

7.13.1. RGMII

Among the RGMII interface in 100Base-TX and 10Base-T modes, TXC and RXC sources are 25MHz and 2.5MHz respectively; while in 1000Base-T mode, TXC and RXC sources are 125MHz. TXC will always be generated by the MAC and RXC will always be generated by the PHY. TXD[3:0] and RXD[3:0] signals are used for data transitions on the rising and falling edge of the clock.

7.13.2. SGMII

The Serial Gigabit Media Independent Interface (SGMII) is a standard interface which is used to carry frame data and link status information between a PHY and an Ethernet MAC. The SGMII uses a differential pair for data and clock signals to provide signal integrity while minimizing system noise. The data signals operate at 1.25G/baud and the clocks operate as a 625MHz double data rate (DDR) interface.

7.13.3. Management Interface

The management interface provides access to the internal registers through the MDC and MDIO pins as described in IEEE 802.3u section 22. The MDC signal, provided by the MAC, is the management data clock reference to the MDIO signal. The MDIO is the management data input/output and is a bi-directional signal that runs synchronously to MDC. The MDIO pin needs a 1.5k Ohm pull-up resistor to maintain the MDIO high during idle and turnaround.

The RTL8211FS(I)(-VS) can share the same MDIO line. In switch/router applications, each port should be assigned a unique address during the hardware reset sequence, and it can only be addressed via that unique PHY address. For detailed information on the management registers, see section 8 Register Descriptions, page 37.

Table 13. Management Frame Format

	Management Frame Fields							
	Preamble	**ST**	**OP**	**PHYAD**	**REGAD**	**TA**	**DATA**	**IDLE**
Read	1…1	01	10	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDD	Z
Write	1…1	01	01	AAAAA	RRRRR	10	DDDDDDDDDDDDDDDD	Z

Table 14. Management Frame Description

Name	Description
Preamble	32 Contiguous Logical 1's Sent by the MAC on MDIO, along with 32 Corresponding Cycles on MDC. This provides synchronization for the PHY.
ST	Start of Frame. Indicated by a 01 pattern.

Name	Description
OP	Operation Code. Read: 10 Write: 01
PHYAD	PHY Address. Up to eight PHYs can be connected to one MAC. This 3-bit field selects which PHY the frame is directed to.
REGAD	Register Address. This is a 5-bit field that sets which of the 32 registers of the PHY this operation refers to.
TA	Turnaround. This is a 2-bit-time spacing between the register address and the data field of a frame to avoid contention during a read transaction. For a read transaction, both the STA and the PHY remain in a high-impedance state for the first bit time of the turnaround. The PHY drives a zero bit during the second bit time of the turnaround of a read transaction.
DATA	Data. These are the 16 bits of data.
IDLE	Idle Condition. Not truly part of the management frame. This is a high impedance state. Electrically, the PHY's pull-up resistor will pull the MDIO line to a logical '1'.

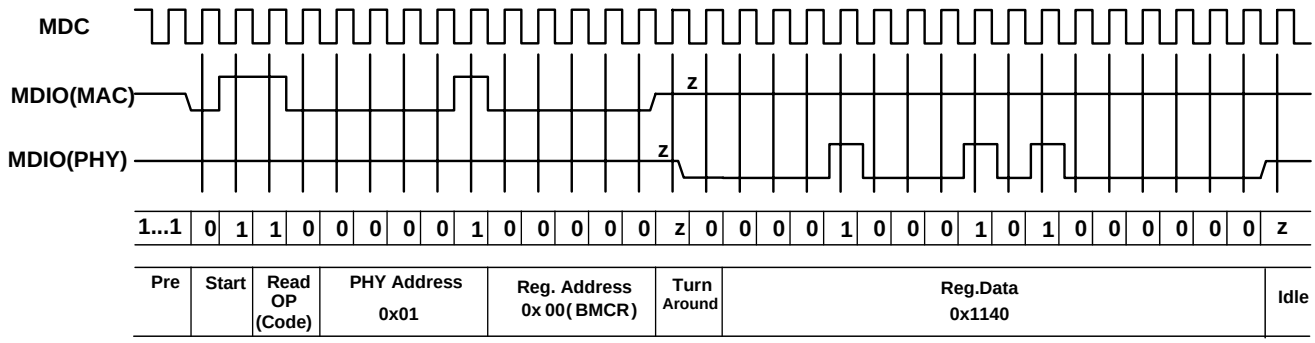


Figure 11. MDC/MDIO Read Timing

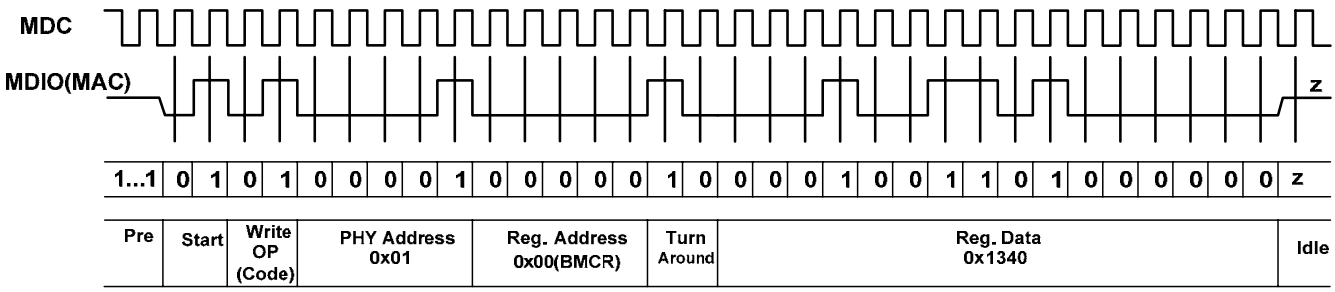


Figure 12. MDC/MDIO Write Timing

7.13.4. Change Page

Set MDIO commands as shown below in order to switch to the desired Page 0xXYZ (in Hex).

1. Write Register 31 Data = 0x0XYZ (Page 0xXYZ)

2. Read/Write the target Register Data

3. Write Register 31 Data = 0x0000 or 0xa42 (switch back to IEEE Standard Registers)

7.13.5. Access to MDIO Manageable Device (MMD)

The MDIO Manageable Device (MMD) is an extension to the management interface that provides the ability to access more device registers while still retaining logical compatibility with the MDIO interface, defined in Table 22, page 39. Access to MMD configuration is provided via Registers 13 and 14.

MMD Read/Write Operation

1. Write Function field to 00 (address mode) and DEVAD field to the device address value for the desired MMD (Register 13).

2. Write the desired address value to the MMD's address register (Register 14).

3. Write Function field to 01 (data mode; no post increment) and DEVAD field to the same device address for the desired MMD (Register 13).

4. Read: Go to step 5. Write: Go to step 6.

5. Read the content of the selected register in MMD (Register 14).

6. Write the content of the selected register in MMD (Register 14).

7.14. Auto-Negotiation

Auto-Negotiation is a mechanism to determine the fastest connection between two link partners. For copper media applications, it was introduced in IEEE 802.3u for Ethernet and Fast Ethernet, and then in IEEE 802.3ab to address extended functions for Gigabit Ethernet. It performs the following:

- Auto-Negotiation Priority Resolution
- Auto-Negotiation Master/Slave Resolution
- Auto-Negotiation PAUSE/ASYMMETRIC PAUSE Resolution
- Crossover Detection & Auto-Correction Resolution

Upon de-assertion of a hardware reset, the RTL8211FS(I)(-VS) can be configured to have auto-negotiation enabled, or be set to operate in 10Base-T, 100Base-TX, or 1000Base-T mode via the ANAR and GBCR register (Register 4 and 9).

The auto-negotiation process is initiated automatically upon any of the following:

- Power-up
- Hardware reset
- Software reset (Register 0.15)
- Restart auto-negotiation (Register 0.9)
- Transition from power down to power up (Register 0.11)
- Entering the link fail state

Table 15. 1000Base-T Base and Next Page Bit Assignments

Bit	Name	Bit Description	Register Location
Base Page			
D15	NP	Next Page. 1: Indicates that Next Pages follow 0: Indicates that no Next Pages follow	-
D14	Ack	Acknowledge. 1: Indicates that a device has successfully received its link partner's Link Code Word (LCW)	-
D13	RF	Remote Fault. 1: Indicates to its link partner that a device has encountered a fault condition	-
D[12:5]	A[7:0]	Technology Ability Field. Indicates to its link partner the supported technologies specific to the selector field value.	Register 4.[12:5] Table 29, page 43.
D[4:0]	S[4:0]	Selector Field. Always 00001. Indicates to its link partner that it is an IEEE 802.3 device.	Register 4.[4:0] Table 29, page 43.
PAGE 0 (Message Next Page)			
M15	NP	Next Page. 1: Indicates that Next Pages follow 0: Indicates that no Next Pages follow	-
M14	Ack	Acknowledge. 1: Indicates that a device has successfully received its link partner's Link Code Word (LCW)	-
M13	MP	Message Page. 1: Indicates to its link partner that this is a message page, not an unformatted page.	-
M12	Ack2	Acknowledge 2. 1: Indicates to its link partner that the device has the ability to comply with the message.	-

Bit	Name	Bit Description	Register Location
M11	T	Toggle. Used by the NWay arbitration function to ensure synchronization with its link partner during Next Page exchange.	-
M[10:0]	-	1000Base-T Message Code (Always 8).	-
PAGE 1 (Unformatted Next Page)			
U15	NP	Next Page. 1: Indicates that Next Pages follow 0: Indicates that no Next Pages follow	-
U14	Ack	Acknowledge. 1: Indicates that a device has successfully received its link partner's Link Code Word (LCW)	-
U13	MP	Message Page. 1: Indicates to its link partner that this is a message page, not an unformatted page.	-
U12	Ack2	Acknowledge 2. 1: Indicates to its link partner that the device has the ability to comply with the message.	-
U11	T	Toggle. Used by the NWay arbitration function to ensure synchronization with its link partner during Next Page exchange.	-
U[10:5]	-	Reserved. Transmit as 0	-
U4	-	1000Base-T Half Duplex. 1: Half duplex 0: No half duplex	-
U3	-	1000Base-T Full Duplex. 1: Full duplex 0: No full duplex	-
U2	-	1000Base-T Port Type Bit. 1: Multi-port device 0: Single-port device	Register 9.10 (GBCR) Table 34, page 46.
U1	-	1000Base-T Master-Slave Manual Configuration Value. 1: Master 0: Slave This bit is ignored if bit 9.12=0	Register 9.11 (GBCR) Table 34, page 46.
U0	-	1000Base-T Master-Slave Manual Configuration Enable. 1: Manual Configuration Enable This bit is intended to be used for manual selection in Master-Slave mode, and is to be used in conjunction with bit 9.11	Register 9.12 (GBCR) Table 34, page 46.
PAGE 2 (Unformatted Next Page)			
U15	NP	Next Page. 1: Indicates that Next Pages follow 0: Indicates that no Next Pages follow	-
U14	Ack	Acknowledge. 1: Indicates that a device has successfully received its link partner's Link Code Word (LCW)	-
U13	MP	Message Page. 1: Indicates to its link partner that this is a message page, not an unformatted page	-

Bit	Name	Bit Description	Register Location
U12	Ack2	Acknowledge 2. 1: Indicates to its link partner that the device has the ability to comply with the message	-
U11	T	Toggle. Used by the NWay arbitration function to ensure synchronization with its link partner during Next Page exchange.	-
U[10:0]	-	1000Base-T Master-Slave Seed Bit[10:0]	Master-Slave Seed Value SB[10:0]

7.14.1. Auto-Negotiation Priority Resolution

Upon the start of auto-negotiation, to advertise its capabilities each station transmits a 16-bit packet called a Link Code Word (LCW), within a burst of 17 to 33 Fast Link Pulses (FLP). A device capable of auto-negotiation transmits and receives the FLPs. The receiver must identify three identical LCWs before the information is authenticated and used in the arbitration process. The devices decode the base LCW and select capabilities with the highest common denominator supported by both devices.

To advertise 1000Base-T capability, both link partners, sharing the same link medium, should engage in Next Page (1000Base-T Message Page, Unformatted Page 1, and Unformatted Page 2) exchange.

Auto-negotiation ensures that the highest priority protocol will be selected as the link speed based on the following priorities advertised through the Link Code Word (LCW) exchange. Refer to IEEE 802.3 Clause 28 for detailed information.

1. 1000Base-T Full Duplex (highest priority)

2. 1000Base-T Half Duplex

3. 100Base-TX Full Duplex

4. 100Base-TX Half Duplex

5. 10Base-T Full Duplex

6. 10Base-T Half Duplex (lowest priority)

7.14.2. Auto-Negotiation Master/Slave Resolution

To establish a valid 1000Base-T link, the Master/Slave mode of both link partners should be resolved through the auto-negotiation process:

- Master Priority
  - Multi-port > Single-port
  - Manual > Non-manual
- Determination of Master/Slave configuration from LCW
  - Manual_MASTER=U0*U1
  - Manual_SLAVE=U0*!U1
  - Single-port device=!U0*!U2
  - Multi-port device=!U0*U2
    Where: U0 is bit 0 of the Unformatted Page 1
    U1 is bit 1 of the Unformatted Page 1
    U2 is bit 2 of the Unformatted Page 1
- Where there are two stations with the same configuration, the one with higher Master-Slave seed SB[10:0] in the unformatted page 2 shall become Master.
- Master-Slave configuration process resolution:
  - Successful: Bit 10.15 Master-Slave Configuration Fault is set to logical 0, and Bit 10.14 is set to logical 1 for Master resolution, or set to logical 0 for Slave resolution.
  - Unsuccessful: Auto-Negotiation restarts.
  - Fault Detect: Bit 10.15 is set to logical 1 to indicate that a configuration fault has been detected. Auto-Negotiation restarts automatically. This happens when both stations are set to manual Master mode or manual Slave mode, or after seven attempts to configure the Master-Slave relationship through the seed method has failed.

7.14.3. Auto-Negotiation PAUSE/ASYMMETRIC PAUSE Resolution

Auto-negotiation is also used to determine the flow control capability between link partners. Flow control is a mechanism that can force a busy transmitting link partner to stop transmitting in a full duplex environment by sending special MAC control frames. In IEEE 802.3u, a PAUSE control frame had already been defined. However, in IEEE 802.3ab, a new ASY-PAUSE control frame was defined; if the MAC can only generate PAUSE frames but is not able to respond to PAUSE frames generated by the link partner, then it is called ASYMMETRIC PAUSE.

PAUSE/ASYMMETRIC PAUSE capability can be configured by setting the ANAR bits 10 and 11 (Table 29, page 43). Link partner PAUSE capabilities can be determined from ANLPAR bits 10 and 11 (Table 30, page 44). A PHY layer device such as the RTL8211FS(I)(-VS) is not directly involved in PAUSE resolution, but simply advertises and reports PAUSE capabilities during the Auto-Negotiation process. The MAC is responsible for final PAUSE/ASYMMETRIC PAUSE resolution after a link is established, and is responsible for correct flow control actions thereafter.

7.15. Crossover Detection and Auto-Correction

Ethernet needs a crossover mechanism between both link partners to cross the transmit signal to the receiver when the medium is twisted-pair cable. Crossover Detection & Auto-Correction Configuration eliminates the need for crossover cables between devices, such as two computers connected to each other with a CAT.5 Ethernet cable. The basic concept is to assume the initial default setting is MDI mode, and then check the link status. If no link is established after a certain time, change to MDI Crossover mode and repeat the process until a link is established. An 11-bit pseudo-random timer is applied to decide the mode change time interval.

Crossover Detection & Auto-Correction is not a part of the Auto-Negotiation process, but it utilizes the process to exchange the MDI/MDI Crossover configuration. If the RTL8211FS(I)(-VS) is configured to only operate in 100Base-TX or only in 10Base-T mode, then Auto-Negotiation is disabled only if the Crossover Detection & Auto-Correction function is also disabled. If Crossover Detection & Auto-Correction are enabled, then Auto-Negotiation is enabled and the RTL8211FS(I)(-VS) advertises only 100Base-TX mode or 10Base-T mode. If the speed of operation is configured manually and Auto-Negotiation is still enabled because the Crossover Detection & Auto-Correction function is enabled, then the duplex advertised is as follows:

1. If it is set to half duplex, then only half duplex is advertised.

2. If it is set to full duplex, then both full and half duplex are advertised.

If the user wishes to advertise only full duplex at a particular speed with the Crossover Detection & Auto-Correction function enabled, then Auto-Negotiation should be enabled (Register 0.12) with the appropriate advertising capabilities set in registers 4 or 9. The Crossover Detection & Auto-Correction function may be enabled/disable by setting (Page 0xa43, Reg 24, bit[9:8]) manually, see section 8.5.16, page 50.

After initial configuration following a hardware reset, Auto-Negotiation can be enabled and disabled via Register 0.12, speed via Registers 0.13, 0.6, and duplex via Register 0.8. The abilities that are advertised can be changed via Registers 4 and 9. Changes to Registers 0.12, 0.13, 0.6, and 0.8 do not take effect unless at least one of the following events occurs:

- Software reset (Register 0.15)
- Restart of Auto-Negotiation (Register 0.9)
- Transition from power-down to power-up (Register 0.11)

Registers 4 and 9 are internally latched once each time Auto-Negotiation enters the ABILITY DETECT state in the arbitration state machine (IEEE 802.3 Clause 28). Hence a write into Register 4 or 9 has no effect once the RTL8211FS(I)(-VS) begins to transmit Fast Link Pulses.

Register 7 is treated in a similar manner as 4 and 9 during additional Next Page exchanges. Once the RTL8211FS(I)(-VS) completes Auto-Negotiation, it updates the various statuses in Registers 1, 5, 6, and 10. The speed, duplex, page received, and Auto-Negotiation completed statuses are also available in Page 0xa43, Reg 26 and 29 (Reg 29 is valid after enabling the interrupts in Page 0xa42, Reg 18).

7.16. LED Configuration

7.16.1. Customized LED Function

The RTL8211FS(I)(-VS) supports three LED pins, suitable for multiple types of applications that can directly drive the LEDs. The output of these pins is determined by setting the corresponding bits in Page 0xd04 Register 16 and 18 (see section 8.5.22, page 53 and 8.5.24, page 54). The functionality of the RTL8211FS(I)(-VS) LEDs is shown in Table 16.

Table 16. LED Default Definitions

Operation Mode CFG_MODE[2:0]	Description		
	LED0	LED1	LED2
3'b000: UTP ←→ RGMII 3'b011: UTP ←→ SGMII 3'b100: SGMII (PHY side) ←→ RGMII (MAC side) 3'b101: SGMII (MAC side) ←→ RGMII (PHY side)	10M Link and Active (Transmitting or Receiving)	100M Link and Active (Transmitting or Receiving)	1000M Link and Active (Transmitting or Receiving)
3'b001: Fiber ←→ RGMII	N/A	100M Link and Active (Transmitting or Receiving)	1000M Link and Active (Transmitting or Receiving)
3'b010: UTP/Fiber ←→ RGMII (Media Auto Detection)	UTP 10M/100M/1000M Link up	Fiber 100M/1000M Link up	UTP or Fiber Link and Active (Transmitting or Receiving)
3'b110/3'b111: UTP ←→ Fiber (Media Conversion)	Link and Active (Transmitting or Receiving)	UTP and Fiber are both 100M Link up	UTP and Fiber are both 1000M Link up

The LED pins can be customized from Page 0xd04 Register 16 and 18. To change the LED settings, see note (below) and Table 17 LED Register Table, which summarizes several configuration types (see also Table 18 LED Configuration Table 1, and Table 19 LED Configuration Table 2, page 34).

Note: To switch to Page 0xd04, set Register 31 Data=0x0d04 (set page). After LED setting, switch back to the PHY's IEEE Standard Registers, i.e. Page 0 or Page 0xa42 (Register 31 Data = 0 or 0xa42).

Table 17. LED Register Table

Pin	LINK Speed			Active (Tx/Rx)	Common Mode	Media Select
	10Mbps	100Mbps	1000Mbps			
LED0	Reg16 Bit0	Reg16 Bit1	Reg16 Bit3	Reg16 Bit4	Reg18 Bit11	Reg18 Bit10
LED1	Reg16 Bit5	Reg16 Bit6	Reg16 Bit8	Reg16 Bit9	Reg18 Bit13	Reg18 Bit12
LED2	Reg16 Bit10	Reg16 Bit11	Reg16 Bit13	Reg16 Bit14	Reg18 Bit15	Reg18 Bit14

Table 18. LED Configuration Table 1

Pin	LINK Bit			Active (TX/RX) Bit	Description
	10Mbps	100Mbps	1000Mbps		
LED0 LED1 LED2	0	0	0	0	N/A
	0	0	0	1	N/A
	0	0	1	0	Link 1000
	0	0	1	1	Link 1000+Active
	0	1	0	0	Link 100
	0	1	0	1	Link 100+Active
	0	1	1	0	Link 100/1000
	0	1	1	1	Link 100/1000+Active
	1	0	0	0	Link 10
	1	0	0	1	Link 10+Active
	1	0	1	0	Link 10/1000
	1	0	1	1	Link 10/1000+Active
	1	1	0	0	Link 10/100
	1	1	0	1	Link 10/100+Active
	1	1	1	0	Link 10/100/1000
	1	1	1	1	Link 10/100/1000+Active

Table 19. LED Configuration Table 2

Pin	Common Mode	Media Select	Description
LED0 LED1 LED2	0	0	Media Select bit is valid when Common Mode = 1'b0. The corresponding LED indicates the UTP link status according to LED Configuration Table 1.
	0	1	Media Select bit is valid when Common Mode = 1'b0. The corresponding LED indicates the SERDES link status according to LED Configuration Table 1.
	1	X (Don’t care)	Media Select bit is not valid when Common Mode = 1'b1. The corresponding LED indicates the UTP and SERDES link status according to LED Configuration Table 1. The behavior must be the same on both sides and then the LED would be active. For example, the LED2 turns on only if the UTP and Fiber are both link up at 1000M in the Media Conversion mode.

7.16.2. EEE LED Function

EEE Idle Mode: LED continuous slow blinking.

EEE Active Mode: LED fast and slow blinking (on packet transmitting and receiving).

Refer to section 8.5.23, page 54 for EEE LED enable setting.

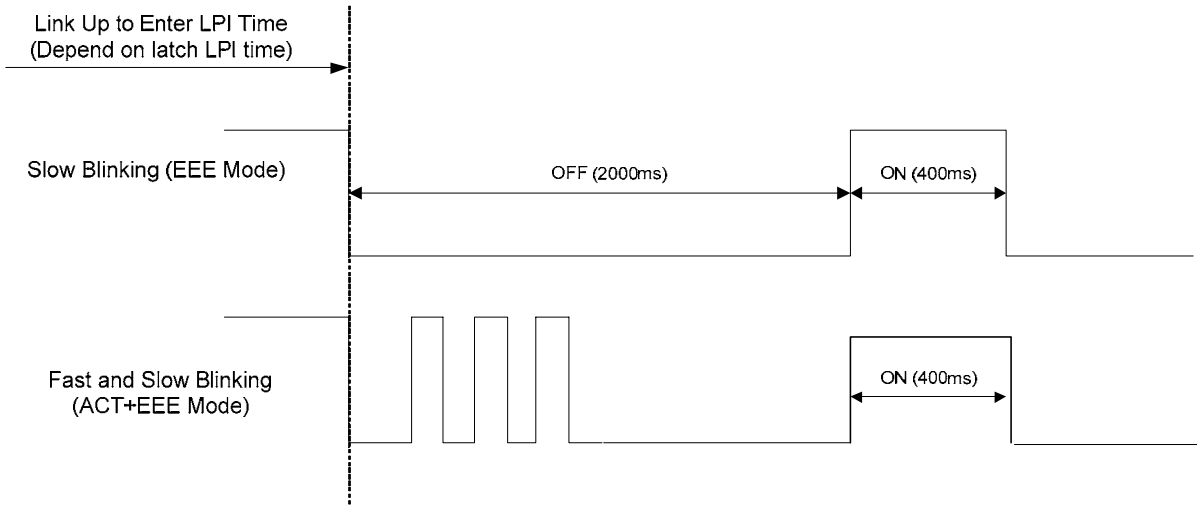


Figure 13. EEE LED Behavior

7.17. Polarity Correction

The RTL8211FS(I)(-VS) automatically corrects polarity errors on the receive pairs in 1000Base-T and 10Base-T modes. In 100Base-TX mode polarity is irrelevant. In 1000Base-T mode, receive polarity errors are automatically corrected based on the sequence of idle symbols. Once the descrambler is locked, the polarity is also locked on all pairs. The polarity becomes unlocked only when the receiver loses lock.

In 10Base-T mode, polarity errors are corrected based on the detection of validly spaced link pulses. The detection begins during the MDI crossover detection phase and locks when the 10Base-T link is up. The polarity becomes unlocked when the link is down.

7.18. Power

The RTL8211FS(I)(-VS) implements a voltage regulator to generate operating power. The system vendor needs to supply a 3.3V, 1A steady power source. The RTL8211FS(I)(-VS) converts the 3.3V steady power source to 1.0V via a switching regulator.

The RTL8211FS(I)(-VS) implements an option for the RGMII I/O power. The standard I/O voltage of the RGMII interface is 3.3V, with support for 2.5/1.8/1.5V to lower EMI. The 2.5/1.8/1.5V power source for RGMII is supplied from the internal LDO.

7.19. PHY Reset (Hardware Reset)

The RTL8211FS(I)(-VS) has a PHYRSTB pin to reset the chip. For a complete PHY reset, this pin must be asserted low for at least 10ms (Tgap in Figure 14) for the internal regulator. Wait for at least 50ms* (for internal circuits settling time) before accessing the PHY register. All registers will return to default values after a hardware reset.

** Note: Refer to Note 5 in section 9.1, page 75, and the RTL8211F_Series_Power_Sequence_App_Note for more detailed information.*

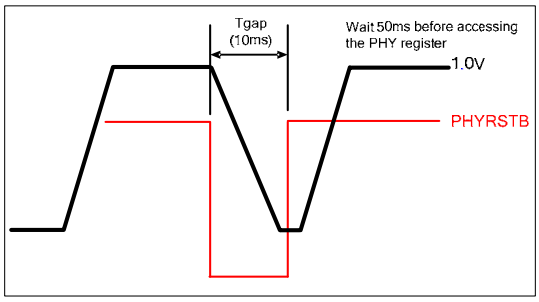


Figure 14. PHY Reset Timing

8. Register Descriptions

Table 20. Register Access Types

Type	Description
LH	Latch high. If the status is high, this field is set to ‘1’ and remains set.
RC	Read-cleared. The register field is cleared after read.
RO	Read only.
WO	Write only.
RW	Read and Write
SC	Self-cleared. Writing a ‘1’ to this register field causes the function to be activated immediately, and then the field will be automatically cleared to’0’ .

8.1. UTP Register Mapping and Definitions

Table 21. UTP Register Mapping and Definitions

Page	Offset	Access	Name	Description
0	0	RW	BMCR	Basic Mode Control Register.
0	1	RO	BMSR	Basic Mode Status Register.
0	2	RO	PHYID1	PHY Identifier Register 1.
0	3	RO	PHYID2	PHY Identifier Register 2.
0	4	RW	ANAR	Auto-Negotiation Advertising Register.
0	5	RO	ANLPAR	Auto-Negotiation Link Partner Ability Register.
0	6	RO	ANER	Auto-Negotiation Expansion Register.
0	7	RW	ANNPTR	Auto-Negotiation Next Page Transmit Register.
0	8	RO	ANNPRR	Auto-Negotiation Next Page Receive Register.
0	9	RW	GBCR	1000Base-T Control Register.
0	10	RO	GBSR	1000Base-T Status Register.
0	11~12	RO	RSVD	Reserved.
0	13	WO	MACR	MMD Access Control Register.
0	14	RW	MAADR	MMD Access Address Data Register.
0	15	RO	GBESR	1000Base-T Extended Status Register.
0xa42	16~17	RO	RSVD	Reserved.
0xa42	18	RW	INER	Interrupt Enable Register.
0xa42	19~23	RO	RSVD	Reserved.
0xa43	24	RW	PHYCR1	PHY Specific Control Register 1.
0xa43	25	RW	PHYCR2	PHY Specific Control Register 2.
0xa43	26	RO	PHYSR	PHY Specific Status Register.
0xa43	27~28	RO	RSVD	Reserved.
0xa43	29	RO	INSR	Interrupt Status Register.
0xa43	30	RO	RSVD	Reserved.
0xa43	31	RW	PAGSR	Page Select Register.
0xa46	20	RW	PHYSCR	PHY Special Config Register
0xd04	16	RW	LCR	LED Control Register.

Page	Offset	Access	Name	Description
0xd04	17	RW	EEELCR	EEE LED Control Register.
0xd04	18	RW	FLCR	Fiber LED Control Register
0xd08	21	RW	MIICR	MII Control Register
0xd40	22	RW	INTBCR	INTB Pin Control Register.
0xe40~ 0xe44	16~23	RW	-	PTP-related registers (RTL8211FS(I)-VS only).

Note 1: These UTP IEEE Standard Registers 0 to 15 are valid if MDI is selected as UTP mode.
Note 2: To access the IEEE Standard Registers 0 to 15, the Page Select Register (PAGSR, Register 31) should be set as '0' or '0xa42'(default value).
Note 3: For example, to switch to Page 0xd04, set Register 31 Data=0x0d04 (change to Page 0xd04). After LED setting, switch back to the PHY's IEEE Standard Registers, i.e. Page 0 or Page 0xa42 (Register 31 Data = 0 or 0xa42).

8.2. UTP MMD Register Mapping and Definition

Table 22. MMD Register Mapping and Definition

Device	Offset	Access	Name	Description
3	0	RW	PC1R	PCS Control 1 Register.
3	1	RW	PS1R	PCS Status 1 Register.
3	20	RO	EEECR	EEE Capability Register.
3	22	RC	EEEWER	EEE Wake Error Register.
7	60	RW	EEEAR	EEE Advertisement Register.
7	61	RO	EEELPAR	EEE Link Partner Ability Register.

8.3. Fiber Register Mapping and Definitions

Table 23. Fiber Registers Mapping and Definitions

Offset	Access	Name	Description
0	RW	Fiber BMCR	Fiber Basic Mode Control Register.
1	RO	Fiber BMSR	Fiber Basic Mode Status Register.
2	RO	PHYID1	PHY Identifier Register 1.
3	RO	PHYID2	PHY Identifier Register 2.
4	RW	1000Base-X ANAR	1000Base-X Auto-Negotiation Advertising Register.
5	RO	1000Base-X ANLPAR	1000Base-X Auto-Negotiation Link Partner Ability Register.
6~14	RO	RSVD	Reserved.
15	RO	Fiber ESR	Extended Status Register.

Note: These Fiber IEEE Standard Registers are valid if MDI is selected as Fiber mode.

8.4. SERDES Registers Mapping and Definitions

Table 24. SERDES Registers Mapping and Definitions

Page	Offset	Access	Name	Description
0xde1	17	RW	SERDES INER	SERDES Interrupt Enable Register.
0xde1	18	RO	SERDES INSR	SERDES Interrupt Status Register.
0xd08	20	RW	SGMII ANARSEL	SGMII Auto-Negotiation Advertising Register Select.
0xd08	16	RW	SGMII ANAR	SGMII Auto-Negotiation Advertising Register.
0xdc0	21	RO	SGMII ANLPAR	SGMII Auto-Negotiation Link Partner Ability Register.

Note: These registers are valid if the SGMII MAC mode is selected.

8.5. Register Tables

8.5.1. BMCR (Basic Mode Control Register, Address 0x00)

Table 25. BMCR (Basic Mode Control Register, Address 0x00)

Bit	Name	Type	Default	Description
0.15	Reset	RW, SC	0	Reset. 1: PHY reset 0: Normal operation Register 0 (BMCR) and register 1 (BMSR) will return to default values after a software reset (set Bit 0.15 to 1). This action may change the internal PHY state and the state of the physical link associated with the PHY.
0.14	Loopback	RW	0	Loopback Mode. 1: Enable PCS loopback mode 0: Disable PCS loopback mode
0.13	Speed[0]	RW	0	Speed Select Bit 0. In forced mode, i.e., when Auto-Negotiation is disabled, bits 0.6 and 0.13 determine device speed selection.
0.12	ANE	RW	1	Auto-Negotiation Enable. 1: Enable Auto-Negotiation 0: Disable Auto-Negotiation
0.11	PWD	RW	0	Power Down. 1: Power down (only Management Interface and logic are active; link is down) 0: Normal operation
0.10	Isolate	RW	0	Isolate. 1: RGMII interface is isolated; the serial management interface (MDC, MDIO) is still active. When this bit is asserted, the RTL8211FS(I)(-VS) ignores TXD[3:0], and TXCTL inputs, and presents a high impedance on TXC, RXC, RXCTL, RXD[3:0]. 0: Normal operation
0.9	Restart_AN	RW, SC	0	Restart Auto-Negotiation. 1: Restart Auto-Negotiation 0: Normal operation
0.8	Duplex	RW	0	Duplex Mode. 1: Full Duplex operation 0: Half Duplex operation This bit is valid only in force mode, i.e., NWay is disabled.

Speed[1]	Speed[0]	Speed Enabled
1	1	Reserved
1	0	1000Mbps
0	1	100Mbps
0	0	10Mbps

Bit	Name	Type	Default	Description
0.7	Collision Test	RW	0	Collision Test. 1: Collision test enabled 0: Normal operation
0.6	Speed[1]	RW	1	Speed Select Bit 1. Refer to bit 0.13.
0.5	Uni-directional enable	RW	0	Uni-Directional Enable 1: Enable packet transmit without respect to linkok status 0: Packet transmit permitted when link is established
0.4:0	RSVD	RO	00000	Reserved.

Note 1: Changes to Registers 0.12, 0.13, 0.6, and 0.8 do not take effect unless at least one of the following events occurs: Software reset (0.15) is asserted, Restart_AN (0.9) is asserted, or PWD(0.11) transitions from power-down to normal operation.

Note 2: When the RTL8211FS(I)(-VS) is switched from power down to normal operation, a software reset and restart auto-negotiation is performed, even if bits Reset (0.15) and Restart_AN (0.9) are not set by the user.

Note 3: Auto-Negotiation is enabled when speed is set to 1000Base-T. Crossover Detection & Auto-Correction takes precedence over Auto-Negotiation disable (0.12=0). If ANE is disabled, speed and duplex capabilities are advertised by 0.13, 0.6, and 0.8. Otherwise, register 4.8:5 and 9.9:8 take effect.

Note 4: Auto-Negotiation automatically restarts after hardware or software reset regardless of whether or not the restart bit (0.9) is set.

8.5.2. BMSR (Basic Mode Status Register, Address 0x01)

Table 26. BMSR (Basic Mode Status Register, Address 0x01)

Bit	Name	Type	Default	Description
1.15	100Base-T4	RO	0	100Base-T4 Capability. The RTL8211FS(I)(-VS) does not support 100Base-T4 mode. This bit should always be 0.
1.14	100Base-TX (full)	RO	1	100Base-TX Full Duplex Capability. 1: Device is able to perform 100Base-TX in full duplex mode 0: Device is not able to perform 100Base-TX in full duplex mode
1.13	100Base-TX (half)	RO	1	100Base-TX Half Duplex Capability. 1: Device is able to perform 100Base-TX in half duplex mode 0: Device is not able to perform 100Base-TX in half duplex mode
1.12	10Base-T (full)	RO	1	10Base-T Full Duplex Capability. 1: Device is able to perform 10Base-T in full duplex mode. 0: Device is not able to perform 10Base-T in full duplex mode.
1.11	10Base-T (half)	RO	1	10Base-T Half Duplex Capability. 1: Device is able to perform 10Base-T in half duplex mode 0: Device is not able to perform 10Base-T in half duplex mode
1.10	10Base-T2 (full)	RO	0	10Base-T2 Full Duplex Capability. The RTL8211FS(I)(-VS) does not support 10Base-T2 mode and this bit should always be 0.
1.9	10Base-T2 (half)	RO	0	10Base-T2 Half Duplex Capability. The RTL8211FS(I)(-VS) does not support 10Base-T2 mode. This bit should always be 0.

Bit	Name	Type	Default	Description
1.8	1000Base-T Extended Status	RO	1	1000Base-T Extended Status Register. 1: Device supports Extended Status Register 0x0F (15) 0: Device does not support Extended Status Register 0x0F This register is read-only and is always set to 1.
1.7	Uni-directional ability	RO	1	Uni-Directional Ability. 1: PHY able to transmit without linkok 0: PHY not able to transmit without linkok
1.6	Preamble Suppression	RO	0	Preamble Suppression Capability. The RTL8211FS(I)(-VS) default would not accept MDC/MDIO transactions with preamble suppressed.
1.5	Auto-Negotiation Complete	RO	0	Auto-Negotiation Complete. 1: Auto-Negotiation process complete, and contents of Registers 5, 6, 8, and 10 are valid 0: Auto-Negotiation process not complete
1.4	Remote Fault	RC, LH	0	Remote Fault. 1: Remote fault condition detected (cleared on read or by reset). Indication or notification of remote fault from Link Partner 0: No remote fault condition detected
1.3	Auto-Negotiation Ability	RO	1	Auto Configured Link. 1: Device is able to perform Auto-Negotiation 0: Device is not able to perform Auto-Negotiation
1.2	Link Status	RO	0	Link Status. 1: Linked 0: Not Linked This register indicates whether the link was lost since the last read. For the current link status, either read this register twice or read Page 0xa43 Reg 26, bit[2] Link (Real Time).
1.1	Jabber Detect	RC, LH	0	Jabber Detect. 1: Jabber condition detected 0: No Jabber occurred
1.0	Extended Capability	RO	1	1: Extended register capabilities, always 1

8.5.3. PHYID1 (PHY Identifier Register 1, Address 0x02)

Table 27. PHYID1 (PHY Identifier Register 1, Address 0x02)

Bit	Name	Type	Default	Description
2.15:0	OUI_MSB	RO	0000000000011100	Organizationally Unique Identifier Bit 3:18. Always 0000000000011100.

Note: Realtek OUI is 0x000732.

8.5.4. PHYID2 (PHY Identifier Register 2, Address 0x03)

Table 28. PHYID2 (PHY Identifier Register 2, Address 0x03)

Bit	Name	Type	Default	Description
3.15:10	OUI_LSB	RO	110010	Organizationally Unique Identifier Bit 19:24. Always 110010.
3.9:4	Model Number	RO	010001	Manufacture's Model Number
3.3:0	Revision Number	RO	0110	Revision Number

8.5.5. ANAR (Auto-Negotiation Advertising Register, Address 0x04)

Table 29. ANAR (Auto-Negotiation Advertising Register, Address 0x04)

Bit	Name	Type	Default	Description
4.15	NextPage	RW	0	1: Additional next pages exchange desired 0: No additional next pages exchange desired
4.14	RSVD	RO	0	Reserved.
4.13	Remote Fault	RW	0	1: Set Remote Fault bit 0: No remote fault detected
4.12	RSVD	RO	0	Reserved.
4.11	Asymmetric PAUSE	RW	0	1: Advertise support of asymmetric pause 0: No support of asymmetric pause
4.10	PAUSE	RW	0	1: Advertise support of pause frames 0: No support of pause frames
4.9	100Base-T4	RO	0	1: 100Base-T4 support 0: 100Base-T4 not supported
4.8	100Base-TX (Full)	RW	1	1: Advertise support of 100Base-TX full-duplex mode 0: Not advertised
4.7	100Base-TX (Half)	RW	1	1: Advertise support of 100Base-TX half-duplex mode 0: Not advertised
4.6	10Base-T (Full)	RW	1	1: Advertise support of 10Base-TX full-duplex mode 0: Not advertised
4.5	10Base-T (Half)	RW	1	1: Advertise support of 10Base-TX half-duplex mode 0: Not advertised
4.4:0	Selector Field	RO	00001	Indicates the RTL8211FS(I)(-VS) supports IEEE 802.3

Note 1: The setting of Register 4 has no effect unless NWay is restarted or the link goes down, i.e., software reset (0.15) is asserted, Restart_AN (0.9) is asserted, or PWD (0.11) transitions from power down to normal operation.

Note 2: If 1000Base-T is advertised, then the required next pages are automatically transmitted. Register 4.15 should be set to 0 if no additional next pages are needed.

8.5.6. ANLPAR (Auto-Negotiation Link Partner Ability Register, Address 0x05)

Table 30. ANLPAR (Auto-Negotiation Link Partner Ability Register, Address 0x05)

Bit	Name	Type	Default	Description
5.15	Next Page	RO	0	Next Page Indication. Received Code Word Bit 15.
5.14	ACK	RO	0	Acknowledge. Received Code Word Bit 14.
5.13	Remote Fault	RO	0	Remote Fault indicated by Link Partner. Received Code Word Bit 13.
5.12	RSVD	RO	0	Reserved.
5.11:5	Technology Ability Field	RO	00000000	Received Code Word Bit 12:5.
5.4:0	Selector Field	RO	00000	Received Code Word Bit 4:0.

Note: Register 5 is not valid until the Auto-Negotiation complete bit 1.5 indicates completed.

8.5.7. ANER (Auto-Negotiation Expansion Register, Address 0x06)

Table 31. ANER (Auto-Negotiation Expansion Register, Address 0x06)

Bit	Name	Type	Default	Description
6.15:7	RSVD	RO	0x000	Reserved.
6.6	RX NP location ability	RO	1	Received next page storage location ability. 1: Received next page storage location is specified by bit 6.5 0: Received next page storage location is not specified by bit 6.5
6.5	RX NP location	RO	1	Received next page storage location. 1: Link partner next pages are stored in Register 8 0: Link partner next pages are stored in Register 5
6.4	Parallel Detection Fault	RC, LH	0	1: A fault has been detected via the Parallel Detection function 0: A fault has not been detected via the Parallel Detection function
6.3	Link Partner Next Page Able	RO	0	1: Link Partner supports Next Page exchange 0: Link Partner does not support Next Page exchange
6.2	Local Next Page Able	RO	1	1: Local Device is able to send Next Page Always 1.
6.1	Page Received	RC, LH	0	1: A New Page (new LCW) has been received 0: A New Page has not been received
6.0	Link Partner Auto-Negotiation capable	RO	0	1: Link Partner supports Auto-Negotiation 0: Link Partner does not support Auto-Negotiation

Note: Register 6 is not valid until the Auto-Negotiation complete bit 1.5 indicates completed.

8.5.8. ANNPTR (Auto-Negotiation Next Page Transmit Register, Address 0x07)

Table 32. ANNPTR (Auto-Negotiation Next Page Transmit Register, Address 0x07)

Bit	Name	Type	Default	Description
7.15	Next Page	RW	0	Next Page Indication. 0: No more next pages to send 1: More next pages to send Transmit Code Word Bit 15.
7.14	RSVD	RO	0	Transmit Code Word Bit 14.
7.13	Message Page	RW	1	Message Page. 0: Unformatted Page 1: Message Page Transmit Code Word Bit 13.
7.12	Acknowledge 2	RW	0	Acknowledge2. 0: Local device has no ability to comply with the message received 1: Local device has the ability to comply with the message received Transmit Code Word Bit 12.
7.11	Toggle	RO	0	Toggle Bit. Transmit Code Word Bit 11.
7.10:0	Message/Unformatted Field	RW	0x001	Content of Message/Unformatted Page. Transmit Code Word Bit 10:0.

8.5.9. ANNPRR (Auto-Negotiation Next Page Receive Register, Address 0x08)

Table 33. ANNPRR (Auto-Negotiation Next Page Receive Register, Address 0x08)

Bit	Name	Type	Default	Description
8.15	Next Page	RO	0	Received Link Code Word Bit 15.
8.14	Acknowledge	RO	0	Received Link Code Word Bit 14.
8.13	Message Page	RO	0	Received Link Code Word Bit 13.
8.12	Acknowledge 2	RO	0	Received Link Code Word Bit 12.
8.11	Toggle	RO	0	Received Link Code Word Bit 11.
8.10:0	Message/Unformatted Field	RO	0x00	Received Link Code Word Bit 10:0.

Note: Register 8 is not valid until the Auto-Negotiation complete bit 1.5 indicates completed.

8.5.10. GBCR (1000Base-T Control Register, Address 0x09)

Table 34. GBCR (1000Base-T Control Register, Address 0x09)

Bit	Name	Type	Default	Description
9.15:13	Test Mode	RW	0	Test Mode Select. 000: Normal Mode 001: Test Mode 1 – Transmit Jitter Test 010: Test Mode 2 – Transmit Jitter Test (MASTER mode) 011: Test Mode 3 – Transmit Jitter Test (SLAVE mode) 100: Test Mode 4 – Transmit Distortion Test 101, 110, 111: Reserved
9.12	MASTER/SLAVE Manual Configuration Enable	RW	0	Enable Manual Master/Slave Configuration. 1: Manual MASTER/SLAVE configuration 0: Automatic MASTER/SLAVE
9.11	MASTER/SLAVE Configuration Value	RW	0	Advertise Master/Slave Configuration Value. 1: Manual configure as MASTER 0: Manual configure as SLAVE
9.10	Port Type	RW	0	Advertise Device Type Preference. 1: Prefer multi-port device (MASTER) 0: Prefer single port device (SLAVE)
9.9	1000Base-T Full Duplex	RW	1	Advertise 1000Base-T Full-Duplex Capability. 1: Advertise 0: Do not advertise
9.8	RSVD	RW	0	Reserved.
9.7:0	RSVD	RO	0	Reserved.

Note 1: Values set in register 9.12:9 have no effect unless Auto-Negotiation is restarted (Reg 0.9) or the link goes down.
Note 2: Bits 9.11 and 9.10 are ignored when bit 9.12=0.

8.5.11. GBSR (1000Base-T Status Register, Address 0x0A)

Table 35. GBSR (1000Base-T Status Register, Address 0x0A)

Bit	Name	Type	Default	Description
10.15	MASTER/SLAVE Configuration Fault	RO, RC, LH	0	Master/Slave Manual Configuration Fault Detected. 1: MASTER/SLAVE configuration fault detected 0: No MASTER/SLAVE configuration fault detected
10.14	MASTER/SLAVE Configuration Resolution	RO	0	Master/Slave Configuration Result. 1: Local PHY configuration resolved to MASTER 0: Local PHY configuration resolved to SLAVE
10.13	Local Receiver Status	RO	0	Local Receiver Status. 1: Local Receiver OK 0: Local Receiver Not OK
10.12	Remote Receiver Status	RO	0	Remote Receiver Status. 1: Remote Receiver OK 0: Remote Receiver Not OK

Bit	Name	Type	Default	Description
10.11	Link Partner 1000Base-T Full Duplex Capability	RO	0	Link Partner 1000Base-T Full Duplex Capability. 1: Link Partner is capable of 1000Base-T full duplex 0: Link Partner is not capable of 1000Base-T full duplex
10.10	Link Partner 1000Base-T Half Duplex Capability	RO	0	Link Partner 1000Base-T Half Duplex Capability. 1: Link Partner is capable of 1000Base-T half duplex 0: Link Partner is not capable of 1000Base-T half duplex
10.9:8	RSVD	RO	00	Reserved.
10.7:0	Idle Error Count	RO, RC	0x00	MSB of Idle Error Counter. The counter stops automatically when it reaches 0xff.

Note 1: Values set in register 10.11:10 are not valid until register 6.1 is set to 1.

Note 2: Register 10 is not valid until the Auto-Negotiation complete bit 1.5 indicates completed.

8.5.12. MACR (MMD Access Control Register, Address 0x0D)

Table 36. MACR (MMD Access Control Register, Address 0x0D)

Bit	Name	Type	Default	Description
13.15:14	Function	WO	0	00: Address 01: Data with no post increment 10: Data with post increment on reads and writes 11: Data with post increment on writes only
13.13:5	RSVD	RO	000000000	Reserved.
13.4:0	DEVAD	WO	0	Device Address.

Note 1: This register is used in conjunction with the MAADR (Register 14) to provide access to the MMD address space.

Note 2: If the MAADR accesses for address (Function=00), then it is directed to the address register within the MMD associated with the value in the DEVAD field.

Note 3: If the MAADR accesses for data (Function≠00), both the DEVAD field and MMD's address register direct the MAADR data accesses to the appropriate registers within the MMD.

8.5.13. MAADR (MMD Access Address Data Register, Address 0x0E)

Table 37. MAADR (MMD Access Address Data Register, Address 0x0E)

Bit	Name	Type	Default	Description
14.15:0	Address Data	RW	0x0000	13.15:14 = 00 → MMD DEVAD's address register 13.15:14 = 01, 10, or 11 → MMD DEVAD's data register as indicated by the contents of its address register

Note: This register is used in conjunction with the MACR (Register 13; Table 36) to provide access to the MMD address space.

8.5.14. GBESR (1000Base-T Extended Status Register, Address 0x0F)

Table 38. GBESR (1000Base-T Extended Status Register, Address 0x0F)

Bit	Name	Type	Default	Description
15.15	1000Base-X FD	RO	0	0: Not 1000Base-X full duplex capable
15.14	1000Base-X HD	RO	0	0: Not 1000Base-X half duplex capable
15.13	1000Base-T FD	RO	1	1: 1000Base-T full duplex capable
15.12	1000Base-T HD	RO	0	1: 1000Base-T half duplex capable
15.11:0	RSVD	RO	0x000	Reserved.

8.5.15. INER (Interrupt Enable Register, Page 0xa42, Address 0x12)

Table 39. INER (Interrupt Enable Register, Page 0xa42, Address 0x12)

Bit	Name	Type	Default	Description
18.15:11	RSVD	RW	00000	Reserved.
18.10	Jabber Interrupt	RW	0	1: Interrupt Enable 0: Interrupt Disable Setting this bit to 0 only disables the jabber interrupt event in the INTB pin. Page 0xa43, Reg29 Bit[10] always reflects the jabber interrupt behavior.
18.9	ALDPS State Change Interrupt	RW	0	1: Interrupt Enable 0: Interrupt Disable Setting this bit to 0 only disables the ALDPS state change interrupt event in the INTB pin. Page 0xa43, Reg29 Bit[9] always reflects the ALDPS state change interrupt behavior.
18.8	RSVD	RW	0	Reserved.
18.7	PME (Power Management Event of WOL)	RW	0	1: Interrupt Enable 0: Interrupt Disable Setting this bit to 0 only disables the PME interrupt event in the INTB pin. Page 0xa43, Reg29 Bit[7] always reflects the PME interrupt behavior.
18.6	RSVD	RW	0	Reserved.
18.5	PHY Register Accessible Interrupt	RW	1	1: Interrupt Enable 0: Interrupt Disable Setting this bit to 0 only disables the PHY register access interrupt event in the INTB pin. Page 0xa43, Reg29 Bit[5] always reflects the PHY register access interrupt behavior.
18.4	Link Status Change Interrupt	RW	0	1: Interrupt Enable 0: Interrupt Disable Setting this bit to 0 only disables the link status change interrupt event in the INTB pin. Page 0xa43, Reg29 Bit[4] always reflects the link change interrupt behavior.
18.3	Auto-Negotiation Completed Interrupt	RW	0	1: Interrupt Enable 0: Interrupt Disable Setting this bit to 0 only disables the auto-negotiation completed interrupt event in the INTB pin. Page 0xa43, Reg29 Bit[3] always reflects the auto-negotiation completed interrupt behavior.
18.2	Page Received Interrupt	RW	0	1: Interrupt Enable 0: Interrupt Disable Setting this bit to 0 only disables the page received interrupt event in the INTB pin. Page 0xa43, Reg29 Bit[2] always reflects the page received interrupt behavior.
18.1	RSVD	RW	0	Reserved.

Bit	Name	Type	Default	Description
18.0	Auto-Negotiation Error Interrupt	RW	0	1: Interrupt Enable 0: Interrupt Disable Setting this bit to 0 only disables the auto-negotiation error interrupt event in the INTB pin. Page 0xa43, Reg29 Bit[0] always reflects the auto-negotiation error interrupt behavior.

8.5.16. PHYCR1 (PHY Specific Control Register 1, Page 0xa43, Address 0x18)

Table 40. PHYCR1 (PHY Specific Control Register 1, Page 0xa43, Address 0x18)

Bit	Name	Type	Default	Description
24.15:14	RSVD	RO	00	Reserved.
24.13	PHYAD_0 Enable	RW	1	1: A broadcast from MAC (A command with PHY address = 0) is valid. MDC/MDIO will respond to this command.
24.12	ALDPS XTAL-OFF Enable	RW	0	1: Enable XTAL off when in ALDPS mode (valid when Bit 24.2 = 1)
24.11:10	RSVD	RO	00	Reserved.
24.9	MDI Mode Manual Configuration Enable	RW	0	1: Enable Manual Configuration of MDI mode
24.8	MDI Mode	RW	1	Set the MDI/MDIX mode. 1: MDI 0: MDIX This bit will take effect only when Bit 24.9 = 1.
24.7	TX CRS Enable	RW	0	1: Assert CRS on transmit 0: Never assert CRS on transmit
24.6	PHYAD Non-zero Detect	RW	0	1: The RTL8211FS(I)(-VS) with PHYAD[2:0] = 000 will latch the first non-zero PHY address as its own PHY address
24.5	RSVD	RO	0	Reserved.
24.4	Preamble Check Enable	RW	1	1: Check preamble when receiving an MDC/MDIO command
24.3	Jabber Detection Enable	RW	1	1: Enable Jabber Detection
24.2	ALDPS Enable	RO	0	1: Enable Link Down Power Saving Mode
24.1	ALDPS PLL-OFF Enable	RW	0	1: Enable PLL off when in ALDPS mode (valid when Bit 24.2= 1)
24.0	RSVD	RO	0	Reserved.

Note: The method to disable auto-crossover and force MDI or MDIX mode is as follows:

Step 1: Set Bit 24.9=1 (Manual Configuration of MDI mode) and set Bit24.8=1 (MDI) or 0 (MDIX).

Step 2: Perform a PHY reset, i.e., set Page 0, Reg0 bit[15]=1.

8.5.17. PHYCR2 (PHY Specific Control Register 2, Page 0xa43, Address 0x19)

Table 41. PHYCR2 (PHY Specific Control Register 2, Page 0xa43, Address 0x19)

Bit	Name	Type	Default	Description
25.15:14	RSVD	RO	00	Reserved.
25.13:12	CLKOUT Source	RW	00	Source select of the CLKOUT pin clock output. 00: Free run clock generated from internal PLL. 01: UTP recovery receive clock for Sync Ethernet. (Valid only if in UTP mode) 10: Fiber recovery receive clock for Sync Ethernet. (Valid only if in FIBER mode) 11: PTP synchronized clock output. *Note: Issue a Software Reset (0.15) in order to allow the setting to take effect.*
25.11	CLKOUT Frequency Select	RW	1	Frequency select of the CLKOUT pin clock output. 0: 25MHz 1: 125MHz
25.10:8	RSVD	RO	000	Reserved.
25.7	CLKOUT SSC Enable	RW	0	1: Enable Spread-Spectrum Clocking (SSC) on CLKOUT output clock.
25.6	RSVD	RO	1	Reserved.
25.5	PHY-mode EEE Enable	RW	1	1: Enable EEE in PHY mode.
25.4	RSVD	RO	0	Reserved.
25.3	RXC SSC Enable	RW	0	1: Enable Spread-Spectrum Clocking (SSC) on RXC clock output.
25.2	RSVD	RO	0	Reserved.
25.1	RXC Enable	RW	1	1: RXC clock output enabled.
25.0	CLKOUT Enable	RW	1	1: CLKOUT clock output enabled.

8.5.18. PHYSR (PHY Specific Status Register, Page 0xa43, Address 0x1A)

Table 42. PHYSR (PHY Specific Status Register, Page 0xa43, Address 0x1A)

Bit	Name	Type	Default	Description
26.15	RSVD	RO	0	Reserved.
26.14	ALDPS State	RO	0	Link Down Power Saving Mode. 1: Reflects local device entered Link Down Power Saving Mode, i.e., cable not plugged in (reflected after 3 sec). 0: With cable plugged in
26.13	MDI Plug	RO	0	MDI Status. 1: Plugged 0: Unplugged
26.12	NWay Enable	RO	1	Auto-Negotiation (NWay) Status. 1: Enable 0: Disable
26.11	Master Mode	RO	0	Device is in Master/Slave Mode. 1: Master mode 0: Slave mode
26.10:9	RSVD	RO	00	Reserved.

Bit	Name	Type	Default	Description
26.8	EEE capability	RO	0	1: Both local and link-partner have EEE capability of current speed
26.7	Rxflow Enable	RO	0	Rx Flow Control. 1: Enable 0: Disable
26.6	Txflow Enable	RO	0	Tx Flow Control. 1: Enable 0: Disable
26.5:4	Speed	RO	00	Link Speed. 11: Reserved 10: 1000Mbps 01: 100Mbps 00: 10Mbps
26.3	Duplex	RO	0	Full/Half Duplex Mode. 1: Full duplex 0: Half duplex
26.2	Link (Real Time)	RO	0	Real Time Link Status. 1: Link OK 0: Link not OK
26.1	MDI Crossover Status	RO	1	MDI/MDI Crossover Status. 1: MDI 0: MDI Crossover
26.0	Jabber (Real Time)	RO	0	Real Time Jabber Indication. 1: Jabber Indication 0: No Jabber Indication

Note 1: Bit 26.11 is valid only when in Giga mode.

Note 2: Bit 26.8 asserts at 10M speed when local device is EEE capable.

8.5.19. INSR (Interrupt Status Register, Page 0xa43, Address 0x1D)

Table 43. INSR (Interrupt Status Register, Page 0xa43, Address 0x1D)

Bit	Name	Type	Default	Description
29.15:11	RSVD	RO, RC	00000	Reserved.
29.10	Jabber	RO, RC	0	1: Jabber detected 0: No jabber detected
29.9	ALDPS State Change	RO, RC	0	1: ALDPS state changed 0: ALDPS state not changed
29.8	RSVD	RO, RC	0	Reserved.
29.7	PME (Power Management Event of WOL)	RO, RC	0	1: WOL event occurred 0: WOL event did not occur
29.6	RSVD	RO, RC	0	Reserved.
29.5	PHY Register Accessible	RO, RC	0	1: Can access PHY Register through MDC/MDIO 0: Cannot access PHY Register through MDC/MDIO
29.4	Link Status Change	RO, RC	0	1: Link status changed 0: Link status not changed
29.3	Auto-Negotiation Completed	RO, RC	0	1: Auto-Negotiation completed 0: Auto-Negotiation not completed
29.2	Page Received	RO, RC	0	1: Page (a new LCW) received 0: Page not received
29.1	RSVD	RO, RC	0	Reserved.
29.0	Auto-Negotiation Error	RO, RC	0	1: Auto-Negotiation Error 0: No Auto-Negotiation Error

8.5.20. PAGSR (Page Select Register, Page 0xa43, Address 0x1F)

Table 44. PAGSR (Page Select Register, Page 0xa43, Address 0x1F)

Bit	Name	Type	Default	Description
31.15:12	RSVD	RW	0	Reserved.
31.11:0	PageSel	RW	0xa42	Page Select (in HEX). 0xa42: Page 0xa42 (default page)

8.5.21. PHYSCR (PHY Special Config Register, Page 0xa46, Address 0x14)

Table 45. PHYSCR (PHY Special Config Register, Page 0xa46, Address 0x14)

Bit	Name	Type	Default	Description
20.15:2	RSVD	RO	0	Reserved.
20.1	PHY Special Config Done	RW	0	1: Write 1 to indicate the special PHY parameter configuration has been done.
20.0	RSVD	RO	0	Reserved.

8.5.22. LCR (LED Control Register, Page 0xd04, Address 0x10)

Table 46. LCR (LED Control Register, Page 0xd04, Address 0x10)

Bit	Name	Type	Default	Description
16.15	RSVD	RO	0	Reserved.
16.14	LED2_ACT	RW	1	LED2 Active (Transmitting or Receiving) Indication
16.13	LED2_LINK_1000	RW	1	LED2 Link Indication: 1000Mbps
16.12	RSVD	RO	0	Reserved.
16.11	LED2_LINK_100	RW	0	LED2 Link Indication: 100Mbps
16.10	LED2_LINK_10	RW	0	LED2 Link Indication: 10Mbps
16.9	LED1_ACT	RW	1	LED1 Active (Transmitting or Receiving) Indication
16.8	LED1_LINK_1000	RW	0	LED1 Link Indication: 1000Mbps
16.7	RSVD	RO	0	Reserved.
16.6	LED1_LINK_100	RW	1	LED1 Link Indication: 100Mbps
16.5	LED1_LINK_10	RW	0	LED1 Link Indication: 10Mbps
16.4	LED0_ACT	RW	1	LED0 Active (Transmitting or Receiving) Indication
16.3	LED0_LINK_1000	RW	0	LED0 Link Indication: 1000Mbps
16.2	RSVD	RO	0	Reserved.
16.1	LED0_LINK_100	RW	0	LED0 Link Indication: 100Mbps
16.0	LED0_LINK_10	RW	1	LED0 Link Indication: 10Mbps

8.5.23. EEELCR (EEE LED Control Register, Page 0xd04, Address 0x11)

Table 47. EEELCR (EEE LED Control Register, Page 0xd04, Address 0x11)

Bit	Name	Type	Default	Description
17.15:4	RSVD	RO	0	Reserved.
17.3	LED2 EEE Enable	RW	1	1: Enable EEE LED indication of LED2.
17.2	LED1 EEE Enable	RW	1	1: Enable EEE LED indication of LED1.
17.1	LED0 EEE Enable	RW	1	1: Enable EEE LED indication of LED0.
17.0	RSVD	RO	0	Reserved.

8.5.24. FLCR (Fiber LED Control Register, Page 0xd04, Address 0x12)

Table 48. FLCR (Fiber LED Control Register, Page 0xd04, Address 0x12)

Bit	Name	Type	Default	Description
18.15	LED2 Common Mode	RW	0	1: Enable LED2 common mode.
18.14	LED2 Media Select	RW	0	Media selection of LED2. 0: UTP 1: SERDES Valid if LED2 Common Mode = 0
18.13	LED1 Common Mode	RW	0	1: Enable LED1 common mode.
18.12	LED1 Media Select	RW	0	Media selection of LED1. 0: UTP 1: SERDES Valid if LED1 Common Mode = 0
18.11	LED0 Common Mode	RW	0	1: Enable LED0 common mode.
18.10	LED0 Media Select	RW	0	Media selection of LED0. 0: UTP 1: SERDES Valid if LED0 Common Mode = 0
18.9:0	RSVD	RO	0	Reserved.

8.5.25. MIICR (MII Control Register, Page 0xd08, Address 0x15)

Table 49. MIICR (MII Control Register, Page 0xd08, Address 0x15)

Bit	Name	Type	Default	Description
21.15:7	RSVD	RO	0	Reserved.
21.6	RGMII In-band CRS Enable	RW	1	1: Enable in-band CRS Status in RGMII Rx flow.
21.5:0	RSVD	RO	0	Reserved.

8.5.26. INTBCR (INTB Pin Control Register, Page 0xd40, Address 0x16)

Table 50. INTBCR (INTB Pin Control Register, Page 0xd40, Address 0x16)

Bit	Name	Type	Default	Description
22.15:6	RSVD	RO	0	Reserved.
22.5	INTB/PMEB Selection	RW	0	Pin 34 of the RTL8211FS(I)(-VS) functions as: 1: PMEB 0: INTB
22.4:3	RSVD	RO	0	Reserved.
22.2:0	INTB/PTP_GPIO_1 Sel	RW	000	3'b101: Pin 34 of the RTL8211FS(I)(-VS) functions as PTP GPIO_1. Other values: Reserved. *Note: This configuration has higher priority than the INTB/PMEB function.*

8.5.27. PTP_CTL (PTP Control Register, Page 0xe40, Address 0x10)

**Note: This register applies to the RTL8211FS(I)-VS only.*

Table 51. PTP_CTL (PTP Control Register, Page 0xe40, Address 0x10)

Bit	Name	Type	Default	Description
16.15:13	RSVD	RO	000	Reserved.
16.12	UDP_CHKSUM Update	RW	0	Enable auto-correction of UDP Checksum if One-Step Timestamp Insertion is enabled. Only effective to IPv6/UDP packets. 0: Set 0x0000 to the UDP Checksum field 1: Re-compute the UDP Checksum
16.11	P_DRFU_2STEP_INS Enable	RW	0	Enable Hardware-assisted Timestamp Insertion to PDelaly_Resp_Follow_Up messages.
16.10	P_DR_2STEP_INS Enable	RW	0	Enable Hardware-assisted Timestamp Insertion to PDelay_Resp messages.
16.9	DR_2STEP_INS Enable	RW	0	Enable Hardware-assisted Timestamp Insertion to Delay_Resp messages.
16.8	FU_2STEP_INS Enable	RW	0	Enable Hardware-assisted Timestamp Insertion to Follow_Up messages.
16.7	P_DR_1STEP Enable	RW	0	Enable One-Step Timestamp Insertion (t3-t2) to Pdelay_Response messages.
16.6	SYNC_1STEP Enable	RW	0	Enable One-Step Timestamp Insertion (t1) to Sync messages.
16.5	AVB_802.1AS Support	RW	1	1: AVB 802.1AS standard support.
16.4	PTPv2_Layer2 Support	RW	1	1: PTPv2 Layer 2 packets support.
16.3	PTPv2_UDPIPV4 Support	RW	1	1: PTPv2 UDP/IPv4 packets support.
16.2	PTPv2_UDPIPV6 Support	RW	1	1: PTPv2 UDP/IPv6 packets support.
16.1	PTPv1 Support	RW	1	1: PTPv1 packets support.

Bit	Name	Type	Default	Description
16.0	PTP_Enable	RW	1	PTP function enable *Note: Issue a Software Reset (0.15) after setting this bit in order to enable/disable PTP function.*

8.5.28. PTP_INER (PTP Interrupt Enable Register, Page 0xe40, Address 0x11)

**Note: This register applies to the RTL8211FS(I)-VS only.*

Table 52. PTP_INER (PTP Interrupt Enable Register, Page 0xe40, Address 0x11)

Bit	Name	Type	Default	Description
17.15:4	RSVD	RO	0x000	Reserved.
17.3	Tx Timestamp Interrupt	RW	0	1: Interrupt Enable 0: Interrupt Disable Transmit Timestamp ready interrupt.
17.2	Rx Timestamp Interrupt	RW	0	1: Interrupt Enable 0: Interrupt Disable Receive Timestamp ready interrupt.
17.1	TrigGen Interrupt	RW	0	1: Interrupt Enable 0: Interrupt Disable Trigger Generate complete interrupt.
17.0	EventCap Interrupt	RW	0	1: Interrupt Enable 0: Interrupt Disable Event Capture timestamp ready interrupt.

8.5.29. PTP_INSR (PTP Interrupt Status Register, Page 0xe40, Address 0x12)

**Note: This register applies to the RTL8211FS(I)-VS only.*

Table 53. PTP_INSR (PTP Interrupt Status Register, Page 0xe40, Address 0x12)

Bit	Name	Type	Default	Description
18.15:4	RSVD	RO	0x000	Reserved.
18.3	Tx Timestamp Interrupt	RO, RC	0	1: Transmit Timestamp ready interrupt detected.
18.2	Rx Timestamp Interrupt	RO, RC	0	1: Receive Timestamp ready interrupt detected.
18.1	TrigGen Interrupt	RO, RC	0	1: Trigger Generate complete interrupt detected.
18.0	EventCap Interrupt	RO, RC	0	1: Event Capture timestamp ready interrupt detected.

8.5.30. SYNCE_CTL (Sync-E Control Register, Page 0xe40, Address 0x13)

**Note: This register applies to the RTL8211FS(I)-VS only.*

Table 54. SYNCE_CTL (Sync-E Control Register, Page 0xe40, Address 0x13)

Bit	Name	Type	Default	Description
19.15:1	RSVD	RO	0	Reserved.
19.0	SyncE Enable	RW	0	Sync-E function Enable. *Note: Issue a Software Reset (0.15) after setting this bit in order to enable/disable Sync-E function.*

8.5.31. PTP_CLK_CFG (PTP Clock Config Register, Page 0xe41, Address 0x10)

**Note: This register applies to the RTL8211FS(I)-VS only.*

Table 55. PTP_CLK_CFG (PTP Clock Config Register, Page 0xe41, Address 0x10)

Bit	Name	Type	Default	Description
16.15:7	RSVD	RO	0	Reserved.
16.6:5	ptp_clkin_freq_sel	RW	0	PTP CLKIN Frequency Select. 00: 125MHz 01: 25MHz 10: 10MHz 11: Reserved *Note: Issue a Software Reset (0.15) in order to allow the setting to take effect.*
16.4	ptp_clkin_en	RW	0	PTP CLKIN function at GPIO 0 enable *Note: Issue a Software Reset (0.15) in order to allow the setting to take effect.*
16.3:1	ptp_clkadj_mod	RW	0	PTP Clock Adjustment Mode Select. 000: No function 001: Reserved - Issue Direct Read/Write to PTP_Local_Time through PTP_Time_Config registers 010: Direct Read 011: Direct Write - Issue Step Adjustment to PTP_Local_Time through PTP_Time_Config registers 100: Increment Step 101: Decrement Step - Issue Rate Adjustment Read/Write to PTP_Rate_Adj_Amt through PTP_Time_Config_ns registers [24:0]. A 2's complement representation should be used if a negative rate adjustment is needed. 110: Rate Read 111: Rate Write

Bit	Name	Type	Default	Description
16.0	ptp_clkadj_mod_set	RW, SC	0	PTP Clock Adjustment Mode Set. 1: Activate the selected clock adjustment mode as related parameters are properly inserted.

8.5.32. PTP_CFG_NS_LO (PTP Time Config Nano-Sec Low Register, Page 0xe41, Address 0x11)

**Note: This register applies to the RTL8211FS(I)-VS only.*

Table 56. PTP_CFG_NS_LO (PTP Time Config Nano-Sec Low Register, Page 0xe41, Address 0x11)

Bit	Name	Type	Default	Description
17.15:0	PTP_Time_Config_ns[15:0]	RW	0x0000	Time configuration nano-sec field [15:0] / Rate adjustment multiplier field [15:0] A 2's complement representation should be used if a negative rate adjustment is needed.

8.5.33. PTP_CFG_NS_HI (PTP Time Config Nano-Sec High Register, Page 0xe41, Address 0x12)

**Note: This register applies to the RTL8211FS(I)-VS only.*

Table 57. PTP_CFG_NS_HI (PTP Time Config Nano-Sec High Register, Page 0xe41, Address 0x12)

Bit	Name	Type	Default	Description
18.15:14	RSVD	RO	00	Reserved.
18.13:0	PTP_Time_Config_ns[29:16]	RW	0	Time configuration nano-sec field_ns [29:16]/ Rate adjustment multiplier field [24:16]; [24]: Rate adjustment Sign bit (1: higher rate; 0: lower rate); [29:25]: No effect when write, Reflect Sign Extension result when read. A 2's complement representation should be used if a negative rate adjustment is needed.

8.5.34. PTP_CFG_S_LO (PTP Time Config Sec Low Register, Page 0xe41, Address 0x13)

**Note: This register applies to the RTL8211FS(I)-VS only.*

Table 58. PTP_CFG_S_LO (PTP Time Config Sec Low Register, Page 0xe41, Address 0x13)

Bit	Name	Type	Default	Description
19.15:0	PTP_Time_Config_s[15:0]	RW	0x0000	Time configuration sec field [15:0].

8.5.35. PTP_CFG_S_MI (PTP Time Config Sec Mid Register, Page 0xe41, Address 0x14)

**Note: This register applies to the RTL8211FS(I)-VS only.*

Table 59. PTP_CFG_S_MI (PTP Time Config Sec Mid Register, Page 0xe41, Address 0x14)

Bit	Name	Type	Default	Description
20.15:0	PTP_Time_Config_s[31:16]	RW	0x0000	Time configuration sec field [31:16].

8.5.36. PTP_ CFG_S_HI (PTP Time Config Sec High Register, Page 0xe41, Address 0x15)

**Note: This register applies to the RTL8211FS(I)-VS only.*

Table 60. PTP_S_HI (PTP Time Config Sec High Register, Page 0xe41, Address 0x15)

Bit	Name	Type	Default	Description
21.15:0	PTP_Time_Config_s[47:32]	RW	0x0000	Time configuration sec field [47:32].

8.5.37. PTP_TAI_CFG (PTP Application I/F Config Register, Page 0xe42, Address 0x10)

**Note: This register applies to the RTL8211FS(I)-VS only.*

Table 61. PTP_TAI_CFG (PTP Application I/F Config Register, Page 0xe42, Address 0x10)

Bit	Name	Type	Default	Description
16.15:10	RSVD	RO	000000	Reserved.
16.9:8	trig_mod_sel	RW	00	Trigger Generate mode select. Trigger(s) start at time specified in TAI_TS_RW registers. Valid if tai_func_sel = 01. 00: Single rising edge 01: Single falling edge (The high/low level of the GPIO will be adjusted by HW automatically.) 10: Single pulse. The pulse width can be set by pulse_amt fields 11: Periodic pulses. The pulse period and duty cycle can be set by pulse_amt (Page 0xe42, Reg 17, bit[9:0]) and pulse_dc (Page 0xe42, Reg 17, bit[13:12]) fields, see section 8.5.38.
16.7	trig_iflate	RW	0	Trigger-if-Late Control. Valid if tai_func_sel (Bit 16.2:1) = 01. 1: Allow an immediate Trigger when setting a time value which is earlier than the current time.

Bit	Name	Type	Default	Description
16.6	evnt_rf_det	RW	0	Event Capture rising/falling edge detect selection. Valid if tai_func_sel (Bit 16.2:1) = 10. 0: Detection of a rising edge 1: Detection of a falling edge SW should take care of the high/low level of GPIO with this setting.
16.5	evnt_overwr_en	RW	1	Event Capture timestamp overwrite enable. Valid if tai_func_sel (Bit 16.2:1) = 10. 0: Keep the old value, 1: Cause the event timestamp to be overwritten if a new event is detected at the specific GPIO if the upper layer has not yet read the old event timestamp.
16.4:3	tai_gpio_num	RW	00	The GPIO number that is going to be armed.
16.2:1	tai_func_sel	RW	00	PTP Application Interface function select of selected GPIO. 00: Disable function 01: Trigger Generate 10: Event Capture 11: Trigger start time/Event timestamp read (according to current GPIO settings)
16.0	tai_cfg_set	RW, SC	0	PTP Application Interface configuration set. Setting this bit will issue a TAI Configuration 'Set' to the selected GPIO via tai_gpio_num

8.5.38. PTP_TRIG_CFG (PTP Trigger Config Register, Page 0xe42, Address 0x11)

**Note: This register applies to the RTL8211FS(I)-VS only.*

Table 62. PTP_TRIG_CFG (PTP Trigger Config Register, Page 0xe42, Address 0x11)

Bit	Name	Type	Default	Description
17.15:14	RSVD	RO	00	Reserved.
17.13:12	pulse_dc	RW	00	Duty Cycle of a Trigger Pulse. Valid if tai_func_sel (Page 0xe42, Reg 16, bit[2:1]) = 01. Takes effect only on GPIO 0/1. 00: 0% 01: 25% 10: 50% 11: 75%. *Note: The options of 0%, 25%, and 75% are available only when pulse_amt_unit >= 8*PTPCLK period (64 ns).*
17.11:10	pulse_amt_unit	RW	00	The unit of pulse_amt field. 00: nano-second (ns) 01: micro-second (us) 10: milli-second (ms) 11: second (s)

Bit	Name	Type	Default	Description
17.9:0	pulse_amt	RW	0	Period of periodic pulses/Width of the single pulse. *Note 1: when pulse_amt_unit = 2'b00, the value that pulse_amt take effect will be floored to the multiple of PTPCLK period (8ns).* *Note 2: pulse_amt should be greater than 0.*

8.5.39. PTP_TAI_STA (PTP Application I/F Status Register, Page 0xe42, Address 0x12)

**Note: This register applies to the RTL8211FS(I)-VS only.*

Table 63. PTP_TAI_STA (PTP Application I/F Status Register, Page 0xe42, Address 0x12)

Bit	Name	Type	Default	Description
18.15	tai_gpio0_func	RO	0	Indicate GPIO0's function 0: Trigger Generate 1: Event Capture
18.14	tai_gpio0_en	RO	0	GPIO0 function is enabled.
18.13	tai_gpio0_notify	RO,RC	0	Indicate if a Trigger is generated or Event Detected at GPIO0.
18.12	tai_gpio0_err	RO,RC	0	Indicate the start-time of the Trigger is earlier than the current time/an old Event timestamp value is kept at GPIO0.
18.11	tai_gpio1_func	RO	0	Indicate GPIO1's function 0: Trigger Generate 1: Event Capture
18.10	tai_gpio1_en	RO	0	GPIO1 function is enabled.
18.9	tai_gpio1_notify	RO,RC	0	Indicate if a Trigger is generated or Event Detected at GPIO1.
18.8	tai_gpio1_err	RO,RC	0	Indicate the start-time of the Trigger is earlier than the current time/an old Event timestamp value is kept at GPIO1.
18.7:0	RSVD	RO	0x00	Reserved.

8.5.40. PTP_TAI_TS_NS_LO (PTP TAI Timestamp Nano-Sec Low Register, Page 0xe42, Address 0x13)

**Note: This register applies to the RTL8211FS(I)-VS only.*

Table 64. PTP_TAI_TS_NS_LO (PTP TAI Timestamp Nano-Sec Low Register, Page 0xe42, Address 0x13)

Bit	Name	Type	Default	Description
19.15:0	TAI_TS_ns[15:0]	RW	0x0000	PTP Application Interface timestamp Read/Write interface nanosec field [15:0].

8.5.41. PTP_TAI_TS_NS_HI (PTP TAI Timestamp Nano-Sec High Register, Page 0xe42, Address 0x14)

**Note: This register applies to the RTL8211FS(I)-VS only.*

Table 65. PTP_TAI_TS_NS_HI (PTP TAI Timestamp Nano-Sec High Register, Page 0xe42, Address 0x14)

Bit	Name	Type	Default	Description
20.15:14	RSVD	RO	00	Reserved.
20.13:0	TAI_TS_ns[29:16]	RW	0	PTP Application Interface timestamp Read/Write interface nanosec field [29:16].

8.5.42. PTP_TAI_TS_S_LO (PTP TAI Timestamp Sec Low Register, Page 0xe42, Address 0x15)

***Note: This register applies to the RTL8211FS(I)-VS only.*

Table 66. PTP_S_LO (PTP Time Config Sec Low Register, Page 0xe41, Address 0x13)

Bit	Name	Type	Default	Description
21.15:0	TAI_TS_s[15:0]	RW	0x0000	PTP Application Interface timestamp Read/Write interface sec field [15:0].

8.5.43. PTP_TAI_TS_S_HI (PTP TAI Timestamp Sec High Register, Page 0xe42, Address 0x16)

**Note: This register applies to the RTL8211FS(I)-VS only.*

Table 67. PTP_S_MI (PTP Time Config Sec Mid Register, Page 0xe41, Address 0x14)

Bit	Name	Type	Default	Description
22.15:0	TAI_TS_s[31:16]	RW	0x0000	PTP Application Interface timestamp Read/Write interface sec field [31:16].

8.5.44. PTP_TRX_TS_STA (PTP TxRx Timestamp Status Register, Page 0xe43, Address 0x10)

**Note: This register applies to the RTL8211FS(I)-VS only.*

Table 68. PTP_TRX_TS_STA (PTP TxRx Timestamp Status Register, Page 0xe43, Address 0x10)

Bit	Name	Type	Default	Description
16.15	txts_sync_rdy	RO	0	Sync message Transmit timestamp ready.
16.14	txts_dlyreq_rdy	RO	0	Delay_Request Transmit timestamp ready.
16.13	txts_pdlyreq_rdy	RO	0	PDelay_Request Transmit timestamp ready.
16.12	txts_pdlyrsp_rdy	RO	0	PDelay_Response Transmit timestamp ready.
16.11	rxts_sync_rdy	RO	0	Sync message Receive timestamp ready.
16.10	rxts_dlyreq_rdy	RO	0	Delay_Request Receive timestamp ready.

Bit	Name	Type	Default	Description
16.9	rxts_pdlyreq_rdy	RO	0	PDelay_Request Receive timestamp ready.
16.8	rxts_pdlyrsp_rdy	RO	0	PDelay_Response Receive timestamp ready.
16.7:5	RSVD	RO	000	Reserved.
16.4	trxts_overwr_en	RW	1	Transmit/Receive timestamp overwrite enable. When a new PTP packet comes that needs to be time stamped, HW will 0: Keep the old timestamp value, 1: Overwrite the old timestamp value if the older one has not been read by the upper layer.
16.3:2	trxts_msgtype_sel	RW	00	Message Type of Transmit/Receive timestamp select. 00: Sync 01: Delay_Request 10: PDelay_Request 11: PDelay_Response
16.1	trxts_sel	RW	0	Transmit/Receive timestamp read select. 0: Tx 1: Rx
16.0	trxts_rd	RW, SC	0	Transmit/Receive timestamp read enable. Issue a 'Read' for Transmit/Receive timestamp.

8.5.45. PTP_TRX_TS_INFO (PTP TxRx Timestamp Info Register, Page 0xe44, Address 0x10)

**Note: This register applies to the RTL8211FS(I)-VS only.*

Table 69. PTP_TRX_TS_INFO (PTP TxRx Timestamp Info Register, Page 0xe44, Address 0x10)

Bit	Name	Type	Default	Description
16.15:12	trxts_transspec	RO	0000	Transmit/Receive timestamp Transport Specific field
16.11:8	trxts_msgtype	RO	0000	Transmit/Receive timestamp Message Type field
16.7:4	RSVD	RO	0000	Reserved
16.3:0	trxts_ptpver	RO	0000	Transmit/Receive timestamp PTP Version field

8.5.46. PTP_TRX_TS_SH (PTP TxRx Timestamp Source Hash Register, Page 0xe44, Address 0x11)

**Note: This register applies to the RTL8211FS(I)-VS only.*

Table 70. PTP_TRX_TS_SH (PTP TxRx Timestamp Source Hash Register, Page 0xe44, Address 0x11)

Bit	Name	Type	Default	Description
17.15:0	trxts_srchash	RO	0x0000	Transmit/Receive timestamp Source Port ID Hash field.

8.5.47. PTP_TRX_TS_SID (PTP TxRx Timestamp Seq ID Register, Page 0xe44, Address 0x12)

**Note: This register applies to the RTL8211FS(I)-VS only.*

Table 71. PTP_TRX_TS_SID (PTP TxRx Timestamp Seq ID Register, Page 0xe44, Address 0x12)

Bit	Name	Type	Default	Description
18.15:0	trxts_seqid	RO	0x0000	Transmit/Receive timestamp Sequence ID field.

8.5.48. PTP_ TRX_TS NS_LO (PTP TxRx Timestamp Nano-Sec Low Register, Page 0xe44, Address 0x13)

**Note: This register applies to the RTL8211FS(I)-VS only.*

Table 72. PTP_ TRX_TS NS_LO (PTP TxRx Timestamp Nano-Sec Low Register, Page 0xe44, Address 0x13)

Bit	Name	Type	Default	Description
19.15:0	TXRX_TS_ns[15:0]	RO	0x0000	Transmit/Receive timestamp nanosec field [15:0]

8.5.49. PTP_ TRX_TS NS_HI (PTP TxRx Timestamp Nano-Sec High Register, Page 0xe44, Address 0x14)

**Note: This register applies to the RTL8211FS(I)-VS only.*

Table 73. PTP_ TRX_TS NS_HI (PTP TxRx Timestamp Nano-Sec High Register, Page 0xe44, Address 0x14)

Bit	Name	Type	Default	Description
20.15:14	RSVD	RO	00	Reserved.
20.13:0	TXRX_TS_ns[29:16]	RW	0	Transmit/Receive timestamp nanosec field [29:16]

8.5.50. PTP_ TRX_TS S_LO (PTP TxRx Timestamp Sec Low Register, Page 0xe44, Address 0x15)

**Note: This register applies to the RTL8211FS(I)-VS only.*

Table 74. PTP_ TRX_TS S_LO (PTP TxRx Timestamp Sec Low Register, Page 0xe44, Address 0x15)

Bit	Name	Type	Default	Description
21.15:0	TXRX_TS_s[15:0]	RW	0x0000	Transmit/Receive timestamp sec field [15:0].

8.5.51. PTP_ TRX_TS S_MI (PTP TxRx Timestamp Sec Mid Register, Page 0xe44, Address 0x16)

**Note: This register applies to the RTL8211FS(I)-VS only.*

Table 75. PTP_ TRX_TS S_MID (PTP TxRx Timestamp Sec Mid Register, Page 0xe44, Address 0x16)

Bit	Name	Type	Default	Description
22.15:0	TXRX_TS_s[31:16]	RW	0x0000	Transmit/Receive timestamp sec field [31:16].

8.5.52. PTP_ TRX_TS S_HI (PTP TxRx Timestamp Sec High Register, Page 0xe44, Address 0x17)

**Note: This register applies to the RTL8211FS(I)-VS only.*

Table 76. PTP_ TRX_TS S_LO (PTP TxRx Timestamp Sec High Register, Page 0xe44, Address 0x17)

Bit	Name	Type	Default	Description
23.15:0	TXRX_TS_s[47:32]	RW	0x0000	Transmit/Receive timestamp sec field [47:32].

8.5.53. PC1R (PCS Control 1 Register, MMD Device 3, Address 0x00)

Table 77. PC1R (PCS Control 1 Register, MMD Device 3, Address 0x00)

Bit	Name	Type	Default	Description
3.0.15:11	RSVD	RW	0	Reserved.
3.0.10	Clock Stop Enable	RW	0	1: PHY stops RXC when receiving LPI 0: RXC not stoppable
3.0.9:0	RSVD	RW	0	Reserved.

8.5.54. PS1R (PCS Status1 Register, MMD Device 3, Address 0x01)

Table 78. PS1R (PCS Status 1 Register, MMD Device 3, Address 0x01)

Bit	Name	Type	Default	Description
3.1.15:12	RSVD	RO	0	Reserved.
3.1.11	TX LPI Received	RO, LH	0	1: TX PCS has received LPI 0: LPI not received
3.1.10	RX LPI Received	RO, LH	0	1: RX PCS has received LPI 0: LPI not received
3.19	TX LPI Indication	RO	0	1: TX PCS is currently receiving LPI 0: TX PCS is not currently receiving LPI
3.1.8	RX LPI Indication	RO	0	1: RX PCS is currently receiving LPI 0: RX PCS is not currently receiving LPI
3.1.7	RSVD	RO	0	Reserved.
3.1.6	Clock Stop Capable	RO	1	1: MAC stops TXC in LPI 0: TXC not stoppable
3.1.5:0	RSVD	RO	0	Reserved.

8.5.55. EEECR (EEE Capability Register, MMD Device 3, Address 0x14)

Table 79. EEECR (EEE Capability Register, MMD Device 3, Address 0x14)

Bit	Name	Type	Default	Description
3.20.15:3	RSVD	RO	0	Reserved.
3.20.2	1000Base-T EEE	RO	1	1: EEE is supported for 1000Base-T EEE 0: EEE is not supported for 1000Base-T EEE
3.20.1	100Base-TX EEE	RO	1	1: EEE is supported for 100Base-TX EEE 0: EEE is not supported for 100Base-TX EEE
3.20.0	RSVD	RO	0	Reserved.

8.5.56. EEEWER (EEE Wake Error Register, MMD Device 3, Address 0x16)

Table 80. EEEWER (EEE Wake Error Register, MMD Device 3, Address 0x16)

Bit	Name	Type	Default	Description
3.22.15:0	EEE Wake Error Counter	RC	0	Used by PHY types that support EEE to count wake time faults where the PHY fails to complete its normal wake sequence within the time required for the specific PHY type.

8.5.57. EEEAR (EEE Advertisement Register, MMD Device 7, Address 0x3c)

Table 81. EEEAR (EEE Advertisement Register, MMD Device 7, Address 0x3c)

Bit	Name	Type	Default	Description
7.60.15:3	RSVD	RW	0	Reserved.
7.60.2	1000Base-T EEE	RW	1	Advertise 1000Base-T EEE Capability. 1: Advertise 0: Do not advertise
7.60.1	100Base-TX EEE	RW	1	Advertise 100Base-TX EEE Capability. 1: Advertise 0: Do not advertise
7.60.0	RSVD	RW	0	Reserved.

8.5.58. EEELPAR (EEE Link Partner Ability Register, MMD Device 7, Address 0x3d)

Table 82. EEELPAR (EEE Link Partner Ability Register, MMD Device 7, Address 0x3d)

Bit	Name	Type	Default	Description
7.61.15:3	RSVD	RO	0	Reserved.
7.61.2	LP 1000Base-T EEE	RO	0	1: Link Partner is capable of 1000Base-T EEE 0: Link Partner is not capable of 1000Base-T EEE
7.61.1	LP 100Base-TX EEE	RO	0	1: Link Partner is capable of 100Base-TX EEE 0: Link Partner is not capable of 100Base-TX EEE
7.61.0	RSVD	RO	0	Reserved.

8.5.59. Fiber BMCR (Fiber Basic Mode Control Register, Address 0x00)

Table 83. Fiber BMCR (Fiber Basic Mode Control Register, Address 0x00)

<table>
<tr><th>Bit</th><th>Name</th><th>RW</th><th>Default</th><th>Description</th></tr>
<tr><td>0.15</td><td>Reset</td><td>RW, SC</td><td>0</td><td>Software Reset.
1: PHY reset
0: Normal operation
Register 0 (Fiber BMCR) and register 1 (Fiber BMSR) will return to default values after a software reset (set Bit 0.15 to 1).
This action may change the internal PHY state and the state of the physical link associated with the PHY.</td></tr>
<tr><td>0.14</td><td>Loopback</td><td>RW</td><td>0</td><td>Loopback Mode.
1: Enable PCS loopback mode
0: Disable PCS loopback mode</td></tr>
<tr><td>0.13</td><td>Speed[0]</td><td>RW</td><td>0</td><td>Speed Select Bit 0.
In forced mode, i.e., when Auto-Negotiation is disabled, bits 6 and 13 determine device speed selection.
<table>
<tr><th>Speed[1]</th><th>Speed[0]</th><th>Speed Enabled</th></tr>
<tr><td>1</td><td>1</td><td>Reserved</td></tr>
<tr><td>1</td><td>0</td><td>1000Mbps</td></tr>
<tr><td>0</td><td>1</td><td>100Mbps</td></tr>
<tr><td>0</td><td>0</td><td>10Mbps</td></tr>
</table></td></tr>
<tr><td>0.12</td><td>ANE</td><td>RW</td><td>1</td><td>Auto-Negotiation Enable.
1: Enable Auto-Negotiation
0: Disable Auto-Negotiation</td></tr>
<tr><td>0.11</td><td>PWD</td><td>RW</td><td>0</td><td>Power Down.
1: Power down (only Management Interface and logic are active; link is down)
0: Normal operation</td></tr>
<tr><td>0.10</td><td>Isolate</td><td>RW</td><td>0</td><td>Isolate.
1: RGMII interface is isolated; the serial management interface (MDC, MDIO) is still active. When this bit is asserted, the RTL8211FS(I)(-VS) ignores TXD[3:0], and TXCTL inputs, and presents a high impedance on TXC, RXC, RXCTL, RXD[3:0].
0: Normal operation</td></tr>
<tr><td>0.9</td><td>Restart_AN</td><td>RW, SC</td><td>0</td><td>Restart Auto-Negotiation.
1: Restart Auto-Negotiation
0: Normal operation</td></tr>
<tr><td>0.8</td><td>Duplex</td><td>RW</td><td>1</td><td>Duplex Mode.
1: Full Duplex operation
0: Half Duplex operation
This bit is valid only in force mode, i.e., NWay is disabled.</td></tr>
<tr><td>0.7</td><td>Collision Test</td><td>RW</td><td>0</td><td>Collision Test.
1: Collision test enabled
0: Normal operation</td></tr>
</table>

Bit	Name	RW	Default	Description
0.6	Speed[1]	RW	1	Speed Select Bit 1. Refer to bit 0.13.
0.5	Uni-directional enable	RW	0	Uni-Directional Enable 1: Enable packet transmit without respect to linkok status 0: Packet transmit permitted when link is established
0.4:0	RSVD	RO	00000	Reserved.

Note: 100Base-FX does not have Auto-Negotiation, and the AN (0.9) needs to be disabled (0.9=0). The speed capabilities bits 0.13, 0.6 are set to 100Mbps.

8.5.60. Fiber BMSR (Basic Mode Status Register, Address 0x01)

Table 84. Fiber BMSR (Fiber Basic Mode Status Register, Address 0x01)

Bit	Name	Type	Default	Description
1.15	100Base-T4	RO	0	100Base-T4 Capability. The RTL8211FS(I)(-VS) does not support 100Base-T4 mode. This bit should always be 0.
1.14	100Base-FX (Full)	RO	0	100Base-FX Full Duplex Capability. 1: Device is able to perform 100Base-X in full duplex mode 0: Device is not able to perform 100Base-X in full duplex mode
1.13	100Base-FX (Half)	RO	0	100Base-FX Half Duplex Capability. 1: Device is able to perform 100Base-X in half duplex mode 0: Device is not able to perform 100Base-X in half duplex mode
1.12	10Base-T (Full)	RO	0	10Base-T Full Duplex Capability. 1: Device is able to perform 10Base-T in full duplex mode. 0: Device is not able to perform 10Base-T in full duplex mode.
1.11	10Base-T (Half)	RO	0	10Base-T Half Duplex Capability. 1: Device is able to perform 10Base-T in half duplex mode 0: Device is not able to perform 10Base-T in half duplex mode
1.10	100Base-T2 (Full)	RO	0	100Base-T2 Full Duplex Capability. The RTL8211FS(I)(-VS) does not support 100Base-T2 mode and this bit should always be 0.
1.9	100Base-T2 (Half)	RO	0	100Base-T2 Half Duplex Capability. The RTL8211FS(I)(-VS) does not support 100Base-T2 mode. This bit should always be 0.
1.8	Extended Status	RO	1	Support Extended Status Register. 1: Device supports Extended Status Register 0x0F (15) 0: Device does not support Extended Status Register 0x0F This register is read-only and is always set to 1.
1.7	RSVD	RO	0	Reserved.
1.6	Preamble Suppression	RO	0	Preamble Suppression Capability. The RTL8211FS(I)(-VS) default will not accept MDC/MDIO transactions with preamble suppressed.

Bit	Name	Type	Default	Description
1.5	Auto-Negotiation Complete	RO	0	Auto-Negotiation Complete. 1: Auto-Negotiation process complete, and contents of registers 5, 6, 8, and 10 are valid 0: Auto-Negotiation process not complete
1.4	Remote Fault	RC, LH	0	Remote Fault. 1: Remote fault condition detected (cleared on read or by reset). Indication or notification of remote fault from Link Partner 0: No remote fault condition detected
1.3	Auto-Negotiation Ability	RO	1	Auto Configured Link. 1: Device is able to perform Auto-Negotiation 0: Device is not able to perform Auto-Negotiation
1.2	Link Status	RO	0	Link Status. 1: Linked 0: Not Linked
1.1	Jabber Detect	RC, LH	0	Jabber Detect. 1: Jabber condition detected 0: No Jabber occurred
1.0	Extended Capability	RO	1	1: Extended register capabilities, always 1

8.5.61. 1000Base-X ANAR (1000Base-X Auto-Negotiation Advertising Register, Address 0x04)

Table 85. 1000Base-X ANAR (Auto-Negotiation Advertising Register, Address 0x04)

Bit	Name	RW	Default	Description
4.15	Next Page	RW	0	1: Additional next pages exchange desired 0: No additional next pages exchange desired
4.14	RSVD	RO	0	Reserved.
4.13:12	Remote Fault	RW	00	Remote Fault. Used to indicate to the link partner that a remote fault condition has been detected: 00: No Error, Link OK 01: Link Failure 10: Off Line 11: Auto-Negotiation Error
4.11:9	RSVD	RO	000	Reserved.
4.8:7	PAUSE	RW	00	Pause. Used to indicate pause capabilities to the link partner. 00: No Pause 01: Symmetric Pause 10: Asymmetric Pause 11: Both Symmetric and Asymmetric Pause
4.6	Half Duplex	RW	0	1'b1: Support half duplex to link partner.
4.5	Full Duplex	RW	1	1'b1: Support full duplex to link partner.
4.4:0	RSVD	RW	00000	Reserved.

Note: The setting of Fiber ANAR Register is valid only when ANE is enabled in the 1000Base-X auto-negotiation mode.

8.5.62. 1000Base-X ANLPAR (1000Base-X Auto-Negotiation Link Partner Ability Register, Address 0x05)

Table 86. 1000Base-X ANLPAR (Auto-Negotiation Link Partner Ability Register, Address 0x05)

Bit	Name	RW	Default	Description
5.15	Next Page	RO	0	Support for transmission and reception of additional link code word encodings.
5.14	ACK	RO	0	Indicates link partner successfully received the previously transmitted base page.
5.13:12	Remote Fault	RO	00	Remote Fault. Used to indicate to the link partner that a remote fault condition has been detected: 00: No Error, Link OK 01: Link Failure 10: Off Line 11: Auto-Negotiation Error
5.11:9	RSVD	RO	000	Reserved.
5.8:7	PAUSE	RO	00	Pause. Used by link partner to indicate its pause capabilities. 00: No Pause 01: Symmetric Pause 10: Asymmetric Pause 11: Both Symmetric and Asymmetric Pause
5.6	Half Duplex	RO	0	1: Link partner support half duplex.
5.5	Full Duplex	RO	0	0: Link partner support full duplex.
5.4:0	RSVD	RO	00000	Reserved.

Note: The setting of Fiber ANLPAR Register is valid only in the 1000Base-X auto-negotiation mode.

8.5.63. Fiber ESR (Fiber Extended Status Register, Address 0x0F)

Table 87. Fiber ESR (Fiber Extended Status Register, Address 0x0F)

Bit	Name	RW	Default	Description
15.15	1000Base-X FD	RO	1	1: Support 1000Base-X full duplex capability.
15.14	1000Base-X HD	RO	0	1: Support 1000Base-X half duplex capability.
15.13:0	RSVD	RO	00000000000000	Reserved.

8.5.64. SERDES INER (SERDES Interrupt Enable Register, Page 0xde1, Address 0x11)

Table 88. SERDES INER (SERDES Interrupt Enable Register, Page 0xde1, Address 0x11)

Bit	Name	RW	Default	Description
17.15:8	RSVD	RO	00000000	Reserved.
17.7	Fiber Speed Changed Interrupt	RW	0	1: Interrupt Enable 0: Interrupt Disable Setting this bit to 0 only disables the Fiber speed change interrupt event in the INTB pin. SERDES INSR Bit[7] always reflects the Fiber speed change interrupt behavior.
17.6	Fiber Duplex Changed Interrupt	RW	0	1: Interrupt Enable 0: Interrupt Disable Setting this bit to 0 only disables the Fiber duplex change interrupt event in the INTB pin. SERDES INSR Bit[6] always reflects the Fiber duplex change interrupt behavior.
17.5	Fiber/SGMII Signal Detection Changed Interrupt	RW	0	1: Interrupt Enable 0: Interrupt Disable Setting this bit to 0 only disables the Fiber/SGMII signal detection change interrupt event in the INTB pin. SERDES INSR Bit[5] always reflects the Fiber/SGMII signal detection change interrupt behavior.
17.4	Fiber/SGMII Link Status Change Interrupt	RW	0	1: Interrupt Enable 0: Interrupt Disable Setting this bit to 0 only disables the Fiber/SGMII link status change interrupt event in the INTB pin. SERDES INSR Bit[4] always reflects the Fiber/SGMII link change interrupt behavior.
17.3:1	RSVD	RO	000	Reserved.
17.0	Fiber/SGMII Auto-Negotiation Error Interrupt	RW	0	1: Interrupt Enable 0: Interrupt Disable Setting this bit to 0 only disables the Fiber/SGMII auto-negotiation error interrupt event in the INTB pin. SERDES INSR Bit[0] always reflects the Fiber/SGMII auto-negotiation error interrupt behavior.

8.5.65. SERDES INSR (SERDES Interrupt Status Register, Page 0xde1, Address 0x12)

Table 89. SERDES INSR (SERDES Interrupt Status Register, Page 0xde1, Address 0x12)

Bit	Name	RW	Default	Description
18.15:8	RSVD	RO, RC	00000000	Reserved.
18.7	Fiber Speed Changed	RO, RC	0	1: Fiber Speed Changed 0: No Fiber Speed Changed
18.6	Fiber Duplex Changed	RO, RC	0	1: Fiber Duplex Changed 0: No Fiber Duplex Changed
18.5	SERDES Signal Detection Changed	RO, RC	0	1: Fiber/SGMII Signal Detection Changed 0: No Fiber/SGMII Signal Detection Changed

Bit	Name	RW	Default	Description
18.4	SERDES Link Status Change	RO, RC	0	1: Fiber/SGMII Link Status Change 0: No Fiber/SGMII Link Status Change
18.3:1	RSVD	RO, RC	000	Reserved.
18.0	SERDES Auto-Negotiation Error	RO, RC	0	1: Fiber/SGMII Auto-Negotiation Error 0: No Fiber/SGMII Auto-Negotiation Error

8.5.66. SGMII ANARSEL (SGMII Auto-Negotiation Advertising Register Select, Page 0xd08, Address 0x14)

Table 90. SGMII ANARSEL (SGMII Auto-Negotiation Advertising Register Select, Page 0xd08, Address 0x14)

Bit	Name	RW	Default	Description
20.15:12	RSVD	RO	0000	Reserved.
20.11	En_Select Link Info	RW	0	1: Enable link information is selected by register.
20.10	RSVD	RO	0	Reserved.
20.9:8	Select Link Info.	RW	00	Select link information. 00: Reserved 01: Reserved 10: Reserved 11: Select link information by SGMII ANAR
20.7:0	RSVD	RW	00000000	Reserved.

8.5.67. SGMII ANAR (SGMII Auto-Negotiation Advertising Register, Page 0xd08, Address 0x10)

Table 91. SGMII ANAR (SGMII Auto-Negotiation Advertising Register, Page 0xd08, Address 0x10)

Bit	Name	RW	Default	Description
16.15:7	RSVD	RO	000000000	Reserved.
16.6:4	RSVD	RW	101	Reserved.
16.3	Link Status	RW	0	Link Status. 1: Linked 0: Not Linked
16.2	Duplex	RW	0	Duplex Mode. 1: Full Duplex operation 0: Half Duplex operation
16.1:0	Speed	RW	00	Speed. 00: 10Mbps 01: 100Mbps 10: 1000Mbps 11: Reserved

8.5.68. SGMII ANLPAR (SGMII Auto-Negotiation Link Partner Ability Register, Page 0xdc0, Address 0x15)

Table 92. SGMII ANLPAR (SGMII Auto-Negotiation Link Partner Ability Register, Page 0xdc0, Address 0x15)

Bit	Name	RW	Default	Description
21.15	Link Status	RO	0	Link Status. 1: Linked; 0: Not Linked
21.14:13	RSVD	RO	00	Reserved.
21.12	Duplex	RO	0	Duplex Mode. 1: Full Duplex operation 0: Half Duplex operation
21.11:10	Speed	RO	00	Speed. 00: 10Mbps 01: 100Mbps 10: 1000Mbps 11: Reserved
21.9:0	RSVD	RO	0000000000	Reserved.

9. Switching Regulator

The RTL8211FS(I)(-VS) incorporates a state-of-the-art switching regulator that requires a well-designed PCB layout in order to achieve good power efficiency and lower the output voltage ripple and input overshoot. The switching regulator 1.0V output pin (REG_OUT) should be connected only to DVDD10 and AVDD10 (do not provide this power source to other devices).

Use an X5R/X7R low-ESR ceramic capacitor as the output capacitor for switching regulator stability.

Note: Refer to the RTL8211F Series Layout Guide for detailed description.

9.1. Power Sequence

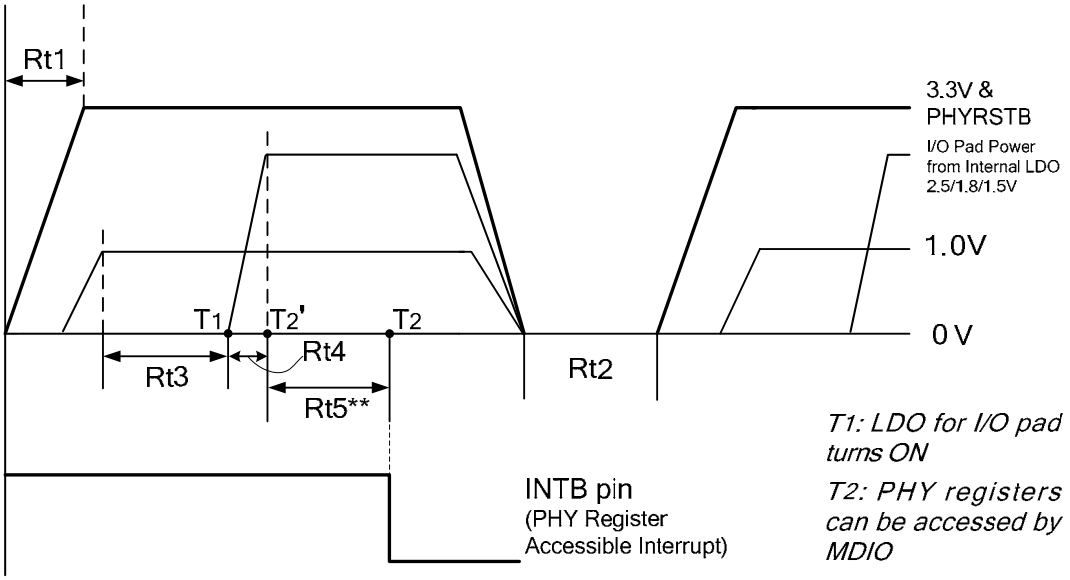


Figure 15. Power Sequence

Table 93. Power Sequence Parameters

Symbol	Description	Min	Typical	Max	Units
Rt1	3.3V Rise Time External I/O Pad Power Rise Time	0.5*	-	100	ms
Rt2	3.3V Off Time	100	-	-	ms
Rt3	Core Logic Ready Time	45	-	-	ms
Rt4	LDO Ready Time	1.5	-	-	ms
Rt5**	Reserved for Specific Parameter Configuration	-	-	100	ms

Note 1: The RTL8211FS(I)(-VS) does not support fast 3.3V rising. The 3.3V rise time should be controlled over 0.5ms.
** A 3.3V rise time between 0.1ms to 0.5ms is conditionally permitted only if the system 3.3V power budget is sufficient to ensure that 3.3V Overcurrent Protection (OCP) will NOT be triggered during the power-on procedure. If the rise time is less than 0.1ms, it will induce a peak voltage in VDD_REG which may cause permanent damage to the regulator.*

Note 2: If there is any action that involves consecutive ON/OFF toggling of the switching-regulator source (3.3V), the design must make sure the OFF state of both the switching-regulator source (3.3V) and output (1.0V) reach 0V, and the time period between the consecutive ON/OFF toggling action must be longer than 100ms.

Note 3: When using an external oscillator or clock source, on stopping the clock source the RTL8211FS(I)(-VS) must also be powered off.

Note 4: The RTL8211FS(I)(-VS) use the integrated LDO to generate the 2.5V, 1.8V, and 1.5V voltages for the I/O pad, the I/O pad voltage can be selected by using the CONFIG pins CFG_LDO[1:0].

Note 5: Rt5 is a reserved window for some PHY special parameter configuration with 100ms duration. The parameters, if needed, can be provided by Realtek. At the point of T_2, i.e. the end of this configuration window, all the PHY registers can be accessed through MDIO.

*** Currently there is no special configuration needed for the RTL8211FS(I)(-VS), the Rt5 can be skipped by setting Page 0xa46, Reg. 20, bit[1]=1 (PHY Special Config Done) at the point of T_2'. The 'PHY Register Accessible Interrupt' will then trigger accordingly, which indicates the PHY registers can be accessed by MDIO.*

10. Characteristics

10.1. Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltages are specified reference to GND unless otherwise specified.

Table 94. Absolute Maximum Ratings

Symbol	Description	Minimum	Maximum	Unit
VDD33, AVDD33	Supply Voltage 3.3V	-0.3	3.6	V
AVDD10, DVDD10	Supply Voltage 1.0V	-0.3	1.2	V
2.5V RGMII/GMII	Supply Voltage 2.5V	-0.2	2.8	V
1.8V RGMII	Supply Voltage 1.8V	-0.2	2.3	V
1.5V RGMII	Supply Voltage 1.5V	-0.2	2.0	V
3.3V DCinput 3.3V DCoutput	Input Voltage Output Voltage	-0.3	3.6	V
1.0V DCinput 1.0V DCoutput	Input Voltage Output Voltage	-0.3	1.2	V
NA	Storage Temperature	-55	+125	°C

Note: Refer to the most updated schematic circuit for correct configuration.

10.2. Recommended Operating Conditions

Table 95. Recommended Operating Conditions

Description	Pins	Minimum	Typical	Maximum	Unit
Supply Voltage VDD	DVDD33, AVDD33	2.97	3.3	3.63	V
	AVDD10, DVDD10	0.95	1.0	1.05	V
	2.5V RGMII/GMII	2.25	2.5	2.75	V
	1.8V RGMII	1.62	1.8	1.98	V
	1.5V RGMII	1.5	1.56	1.62	V
Ambient Operating Temperature T_A (RTL8211FS/RTL8211FS-VS)	-	0	-	70	°C
Ambient Operating Temperature T_A (RTL8211FSI/RTL8211FSI-VS)	-	-40	-	85	°C
Maximum Junction Temperature	-	-	-	125	°C

10.3. Crystal Requirements

Table 96. Crystal Requirements

Symbol	Description/Condition	Minimum	Typical	Maximum	Unit
F_{ref}	Parallel Resonant Crystal Reference Frequency, Fundamental Mode, AT-Cut Type.	-	25	-	MHz
F_{ref} Tolerance	Parallel Resonant Crystal Frequency Tolerance, Fundamental Mode, AT-Cut Type. T_a=0°C~70°C.	-50	-	+50	ppm
F_{ref} Duty Cycle	Reference Clock Input Duty Cycle.	40	-	60	%
ESR	Equivalent Series Resistance.	-	-	50	Ω
DL	Drive Level.	-	-	0.5	mW
Jitter	Broadband Peak-to-Peak Jitter1, 2	-	-	200	ps
V_{ih}_CKXTAL	Crystal Output High Level	1.4	-	-	V
V_{il}_CKXTAL	Crystal Output Low Level	-	-	0.4	V

Note 1: 25kHz to 25MHz RMS < 3ps.
Note 2: Broadband RMS < 9ps.
Note 3: F_{ref} Tolerance +/- 50ppm including effects of aging of the first year, external crystal capacitors, and PCB layout.

10.4. Oscillator/External Clock Requirements

Table 97. Oscillator/External Clock Requirements

Parameter	Condition	Minimum	Typical	Maximum	Unit
Frequency	-	-	25/50	-	MHz
Frequency Tolerance (RTL8211FS/RTL8211FS-VS)	Ta=0°C~70°C	-50	-	50	ppm
Frequency Tolerance (RTL8211FSI/RTL8211FSI-VS)	Ta=-40°C~85°C	-50	-	50	ppm
Duty Cycle	-	40	-	60	%
Broadband Peak-to-Peak Jitter [1, 2]	-	-	-	200	ps
V_{ih}	-	1.4		-	V
V_{il}	-	-	-	0.4	V
Rise Time (10%~90%)	-	-	-	10	ns
Fall Time (10%~90%)	-	-	-	10	ns
Operating Temperature Range	-	-40	-	85	°C

Note 1: 25kHz to 25MHz RMS < 3ps.
Note 2: Broadband RMS < 9ps.
Note 3: Frequency Tolerance +/- 50ppm including effects of aging of the first year, external crystal capacitors, and PCB layout.

10.5. DC Characteristics

Table 98. DC Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
VDD33, AVDD33	3.3V Supply Voltage	-	2.97	3.3	3.63	V
1. MDIO 2. RGMII I/O	2.5V RGMII Supply Voltage	-	2.25	2.5	2.75	V
1. MDIO 2. RGMII I/O	1.8V RGMII Supply Voltage	-	1.62V	1.8V	1.98V	V
1. MDIO 2. RGMII I/O	1.5V RGMII Supply Voltage	-	1.5V	1.56V	1.62V	V
DVDD10, AVDD10	1.0V Supply Voltage	-	0.95	1.0	1.05	V
Voh (3.3V)	Minimum High Level Output Voltage	-	2.4	-	VDD33 + 0.3	V
Voh (2.5V)	Minimum High Level Output Voltage	-	2.0	-	VDD25 + 0.3	V
Voh (1.8V)	Minimum High Level Output Voltage	-	0.9*VDD18	-	VDD18 + 0.3	V
Voh (1.5V)	Minimum High Level Output Voltage	-	0.9*VDD15	-	VDD15 + 0.3	V
Vol (3.3V)	Maximum Low Level Output Voltage	-	-0.3	-	0.4	V
Vol (2.5V)	Maximum Low Level Output Voltage	-	-0.3	-	0.4	V
Vol (1.8V)	Maximum Low Level Output Voltage	-	-0.3	-	0.1*VDD18	V
Vol (1.5V)	Maximum Low Level Output Voltage	-	-0.3	-	0.1*VDD15	V
Vih (3.3V)	Minimum High Level Input Voltage	-	2.0	-	-	V
Vil (3.3V)	Maximum Low Level Input Voltage	-	-	-	0.8	V
Vih (2.5V)	Minimum High Level Input Voltage	-	1.7	-	-	V
Vil (2.5V)	Maximum Low Level Input Voltage	-	-	-	0.7	V
Vih (1.8V)	Minimum High Level Input Voltage	-	1.2	-	-	V
Vil (1.8V)	Maximum Low Level Input Voltage	-	-	-	0.5	V
Vih (1.5V)	Minimum High Level Input Voltage	-	1.0	-	-	V
Vil (1.5V)	Maximum Low Level Input Voltage	-	-	-	0.3	V
Iin	Input Current	Vin=VDD33 or GND	0	-	0.5	µA

Note: Pins not mentioned above remain at 3.3V.

10.6. SGMII Characteristics

10.6.1. SGMII Differential Transmitter Characteristics

Table 99. SGMII Differential Transmitter Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Notes
UI	Unit Interval	799.76	800	800.24	ps	800ps ± 300ppm
T_X1	Eye Mask	-	-	0.15	UI	-
T_X2	Eye Mask	-	-	0.4	UI	-
T_Y1	Eye Mask	300	-	-	mV	-
T_Y2	Eye Mask	-	-	450	mV	-
$V_{TX-OFFSET}$	Output Offset Voltage	600	800	1000	mV	-
$V_{TX-DIFFp-p}$	Output Differential Voltage	600	800	900	mV	-
T_{TX-EYE}	Minimum TX Eye Width	0.7	-	-	UI	-
$T_{TX-JITTER}$	Output Jitter	-	-	0.3	UI	$T_{TX-JITTER-MAX}$ = 1 - $T_{TX-EYE-MIN}$ = 0.3UI
$T_{TX-RISE}$	Output Rise Time	0.125	-	0.25	UI	20% ~ 80%
$T_{TX-FALL}$	Output Fall Time	0.125	-	0.25	UI	20% ~ 80%
R_{TX}	Differential Resistance	80	100	120	ohm	-
C_{TX}	AC Coupling Capacitor	80	100	120	nF	-
L_{TX}	Transmit Length in PCB	-	-	10	inch	-

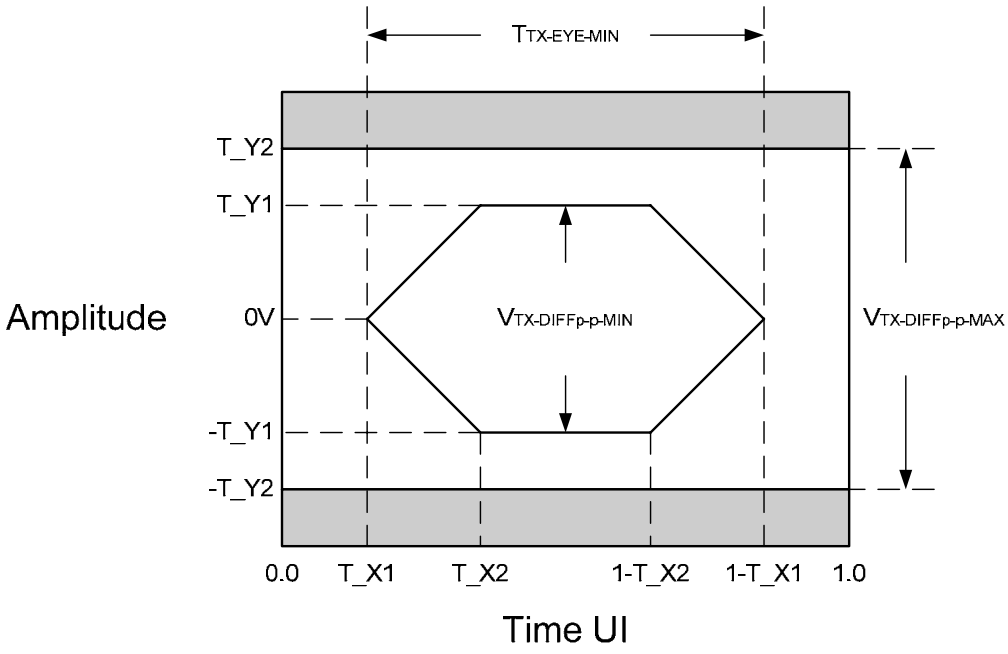


Figure 16. SGMII Differential Transmitter Eye Diagram

10.6.2. SGMII Differential Receiver Characteristics

Table 100. SGMII Differential Receiver Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Notes
UI	Unit Interval	799.76	800	800.24	ps	800ps ± 300ppm
R_X1	Eye Mask	-	-	0.3	UI	-
R_Y1	Eye Mask	100	-	-	mV	-
R_Y2	Eye Mask	-	-	1000	mV	-
$V_{RX-DIFFp-p}$	Input Differential Voltage	200	-	2000	mV	-
T_{RX-EYE}	Minimum RX Eye Width	0.4	-	-	UI	-
$T_{RX-JITTER}$	Input Jitter Tolerance	-	-	0.6	UI	$T_{RX-JITTER-MAX}$ = 1 - $T_{RX-EYE-MIN}$ = 0.6UI
R_{RX}	Differential Resistance	80	100	120	ohm	-

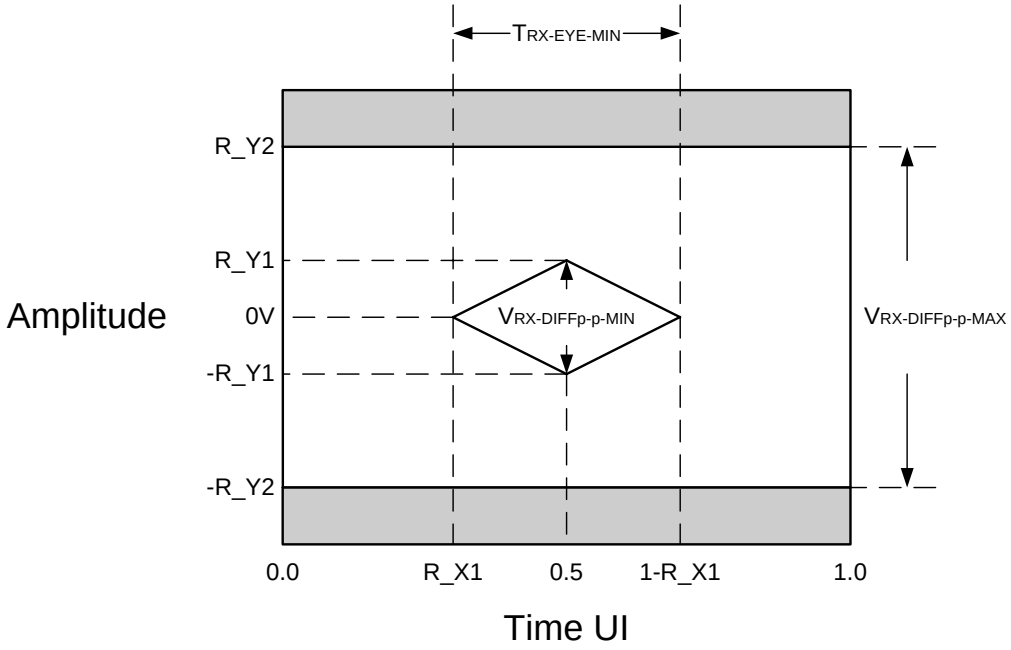


Figure 17. SGMII Differential Receiver Eye Diagram

10.7. 1000Base-X Characteristics

10.7.1. 1000Base-X Differential Transmitter Characteristics

Table 101. 1000Base-X Differential Transmitter Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Notes
UI	Unit Interval	799.76	800	800.24	ps	800ps ± 300ppm
T_X1	Eye Mask	-	-	0.15	UI	-
T_X2	Eye Mask	-	-	0.4	UI	-
T_Y1	Eye Mask	300	-	-	mV	-
T_Y2	Eye Mask	-	-	1000	mV	-
$V_{TX-OFFSET}$	Output Offset Voltage	800	1000	1200	mV	-
$V_{TX-DIFFp-p}$	Output Differential Voltage	600	1600	2000	mV	-
T_{TX-EYE}	Minimum TX Eye Width	0.7	-	-	UI	-
$T_{TX-JITTER}$	Output Jitter	-	-	0.3	UI	$T_{TX-JITTER-MAX}$ = 1 - $T_{TX-EYE-MIN}$ = 0.3UI
$T_{TX-RISE}$	Output Rise Time	0.125	-	0.25	UI	20% ~ 80%
$T_{TX-FALL}$	Output Fall Time	0.125	-	0.25	UI	20% ~ 80%
R_{TX}	Differential Resistance	80	100	120	ohm	-
C_{TX}	AC Coupling Capacitor	80	100	120	nF	-
L_{TX}	Transmit Length in PCB	-	-	10	inch	-

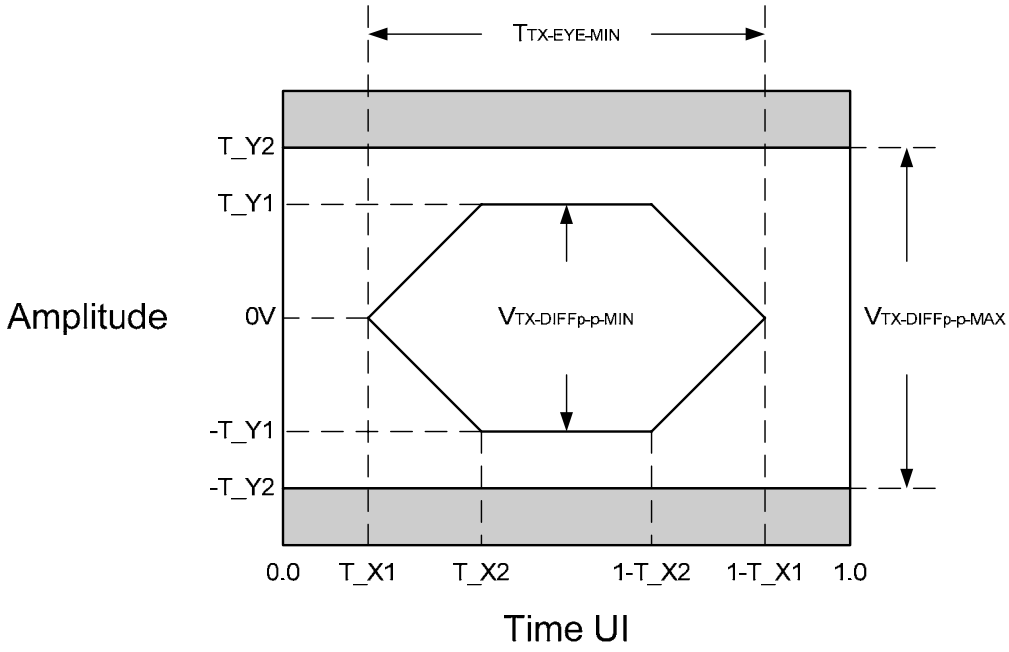


Figure 18. 1000Base-X Differential Transmitter Eye Diagram

10.7.2. 1000Base-X Differential Receiver Characteristics

Table 102. 1000Base-X Differential Receiver Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Notes
UI	Unit Interval	799.76	800	800.24	ps	800ps ± 300ppm
R_X1	Eye Mask	-	-	0.3	UI	-
R_Y1	Eye Mask	100	-	-	mV	-
R_Y2	Eye Mask	-	-	1000	mV	-
$V_{RX-DIFFp-p}$	Input Differential Voltage	200	-	2000	mV	-
T_{RX-EYE}	Minimum RX Eye Width	0.4	-	-	UI	-
$T_{RX-JITTER}$	Input Jitter Tolerance	-	-	0.6	UI	$T_{RX-JITTER-MAX}$ = 1 - $T_{RX-EYE-MIN}$ = 0.6UI
R_{RX}	Differential Resistance	80	100	120	ohm	-

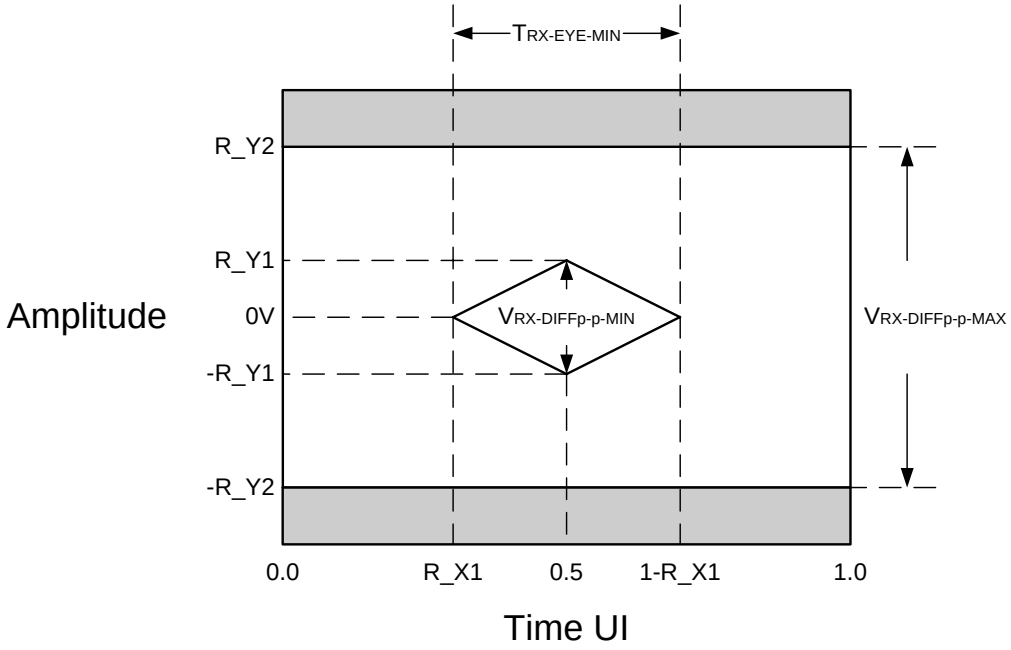


Figure 19. 1000Base-X Differential Receiver Eye Diagram

10.8. AC Characteristics

10.8.1. MDC/MDIO Timing

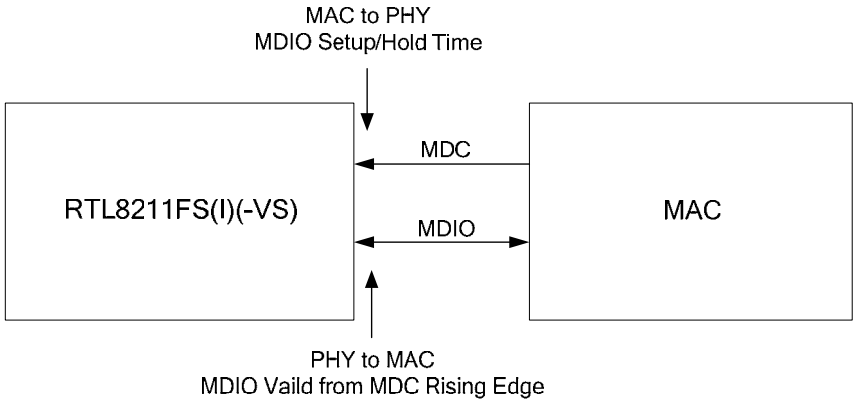


Figure 20. MDC/MDIO Setup, Hold Time, and Valid from MDC Rising Edge Time Definitions

MDC/MDIO Timing – Management Port

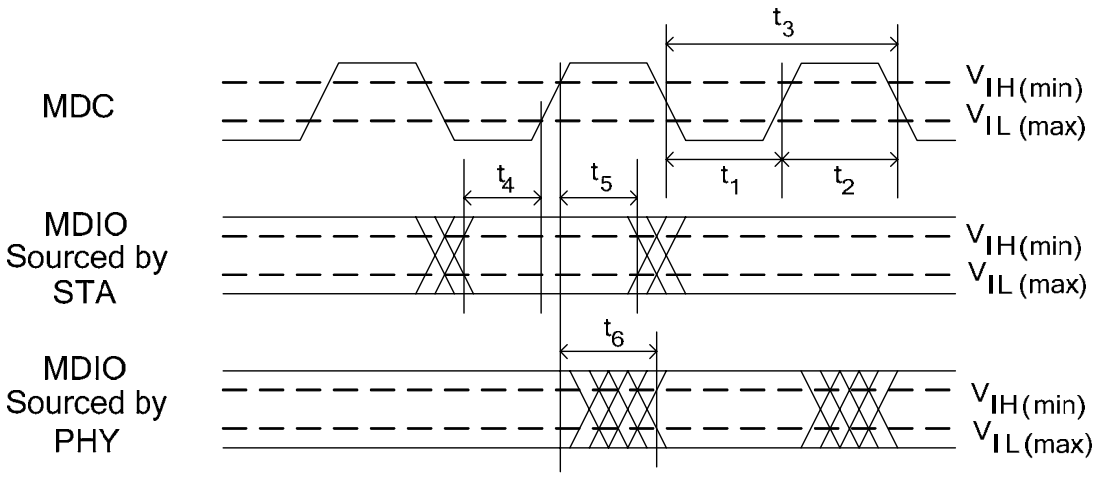


Figure 21. MDC/MDIO Management Timing Parameters

Table 103. MDC/MDIO Management Timing Parameters

Symbol	Description	Minimum	Maximum	Unit
t_1	MDC Low Pulse Width	32	-	ns
t_2	MDC High Pulse Width	32	-	ns
t_3	MDC Period	80	-	ns
t_4	MDIO Setup to MDC Rising Edge	10	-	ns
t_5	MDIO Hold Time from MDC Rising Edge	10	-	ns
t_6	MDIO Valid from MDC Rising Edge	0	300	ns

10.8.2. RGMII Timing Modes

Timing for this interface will be such that the clock and data are generated simultaneously by the source of the signals and therefore skew between the clock and data is critical to proper operation.

Figure 22 shows the effect of adding an additional delay to TXC by PC board (upper side) or by transmitter internally (lower side) when in RGMII mode.

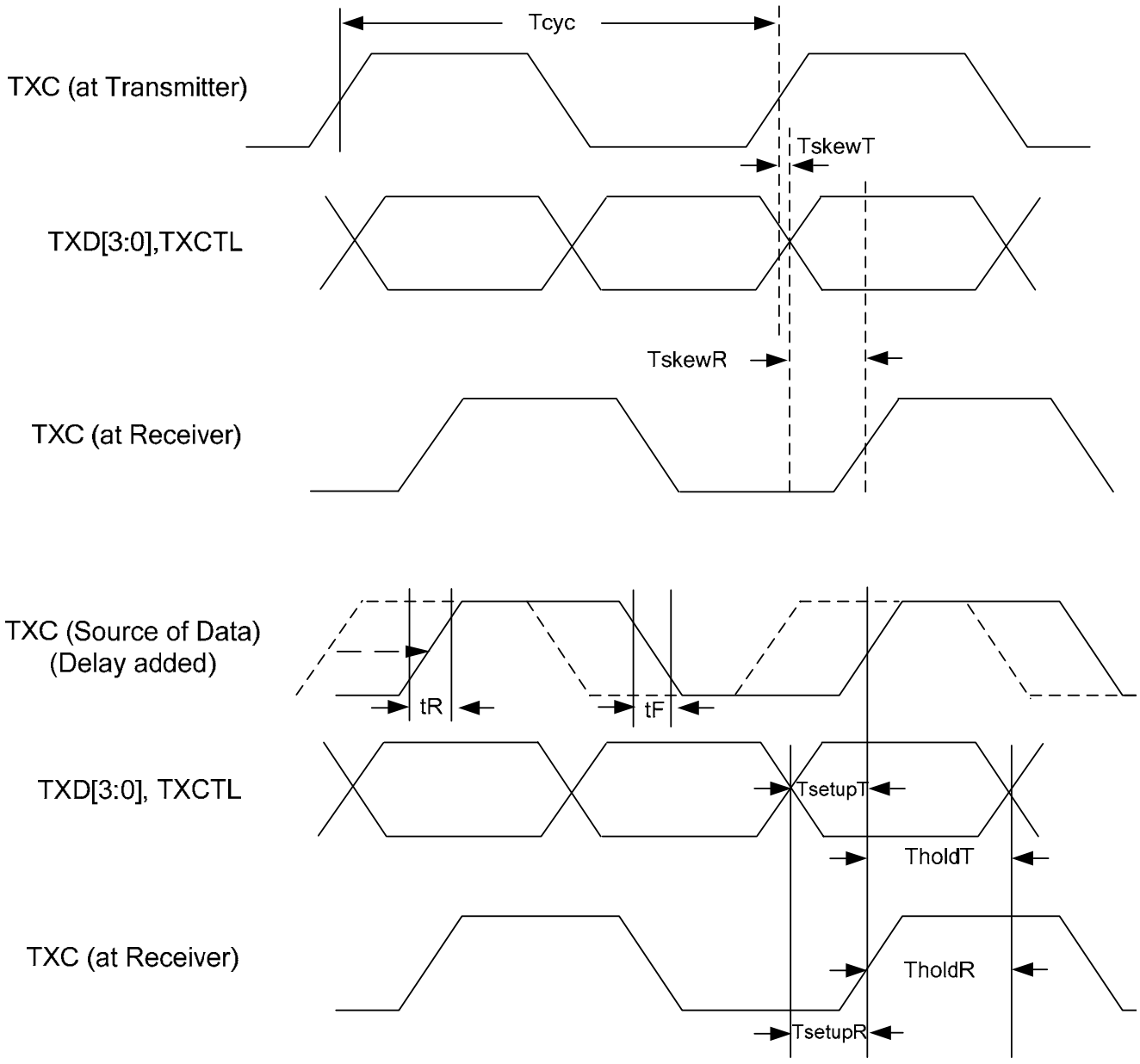


Figure 22. RGMII Timing Modes (For TXC)

Figure 23 shows the effect of adding an additional delay to RXC by PC board (upper side) or by transmitter internally (lower side) when in RGMII mode.

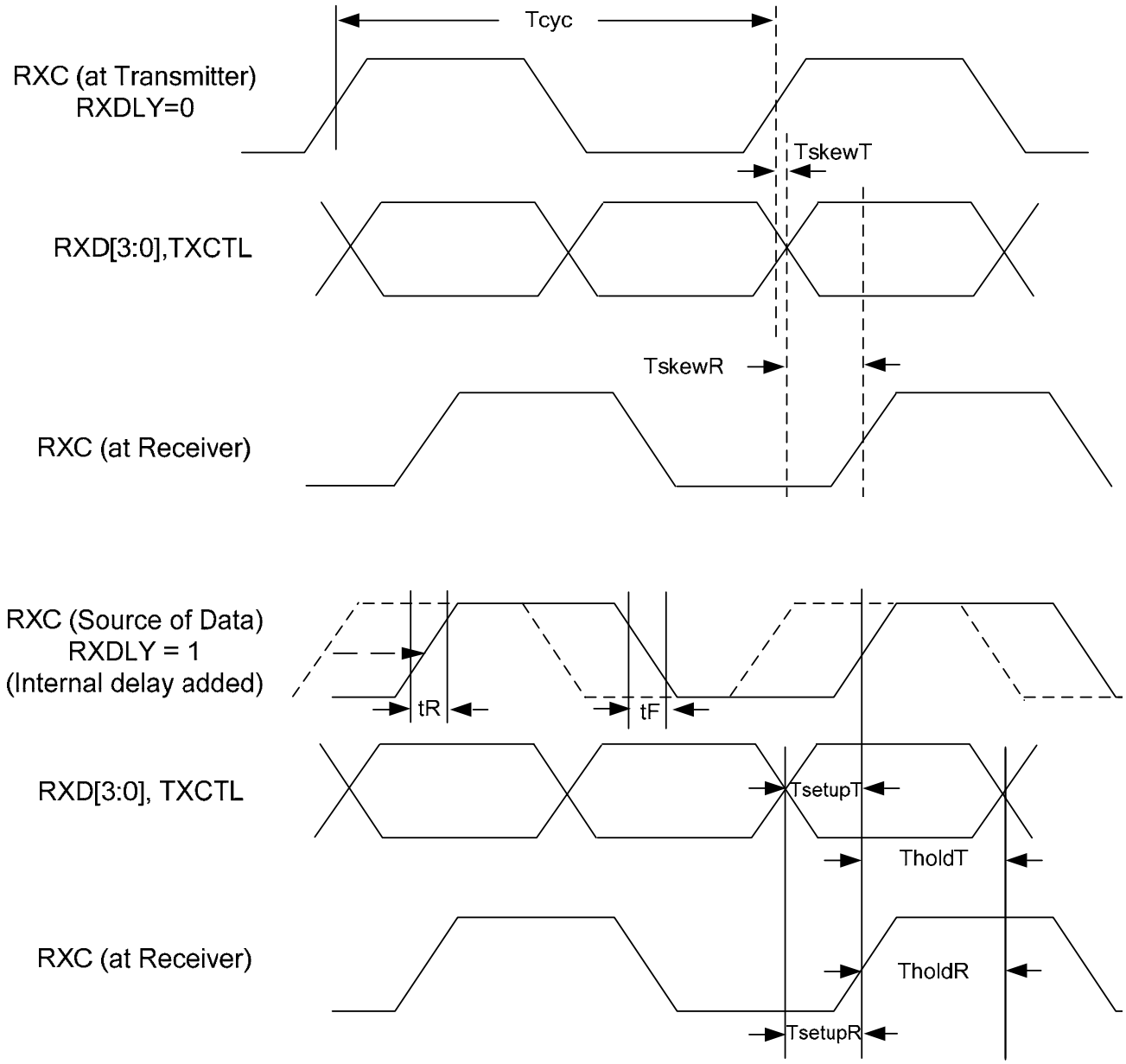


Figure 23. RGMII Timing Modes (For RXC)

Table 104. RGMII Timing Parameters

Symbol	Description	Min	Typical	Max	Units
Tcyc *	Clock Cycle Duration (1000Mbps)	7.2	8	8.8	ns
	Clock Cycle Duration (100Mbps)	36	40	44	ns
	Clock Cycle Duration (10Mbps)	360	400	440	ns
Duty_G	Duty Cycle for 1000	45	50	55	%
Duty_T	Duty Cycle for 10/100	40	50	60	%
tR	TXC/RXC Rise Time (20%~80%)	-	-	0.75	ns
tF	TXC/RXC Fall Time (20%~80%)	-	-	0.75	ns
TsetupT	Data to Clock Output Setup Time at transmitter (with delay integrated at transmitter)	1.2	2	-	ns
TholdT	Clock to Data Output Hold Time at transmitter (with delay integrated at transmitter)	1.2	2	-	ns
TsetupR	Data to Clock Input Setup Time at receiver (with delay integrated at transmitter)	1.0	2	-	ns
TholdR	Clock to Data Input Hold Time at receiver (with delay integrated at transmitter)	1.0	2	-	ns
TskewT **	Data to Clock Output Skew Time at transmitter (without delay integrated)	-0.5	0	0.5	ns
TskewR **	Data to Clock Input Skew Time at receiver (with PCB delay integrated) This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5ns and less than 2.0ns will be added to the associated clock signal.	1	1.8	2.6	ns

**Note: Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest speed transitioned between.*

***Note: For 10/100Mbps, the max value of Skew Time is unspecified.*

10.8.3. SGMII Timing Modes

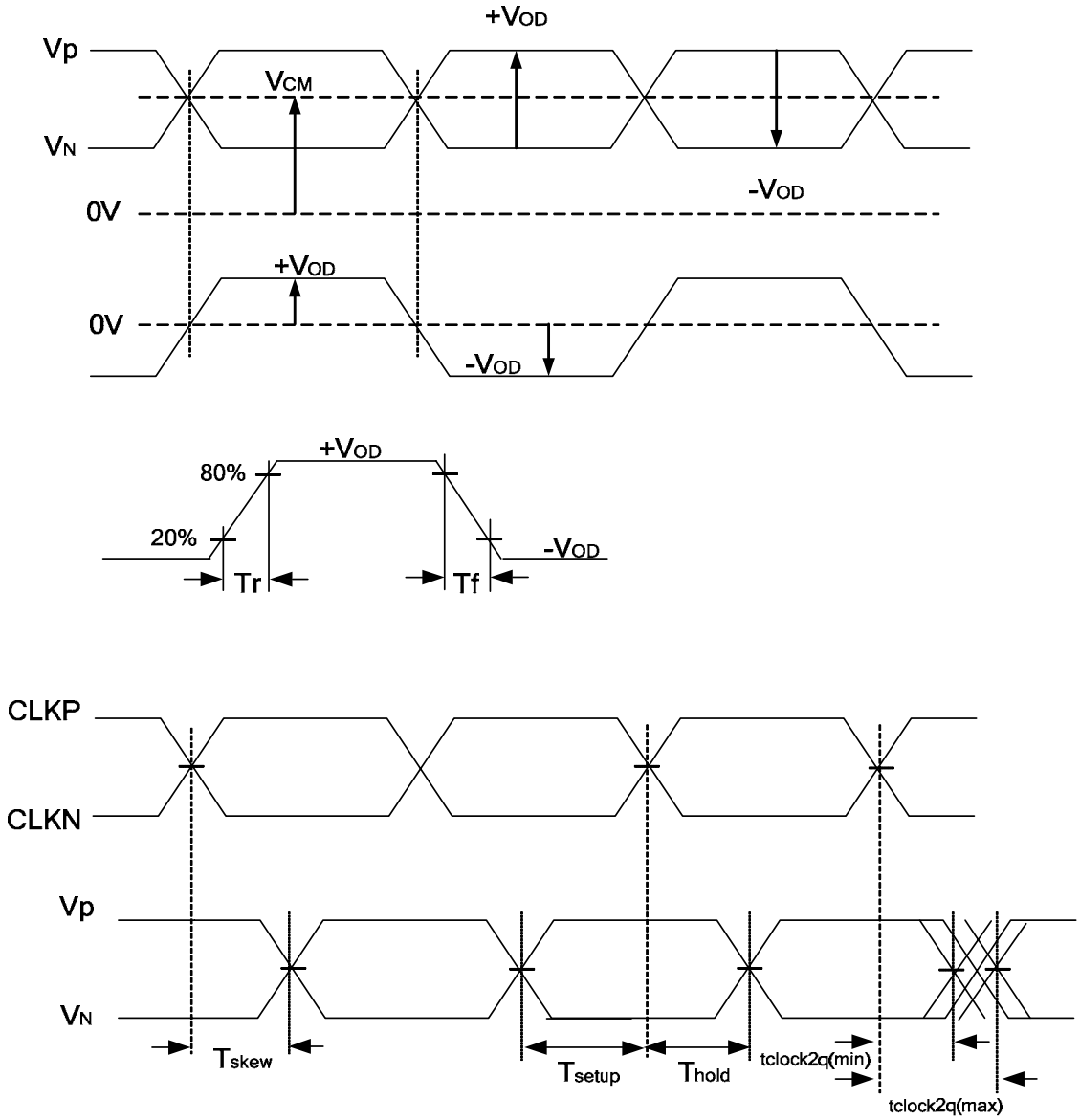


Figure 24. SGMII Timing Modes

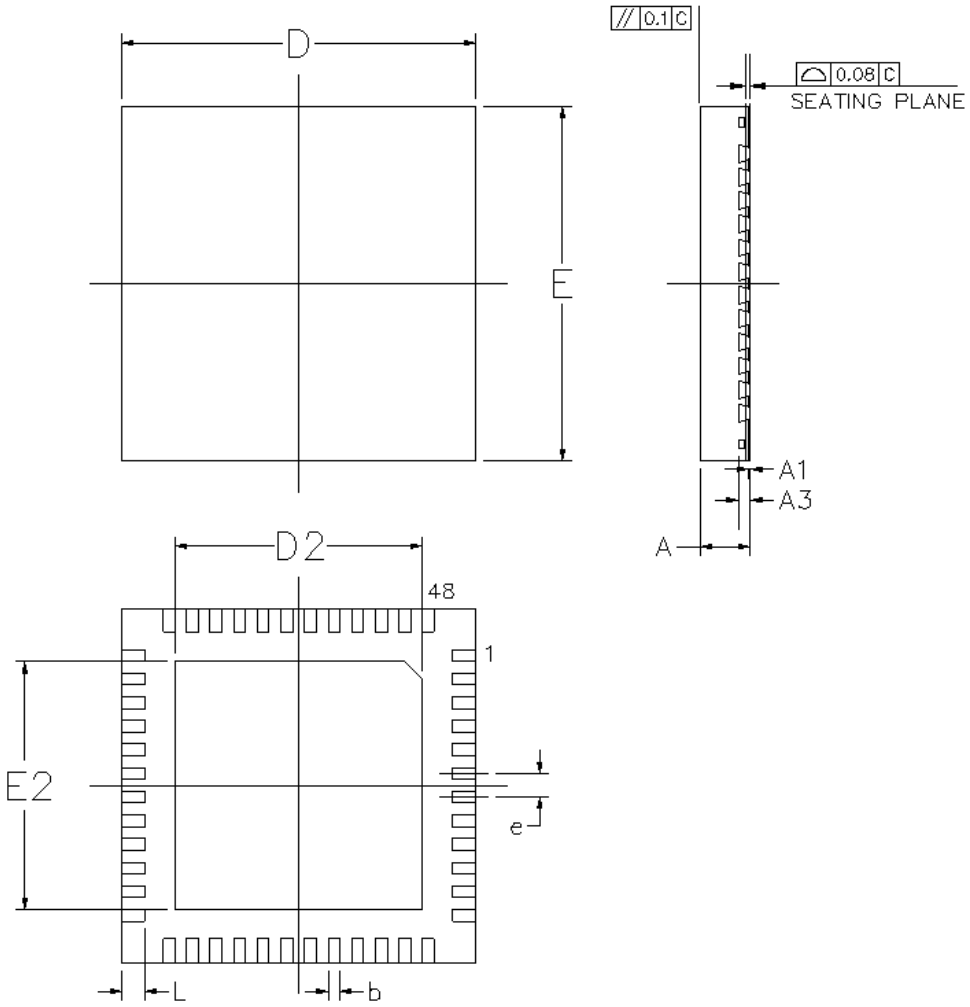
Table 105. Differential Transmitter Output AC Timing

Symbol	Parameter	Min	Typical	Max	Units	Note
clock	Clock Signal Duty Cycle @ 625MHz	48	-	52	%	-
Tf	V_{OD} Fall Time (20%~80%)	80	-	120	ps	-
Tr	V_{OD} Rise Time (20%~80%)	80	-	120	ps	-
T_{skew}	Skew between Two Members of a Differential Pair	-	-	15	ps	-
$t_{clock2q}$	Clock to Data Relationship: From either edge of the clock to valid data	250	-	550	ps	-
-	Effective Clock Period	-	800	-	ps	-
-	Cycle to Cycle Clock Jitter	-	-	100	ps	peak-to-peak
-	Imperfect Duty Cycle	-	-	30	ps	peak-to-peak
-	Data Dependent Skew	-	-	70	ps	peak-to-peak
-	Static Package Skew	-	-	100	ps	peak-to-peak
-	Remaining Window	500	-	-	ps	peak-to-peak

Table 106. Differential Receiver Input AC Timing

Symbol	Parameter	Min	Typical	Max	Units	Note
T_{setup}	Setup Time (20%~80%)	250	-	550	ps	-
T_{hold}	Hold Time (20%~80%)	250	-	550	ps	-
-	Driver Window	500	-	-	ps	peak-to-peak
-	Static Package Skew	100	-	-	ps	peak-to-peak
-	Remaining Window	200	-	-	ps	peak-to-peak

11. Mechanical Dimensions



11.1. Mechanical Dimensions Notes

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.75	0.85	1.00	0.030	0.034	0.039
A_1	0.00	0.02	0.05	0.000	0.001	0.002
A_3		0.20REF			0.008REF	
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E		6.00BSC			0.236BSC	
D2/E2	4.15	4.4	4.65	0.163	0.173	0.183
e		0.40BSC			0.016BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020

Note 1: CONTROLLING DIMENSION: MILLIMETER (mm).

Note 2: REFERENCE DOCUMENT: JEDEC MO-220.

12. Ordering Information

Table 107. Ordering Information

Part Number	Package	Status
RTL8211FS-CG	48-Pin QFN with 'Green' Package	MP
RTL8211FS-VS-CG	48-Pin QFN with 'Green' Package, supports Precision Time Protocol (PTP).	MP
RTL8211FSI-CG	48-Pin QFN with 'Green' Package. Industrial grade.	-
RTL8211FSI-VS-CG	48-Pin QFN with 'Green' Package, supports Precision Time Protocol (PTP). Industrial grade.	-

Note: See page 8 for package identification.

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