



REALTEK

RTL8213B-CG

**10/100/1000M Copper
to
100Base-FX/1000Base-X Fiber
Media Converter**

DRAFT DATASHEET
(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the hardware and software engineer's general information on the Realtek RTL8213B IC.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

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- If working on a prototyping board, use a soldering iron or station that is marked as ESD-safe
- Always disconnect the microcontroller from the prototyping board when it is being worked on

REVISION HISTORY

Revision	Release Date	Summary
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Table of Contents

1. GENERAL DESCRIPTION	1
2. FEATURES.....	3
3. SYSTEM APPLICATIONS.....	5
4. APPLICATION EXAMPLES.....	5
4.1. UNMANAGED MEDIA CONVERTER	5
5. BLOCK DIAGRAM.....	6
6. PIN ASSIGNMENTS	7
6.1. PACKAGE IDENTIFICATION	7
6.2. PIN ASSIGNMENTS TABLE	8
7. PIN DESCRIPTIONS	9
7.1. MEDIA DEPENDENT INTERFACE PINS.....	9
7.2. HIGH SPEED SERIAL INTERFACE PINS.....	9
7.3. GENERAL PURPOSE INTERFACES.....	9
7.4. LED PINS	9
7.5. CONFIGURATION STRAPPING PINS.....	10
7.6. MANAGEMENT INTERFACE PINS	11
7.7. MISCELLANEOUS PINS	11
7.8. EMBEDDED SWITCH REGULATOR PINS.....	12
7.9. POWER AND GND PINS	12
8. PHYSICAL LAYER FUNCTIONAL OVERVIEW	13
8.1. MDI INTERFACE	13
8.2. 1000BASE-T TRANSMIT FUNCTION	13
8.3. 1000BASE-T RECEIVE FUNCTION.....	13
8.4. 100BASE-TX TRANSMIT FUNCTION	13
8.5. 100BASE-TX RECEIVE FUNCTION.....	14
8.6. 10BASE-T TRANSMIT FUNCTION	14
8.7. 10BASE-T RECEIVE FUNCTION	14
8.8. AUTO-NEGOTIATION FOR UTP.....	14
8.9. Crossover DETECTION AND AUTO CORRECTION	15
8.10. POLARITY CORRECTION.....	15
9. GENERAL FUNCTION DESCRIPTIONS.....	16
9.1. RESET.....	16
9.1.1. <i>Hardware Reset</i>	16
9.1.2. <i>Software Reset</i>	16
9.2. IEEE 802.3X FULL DUPLEX FLOW CONTROL	17
9.3. HALF DUPLEX FLOW CONTROL	17
9.3.1. <i>Back-Pressure Mode</i>	17
9.4. SEARCH AND LEARNING	18
9.5. SVL AND IVL/SVL	18

9.6.	ILLEGAL FRAME FILTERING	18
9.7.	IEEE 802.3 RESERVED GROUP ADDRESSES FILTERING CONTROL.....	19
9.8.	BROADCAST/MULTICAST/UNKNOWN DA STORM CONTROL	20
9.9.	PORT SECURITY FUNCTION	20
9.10.	MIB COUNTERS.....	20
9.11.	PORT MIRRORING.....	20
9.12.	VLAN FUNCTION.....	21
9.12.1.	<i>Port-Based VLAN</i>	21
9.12.2.	<i>IEEE 802.1Q Tag-Based VLAN</i>	21
9.12.3.	<i>Protocol-Based VLAN</i>	21
9.13.	QoS FUNCTION.....	22
9.13.1.	<i>Input Bandwidth Control</i>	22
9.13.2.	<i>Priority Assignment</i>	22
9.13.3.	<i>Priority Queue Scheduling</i>	23
9.13.4.	<i>IEEE 802.1p/Q and DSCP Remarking</i>	23
9.13.5.	<i>ACL-Based Priority</i>	23
9.14.	IEEE 802.1X FUNCTION	24
9.14.1.	<i>Port-Based Access Control</i>	24
9.14.2.	<i>Authorized Port-Based Access Control</i>	24
9.14.3.	<i>Port-Based Access Control Direction</i>	24
9.14.4.	<i>MAC-Based Access Control</i>	24
9.14.5.	<i>MAC-Based Access Control Direction</i>	24
9.14.6.	<i>Optional Unauthorized Behavior</i>	24
9.15.	IEEE 802.1D FUNCTION.....	25
9.16.	REALTEK CABLE TEST (RTCT).....	25
9.17.	LED INDICATORS	26
9.18.	GREEN ETHERNET.....	28
9.18.1.	<i>Link-On and Cable Length Power Saving</i>	28
9.18.2.	<i>Link-Down Power Saving</i>	28
9.19.	REGULATOR.....	28
10.	INTERFACE DESCRIPTIONS	29
10.1.	MASTER I2C FOR EEPROM AUTO-LOAD	29
10.2.	REALTEK SLAVE I2C-LIKE INTERFACE FOR EXTERNAL CPU TO ACCESS THE RTL8213B.....	30
10.3.	SLAVE MII MANAGEMENT SMI INTERFACE FOR EXTERNAL CPU TO ACCESS RTL8213B	31
11.	ELECTRICAL CHARACTERISTICS.....	32
11.1.	ABSOLUTE MAXIMUM RATINGS.....	32
11.2.	RECOMMENDED OPERATING RANGE	32
11.3.	THERMAL CHARACTERISTICS	33
11.3.1.	<i>Assembly Description</i>	33
11.3.2.	<i>Material Properties</i>	33
11.3.3.	<i>Simulation Conditions</i>	33
11.3.4.	<i>Thermal Performance of QFN-56 on PCB Under Still Air Convection</i>	34
11.4.	DC CHARACTERISTICS.....	34
11.5.	SWITCH REGULATOR	34
11.6.	AC CHARACTERISTICS.....	35

11.6.1.	<i>Master I2C for EEPROM Auto-load Interface Timing Characteristics</i>	35
11.6.2.	<i>Slave I2C-like Mode Timing Characteristics</i>	36
11.6.3.	<i>Slave MII Management SMI for External CPU Access Interface Timing Characteristics</i>	37
11.6.4.	<i>SGMII/1000Base-X Characteristics</i>	38
11.6.5.	<i>Power and Reset Characteristics</i>	40
12.	MECHANICAL DIMENSIONS	41
13.	ORDERING INFORMATION	42

List of Tables

TABLE 1. PIN ASSIGNMENTS TABLE	8
TABLE 2. MEDIA DEPENDENT INTERFACE PINS	9
TABLE 3. HIGH SPEED SERIAL INTERFACE PINS	9
TABLE 4. GENERAL PURPOSE INTERFACES PINS	9
TABLE 5. LED PINS	10
TABLE 6. CONFIGURATION STRAPPING PINS	10
TABLE 7. MANAGEMENT INTERFACE PINS	11
TABLE 8. MISCELLANEOUS PINS	11
TABLE 9. EMBEDDED SWITCH REGULATOR PINS	12
TABLE 10. POWER AND GND PINS	12
TABLE 11. MEDIA DEPENDENT INTERFACE PIN MAPPING	15
TABLE 12. RESERVED MULTICAST ADDRESS CONFIGURATION TABLE	19
TABLE 13. LED DEFINITIONS	26
TABLE 14. SLAVE MII MANAGEMENT SMI ACCESS FORMAT	31
TABLE 15. ABSOLUTE MAXIMUM RATINGS	32
TABLE 16. RECOMMENDED OPERATING RANGE	32
TABLE 17. ASSEMBLY DESCRIPTION	33
TABLE 18. MATERIAL PROPERTIES	33
TABLE 19. SIMULATION CONDITIONS	33
TABLE 20. THERMAL PERFORMANCE OF QFN-56 ON PCB UNDER STILL AIR CONVECTION	34
TABLE 21. DC CHARACTERISTICS	34
TABLE 22. SWITCH REGULATOR	34
TABLE 23. MASTER I2C FOR EEPROM AUTO-LOAD TIMING CHARACTERISTICS	35
TABLE 24. SLAVE I2C-LIKE MODE TIMING CHARACTERISTICS	36
TABLE 25. MDIO TIMING CHARACTERISTICS AND REQUIREMENT	37
TABLE 26. SGMII/1000BASE-X DIFFERENTIAL TRANSMITTER CHARACTERISTICS	38
TABLE 27. SGMII/1000BASE-X DIFFERENTIAL RECEIVER CHARACTERISTICS	39
TABLE 28. POWER AND RESET CHARACTERISTICS	40
TABLE 29. ORDERING INFORMATION	42

List of Figures

FIGURE 1. UNMANAGED MEDIA CONVERTER.....	5
FIGURE 2. BLOCK DIAGRAM	6
FIGURE 3. PIN ASSIGNMENTS (QFN-40).....	7
FIGURE 4. CONCEPTUAL EXAMPLE OF POLARITY CORRECTION.....	15
FIGURE 5. PROTOCOL-BASED VLAN FRAME FORMAT AND FLOW CHART.....	22
FIGURE 6. PULL-UP AND PULL-DOWN OF LED PINS FOR SINGLE-COLOR LED.....	27
FIGURE 7. PULL-UP AND PULL-DOWN OF LED PINS FOR BI-COLOR LED.....	27
FIGURE 8. SMI START AND STOP COMMAND.....	29
FIGURE 9. MASTER I2C FOR EEPROM AUTO-LOAD INTERFACE CONNECTION EXAMPLE.....	29
FIGURE 10. 8-BIT EEPROM SEQUENTIAL READ	29
FIGURE 11. REALTEK SLAVE I2C-LIKE FOR EXTERNAL CPU ACCESS INTERFACE CONNECTION EXAMPLE.....	30
FIGURE 12. REALTEK SLAVE I2C-LIKE INTERFACE WRITE COMMAND.....	30
FIGURE 13. REALTEK SLAVE I2C-LIKE INTERFACE READ COMMAND.....	30
FIGURE 14. SLAVE MII MANAGEMENT SMI INTERFACE CONNECTION EXAMPLE.....	31
FIGURE 15. MASTER I2C FOR EEPROM AUTO-LOAD TIMING CHARACTERISTICS.....	35
FIGURE 16. SCK/SDA POWER ON TIMING	35
FIGURE 17. SLAVE I2C-LIKE MODE TIMING CHARACTERISTICS.....	36
FIGURE 18. MDIO SOURCED BY THE MASTER	37
FIGURE 19. MDIO SOURCED BY THE RTL8213B (SLAVE)	37
FIGURE 20. SGMII/1000BASE-X DIFFERENTIAL TRANSMITTER EYE DIAGRAM.....	38
FIGURE 21. SGMII/1000BASE-X DIFFERENTIAL RECEIVER EYE DIAGRAM	39
FIGURE 22. POWER AND RESET CHARACTERISTICS.....	40

1. General Description

The RTL8213B-CG is a QFN40, high-performance media converter featuring low-power integrated 1-port Giga-PHY that support 1000Base-T, 100Base-TX, and 10Base-T.

For specific applications, the RTL8213B supports one SerDes interface that could be configured as a SGMII/1000Base-X/100FX interface. The RTL8213B integrates a SRAM for packet buffering, non-blocking switch fabric, and internal register management into a single CMOS device. Only a 25MHz crystal is required; an optional EEPROM is offered for internal register configuration.

The embedded packet storage SRAM in the RTL8213B features superior memory management technology to efficiently utilize memory space. The RTL8213B integrates a 2048-entry look-up table with a 4-way XOR Hashing algorithm for address searching and learning. The table provides read/write access from the Slave I2C-like serial Interface, or Slave Media Independent Interface Management (MIIM) Interface. Each of the entries can be configured as a static entry. Normal entry aging time is between 200 and 400 seconds. Sixteen Filtering Databases are used to provide Independent VLAN Learning and Shared VLAN Learning (IVL/SVL) functions.

The Extension GMAC1 of the RTL8213B implements a 1000Base-X/100Base-FX interface.

The RTL8213B supports standard 802.3x flow control frames for full duplex, and optional backpressure for half duplex. It determines when to invoke the flow control mechanism by checking the availability of system resources, including the packet buffers and transmitting queues. The RTL8213B supports broadcast/multicast output dropping, and will forward broadcast/multicast packets to non-blocked ports only. For IP multicast applications, the RTL8213B can forward IPv4 IGMPv1/v2/v3 and IPv6 MLDv1/v2 snooping protocol packets.

In order to support flexible traffic classification, the RTL8213B supports 48-entry ACL rule check and multiple actions options. Each port can optionally enable or disable the ACL rule check function. The ACL rule key can be based on packet physical port, Layer2, Layer3, and Layer4 information. When an ACL rule matches, the action taken is configurable to Drop/Permit/Redirect/Mirror, change priority value in 802.1q/Q tag, force output tag format and rate policing. The rate policing mechanism supports from 8Kbps to 1Gbps (in 8Kbps steps).

In Bridge operation the RTL8213B supports 16 sets of port configurations: disable, block, learning, and forwarding for Spanning Tree Protocol and Multiple Spanning Tree Protocol. To meet security and management application requirements, the RTL8213B supports IEEE 802.1x Port-based/MAC-based Access Control. A 1-set Port Mirroring function is configured to mirror traffic (RX, TX, or both) appearing on one of the switch's ports. Support is provided on each port for multiple RFC MIB Counters, for easy debug and diagnostics.

To improve real-time and multimedia networking applications, the RTL8213B supports eight priority assignments for each received packet. These are based on (1) Port-based priority; (2) 802.1p/Q VLAN tag priority; (3) DSCP field in IPv4/IPv6 header; and (4) ACL-assigned priority. Each output port supports a weighted ratio of eight priority queues to fit bandwidth requirements in different applications. The input bandwidth control function helps limit per-port traffic utilization. There is one leaky bucket for average packet rate control for each queue of all ports. Queue scheduling algorithm can use Strict Priority (SP) or Weighted Fair Queue (WFQ) or Weighted Round Robin (WRR) or mixed.

The RTL8213B provides a 4096-entry VLAN table for 802.1Q port-based, tag-based, and protocol-based VLAN operation to separate logical connectivity from physical connectivity. The RTL8213B supports four Protocol-based VLAN configurations that can optionally select EtherType, LLC, and RFC1042 as the search key. Each port may be set to any topology via EEPROM upon reset, or Slave I2C-like serial Interface, or Slave Media Independent Interface Management (MIIM) Interface after reset.

2. Features

- Embedded single-port 10/100/1000Base-T PHY
- Each port supports full duplex 10/100/1000M connectivity (half duplex only supported in 10/100M mode)
- Extra Interface (Extension GMAC1) supports
 - ◆ SGMII (1.25Gbps) Interface
 - ◆ 1000Base-X Interface
 - ◆ 100FX Interface
- Full-duplex and half-duplex operation with IEEE 802.3x flow control and backpressure
- Supports 9216-byte jumbo packet length forwarding at wire speed
- Realtek Cable Test (RTCT) function
- Supports 48-entry ACL Rules
 - ◆ Search keys support physical port, Layer2, Layer3, and Layer4 information
 - ◆ Actions include mirror, redirect, dropping, priority adjustment, traffic policing, CVLAN decision, and SVLAN assignment
 - ◆ Supports five types of user defined ACL rule format for 48 ACL rules
 - ◆ Optional per-port enable/disable of ACL function
 - ◆ Optional setting of per-port action to take when ACL mismatch
- Supports IEEE 802.1Q VLAN
 - ◆ Supports 4096 VLANs and 32 Extra Enhanced VLANs
 - ◆ Supports Un-tag definition in each VLAN
 - ◆ Supports VLAN policing and VLAN forwarding decision
 - ◆ Port-based, Tag-based, and Protocol-based VLAN
 - ◆ Up to 4 Protocol-based VLAN entries
 - ◆ Per-port and per-VLAN egress VLAN tagging and un-tagging
- Supports IVL, SVL, and IVL/SVL
- ◆ 2048-entry MAC address table with 4-way hash algorithm
- ◆ Up to 2048-entry L2/L3 Filtering Database
- ◆ Per-port MAC learning limitation
- ◆ System base MAC learning limitation
- Supports Spanning Tree Port Behavior configuration
 - ◆ IEEE 802.1w Rapid Spanning Tree
 - ◆ IEEE 802.1s Multiple Spanning Tree with up to 16 Spanning Tree instances
- Supports IEEE 802.1x Access Control Protocol
 - ◆ Port-Based Access Control
 - ◆ MAC-Based Access Control
- Supports Auto protection from Denial-of-Service attacks
- Supports trap IGMP/MLD packets to external CPU
- Supports Quality of Service (QoS)
 - ◆ Supports per port Input Bandwidth Control
 - ◆ Traffic classification based on IEEE 802.1p/Q priority definition, physical Port, IP DSCP field, ACL definition, VLAN based priority, MAC based priority and SVLAN based priority
 - ◆ Eight Priority Queues per port
 - ◆ Per queue flow control
 - ◆ Min-Max Scheduling
 - ◆ Strict Priority and Weighted Fair Queue (WFQ), Weighted Round Robin (WRR) packet scheduling
 - ◆ One leaky bucket to constrain the average packet rate of each queue
- Supports rate limiting (12 shared meters, with 8kbps granulation)
- Supports RFC MIB Counter
 - ◆ MIB-II (RFC 1213)
 - ◆ Ethernet-Like MIB (RFC 3635)
 - ◆ Interface Group MIB (RFC 2863)

- ◆ RMON (RFC 2819)
- ◆ Bridge MIB (RFC 1493)
- ◆ Bridge MIB Extension (RFC 2674)
- Supports Stacking VLAN and Port Isolation with eight Enhanced Filtering Databases
- Supports IEEE 802.1ad Stacking VLAN
 - ◆ Supports 64 SVLANs
 - ◆ Supports MAC-based 1:N VLAN
- Supports Port Mirror function for one monitor port for multiple mirroring ports
- Security Filtering
 - ◆ Disable learning for each port
 - ◆ Disable learning-table aging for each port
 - ◆ Drop unknown DA for each port
- Broadcast/Multicast/Unknown DA storm control
 - protects system from attack by hackers
- Supports Realtek Green Ethernet features
 - ◆ Link-On Cable Length Power Saving
 - ◆ Link-Down Power Saving
- Port 3 supports 3 parallel LED outputs
- Port 6 supports 2 parallel LED outputs
- Supports Slave I2C-like interface or Slave MII Management interface to access configuration register
- Supports 2K-byte EEPROM space for configuration
- Build in 3.3V to 1.1V switch regulator with power MOS
- 25MHz crystal or 3.3V OSC input
- 5x5 QFN 40-pin package

3. System Applications

- Unmanaged Media converter

4. Application Examples

4.1. Unmanaged Media Converter

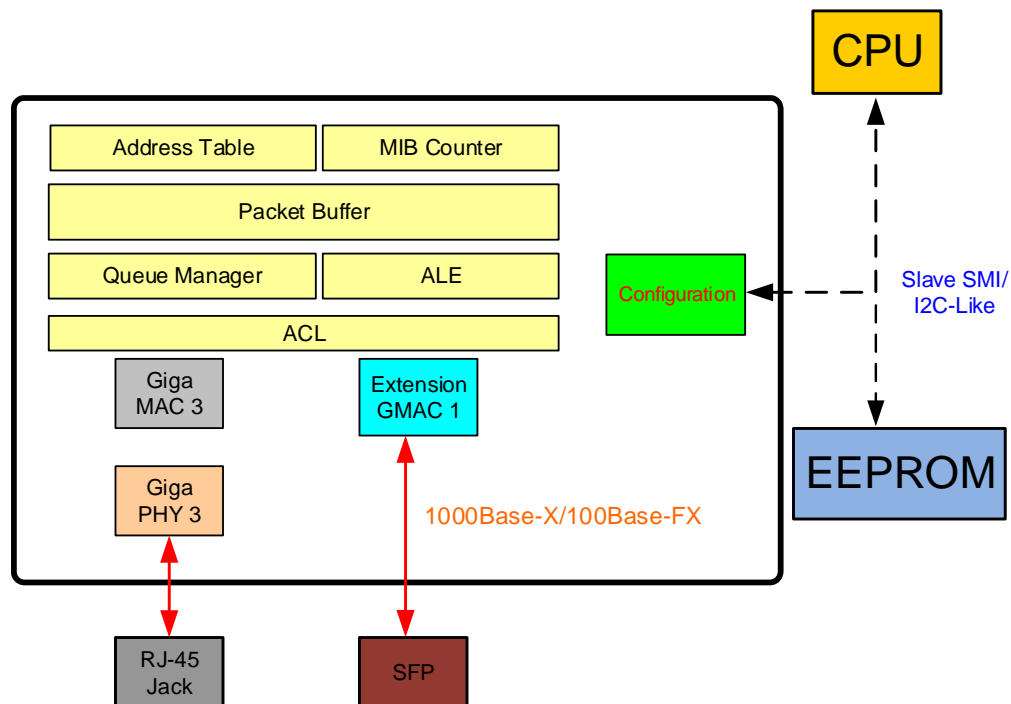


Figure 1. Unmanaged Media Converter

5. Block Diagram

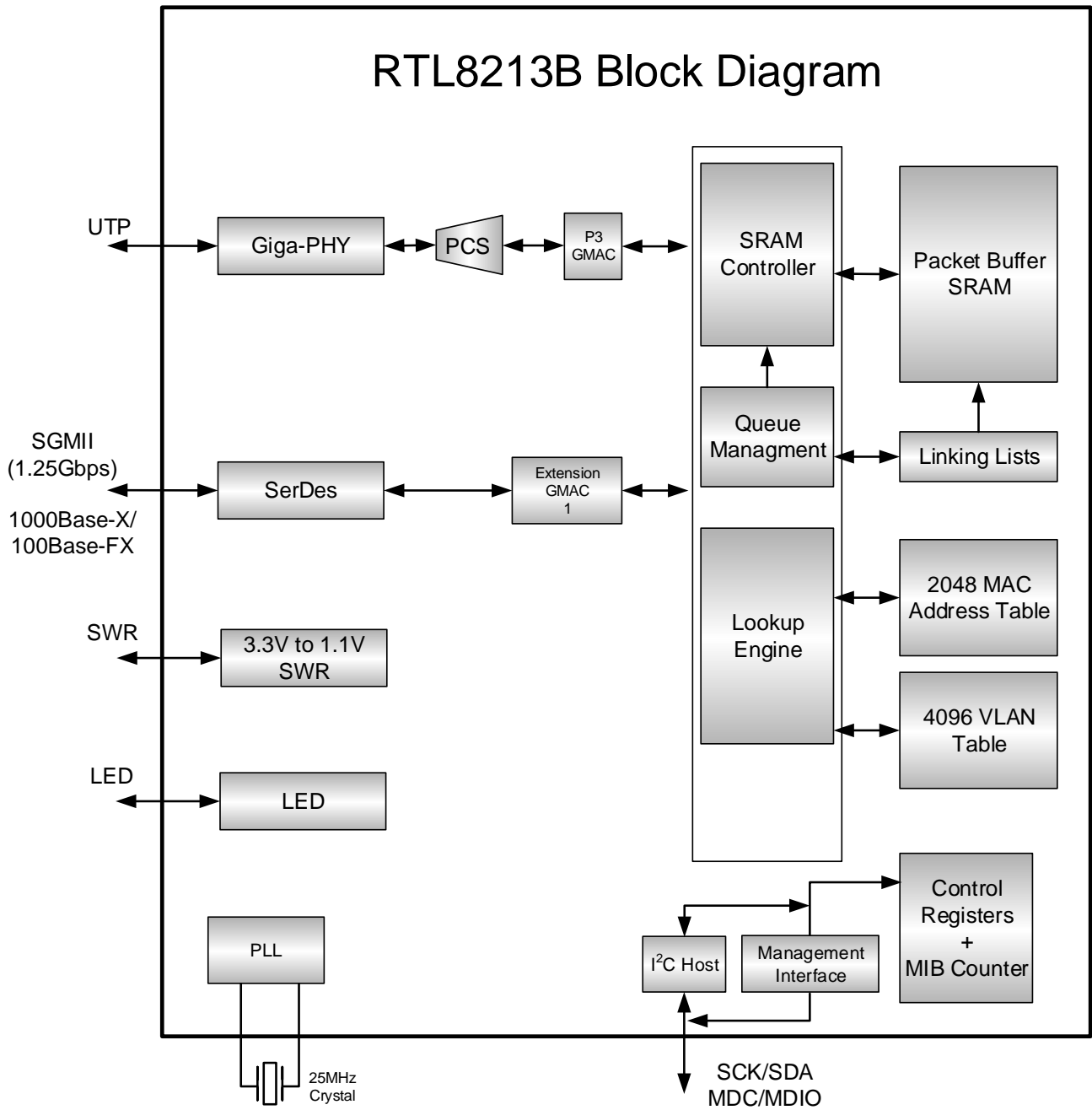


Figure 2. Block Diagram

6. Pin Assignments

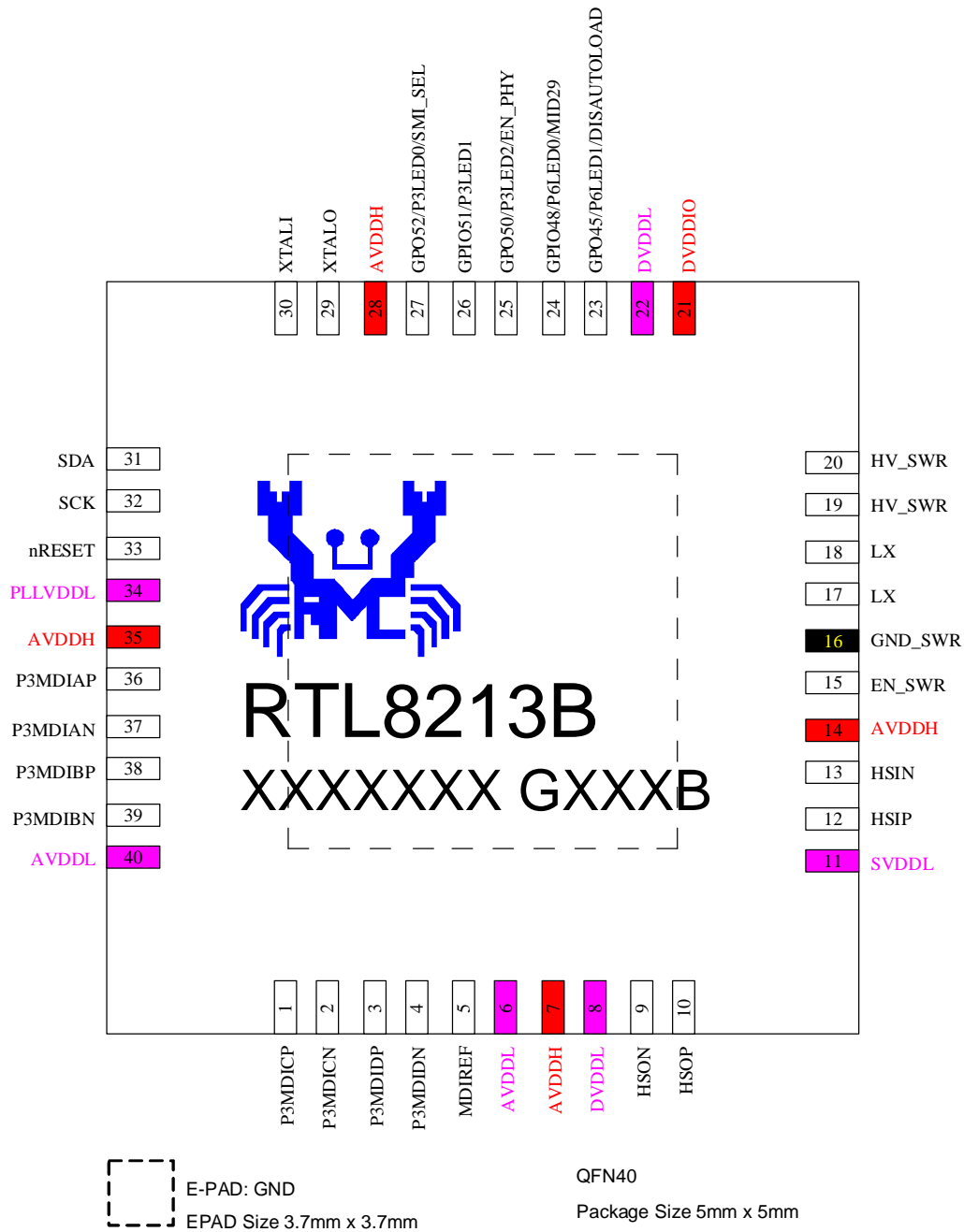


Figure 3. Pin Assignments (QFN-40)

6.1. Package Identification

Green package is indicated by the 'G' in GXXX (Figure 3).

6.2. Pin Assignments Table

Upon Reset: Defined as a short time after the end of a hardware reset.

After Reset: Defined as the time after the specified 'Upon Reset' time.

I: Input Pin

AI: Analog Input Pin

O: Output Pin

AO: Analog Output Pin

I/O: Bi-Directional Input/Output Pin

AI/O: Analog Bi-Directional Input/Output Pin

P: Digital Power Pin

AP: Analog Power Pin

G: Digital Ground Pin

AG: Analog Ground Pin

I_{PU}: Input Pin With Pull-Up Resistor;
(Typical Value = 75K Ohm)

O_{PU}: Output Pin With Pull-Up Resistor;
(Typical Value = 75K Ohm)

Table 1. Pin Assignments Table

Name	Pin No.	Type
P3MDICP	1	AI/O
P3MDICN	2	AI/O
P3MDIDP	3	AI/O
P3MDIDN	4	AI/O
MDIREF	5	AO
AVDDL	6	AP
AVDDH	7	AP
DVDDL	8	P
HSOP	9	AO
HSOP	10	AO
SVDDL	11	AP
HSIP	12	AI
HSIN	13	AI
AVDDH	14	AP
EN_SWR	15	AI
GND_SWR	16	AG
LX	17	AO
LX	18	AO
HV_SWR	19	AP
HV_SWR	20	AP

Name	Pin No.	Type
DVDDIO	21	P
DVDDL	22	P
GPO45/P6LED1/DISAUTOLOAD	23	I/O _{PU}
GPO48/P6LED0/MID29	24	I/O _{PU}
GPO50/P3LED2/EN_PHY	25	I/O _{PU}
GPIO51/P3LED1	26	I/O _{PU}
GPO52/P3LED0 /SMI_SEL	27	I/O _{PU}
AVDDH	28	AP
XTALO	29	AO
XTALI	30	AI
SDA/MDIO	31	I/O
SCK/MDC	32	I/O
nRESET	33	I _{PU}
PLLVDL	34	AP
AVDDH	35	AP
P3MDIAP	36	AI/O
P3MDIAN	37	AI/O
P3MDIBP	38	AI/O
P3MDIBN	39	AI/O
AVDDL	40	AP

7. Pin Descriptions

7.1. Media Dependent Interface Pins

Table 2. Media Dependent Interface Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
P3MDIAP/N	36	AI/O	10	Port 3 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-TX and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100-ohm termination resistor.
	37			
P3MDIBP/N	38			
	39			
P3MDICP/N	1			
	2			
P3MDIDP/N	3			
	4			

7.2. High Speed Serial Interface Pins

Table 3. High Speed Serial Interface Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
HSOP/N	10 9	AO	10	High Speed Serial Output Pins: 125MHz/1.25GHz Differential serial interface to transmit data. Keep floating when unused.
HSIP/N	12 13	AI	10	High Speed Serial Input Pins: 125MHz/1.25GHz Differential serial interface to receive data. Keep floating when unused.

7.3. General Purpose Interfaces

Table 4. General Purpose Interfaces Pins

Pin No.	GPIO	Other Function	Configuration Strapping
23	GPO45	P6LED1	DISAUTOLOAD
24	GPO48	P6LED0	MID29
25	GPO50	P3LED2	EN_PHY
26	GPIO51	P3LED1	-
27	GPO52	P3LED0	SMI_SEL

7.4. LED Pins

The RTL8213B LED Pins work in parallel mode. LED0, LED1, LED2 of Port 3 and LED0, LED1 of Port 6 indicate information that can be defined via register or EEPROM.

When the LED pin is pulled low, the LED output polarity will be high active. When the LED pin is pulled high, the LED output polarity will change from high active to low active. See section 9.17 LED Indicators, page 26 for more details.

Table 5. LED Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
P3LED2/ GPO50/ EN_PHY	25	I/OPU	-	P3LED2 Output Signal. P3LED2 indicates information is defined by register or EEPROM. See section 9.17 LED Indicators, page 26 for more details.
P3LED1/ GPIO51	26	I/OPU	-	P3LED1 Output Signal. P3LED1 indicates information is defined by register or EEPROM. See section 9.17 LED Indicators, page 26 for more details.
P3LED0/ GPO52/ SMI_SEL	27	I/OPU	-	P3LED0 Output Signal. P3LED0 indicates information is defined by register or EEPROM. See section 9.17 LED Indicators, page 26 for more details.
P6LED1/ GPO45/ DISAUTOLOAD	23	I/OPU	-	P6LED1 Output Signal. P6LED1 indicates information is defined by register or EEPROM. See section 9.17 LED Indicators, page 26 for more details.
P6LED0/ GPO48/ MID29	24	I/OPU	-	P6LED0 Output Signal. P6LED0 indicates information is defined by register or EEPROM. See section 9.17 LED Indicators, page 26 for more details.

7.5. Configuration Strapping Pins

Table 6. Configuration Strapping Pins

Pin Name	Pin No.	Type	Description
DISAUTOLOAD/ GPO45/ P6LED1	23	I/OPU	Disable EEPROM Autoload. Pull Up: Disable EEPROM autoload Pull Down: Enable EEPROM autoload <i>Note 1: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.</i> <i>When this pin is pulled low, the LED output polarity will be high active. When this pin is pulled high, the LED output polarity will change from high active to low active.</i> <i>See section 9.17 LED Indicators, page 26 for more details.</i>
MID29/ GPO48/ P6LED0	24	I/OPU	Slave SMI (MDC/MDIO) Device Address. Pull Up: Slave SMI (MDC/MDIO) Device Address is d'29 Pull Down: Slave SMI (MDC/MDIO) Device Address is 0 <i>Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.</i>
EN_PHY/ GPO50/ P3LED2	25	I/OPU	Enable Embedded PHY. Pull Up: Enable embedded PHY Pull Down: Disable embedded PHY <i>Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.</i> <i>When this pin is pulled low, the LED output polarity will be high active. When this pin is pulled high, the LED output polarity will change from high active to low active.</i> <i>See section 9.17 LED Indicators, page 26 for more details.</i>

Pin Name	Pin No.	Type	Description
SMI_SEL/ GPO52/ P3LED0	27	I/OPU	Slave I2C-like/Slave MII Management Interface Selection. Pull Up: Slave I ² C-like interface Pull Down: Slave MII Management interface <i>Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.</i> <i>When this pin is pulled low, the LED output polarity will be high active. When this pin is pulled high, the LED output polarity will change from high active to low active.</i> <i>See section 9.17 LED Indicators, page 26 for more details.</i>

7.6. Management Interface Pins

Table 7. Management Interface Pins

Pin Name	Pin No.	Type	Description
SCK/ MDC	32	I/O	Master I2C Interface Clock for EEPROM auto-download. Slave I2C Interface Clock for external CPU to access DUT. Slave MII Management Interface Clock (selected via the hardware strapping SMI_SEL).
SDA/ MDIO	31	I/O	Master I2C Interface Data for EEPROM auto-download. Slave I2C Interface Data for external CPU to access DUT. Slave MII Management Interface Data (selected via the hardware strapping SMI_SEL).

7.7. Miscellaneous Pins

Table 8. Miscellaneous Pins

Pin Name	Pin No.	Type	Description
MDIREF	5	AO	Reference Resistor. A 2.49K ohm (1%) resistor must be connected between MDIREF and GND.
GPO45/ P6LED1/ DISAUTOLOAD	23	I/OPU	General Purpose Output Interface IO45.
GPO48/ P6LED0/ MID29	24	I/OPU	General Purpose Output Interface IO48.
GPO50/ P3LED2/ EN_PHY	25	I/OPU	General Purpose Output Interface IO50.
GPIO51/ P3LED1	26	I/OPU	General Purpose Input/Output Interface IO51.
GPO52/ P3LED0/ SMI_SEL	27	I/OPU	General Purpose Output Interface IO52.
XTALO	29	AO	25MHz Crystal Clock Output Pin.

Pin Name	Pin No.	Type	Description
XTALI	30	AI	25MHz Crystal Clock Input Pin. 25MHz +/-50ppm tolerance crystal reference. When using a crystal, connect a loading capacitor between crystal pin and ground. When either using an oscillator or driving an external 25MHz clock from another device, XTALO should kept floating.
nRESET	33	IPU	System Reset Input Pin. When low active will reset the RTL8213B-CG.

7.8. Embedded Switch Regulator Pins

Table 9. Embedded Switch Regulator Pins

Pin Name	Pin No.	Type	Description
EN_SWR	15	AI	Enable embedded switch regulator. Pull Up: Enable embedded switch regulator. Pull Down: Disable embedded switch regulator. Note: pulled high or low via an external 4.7k ohm resistor to enable or disable embedded switch regulator.
GND_SWR	16	AG	Regulator Ground.
LX	17, 18	AO	Regulator output. It should connect to the external inductor.
HV_SWR	19, 20	AP	Regulator Power Supply Input.

7.9. Power and GND Pins

Table 10. Power and GND Pins

Pin Name	Pin No.	Type	Description
DVDDIO	21	P	Digital I/O High Voltage Power for LED, Management Interface, and nRESET.
DVDDL	8, 22	P	Digital Low Voltage Power.
AVDDH	7, 14, 28, 35	AP	Analog High Voltage Power.
AVDDL	6, 40	AP	Analog Low Voltage Power.
SVDDL	11	AP	SerDes Low Voltage Power.
PLLVDDL	34	AP	PLL Low Voltage Power.
GND	E-PAD	G	GND.

8. Physical Layer Functional Overview

8.1. MDI Interface

The RTL8213B embeds Single10/100/1000M Ethernet PHYs in one chip. Each port uses a single common MDI interface to support 1000Base-T, 100Base-TX, and 10Base-T. This interface consists of four signal pairs-A, B, C, and D. Each signal pair consists of two bi-directional pins that can transmit and receive at the same time. The MDI interface has internal termination resistors, and therefore reduces BOM cost and PCB complexity. For 1000Base-T, all four pairs are used in both directions at the same time. For 10/100 links and during auto-negotiation, only pairs A and B are used.

8.2. 1000Base-T Transmit Function

The 1000Base-TX transmit function performs 8B/10B coding, scrambling, and 4D-PAM5 encoding. These code groups are passed through a waveform-shaping filter to minimize EMI effects, and are transmitted onto 4-pair CAT5 cable at 125MBaud/s through a D/A converter.

8.3. 1000Base-T Receive Function

Input signals from the media pass through the sophisticated on-chip hybrid circuit to subtract the transmitted signal from the input signal for effective reduction of near-end echo. The received signal is then processed with state-of-the-art technology, e.g., adaptive equalization, BLW (Baseline Wander) correction, cross-talk cancellation, echo cancellation, timing recovery, error correction, and 4D-PAM5 decoding. The 8-bit-wide data is recovered and is sent to the GMII interface at a clock speed of 125MHz. The RX MAC retrieves the packet data from the internal receive MII/GMII interface and sends it to the packet buffer manager.

8.4. 100Base-TX Transmit Function

The 100Base-TX transmit function performs parallel to serial conversion, 4B/5B coding, scrambling, NRZ/NRZI conversion, and MLT-3 encoding. The 5-bit serial data stream after 4B/5B coding is then scrambled as defined by the TP-PMD Stream Cipher function to flatten the power spectrum energy such that EMI effects can be reduced significantly.

The scrambled seed is based on PHY addresses and is unique for each port. After scrambling, the bit stream is driven onto the network media in the form of MLT-3 signaling. The MLT-3 multi-level signaling technology moves the power spectrum energy from high frequency to low frequency, which also reduces EMI emissions.

8.5. 100Base-TX Receive Function

The receive path includes a receiver composed of an adaptive equalizer and DC restoration circuits (to compensate for an incoming distorted MLT-3 signal), an MLT-3 to NRZI and NRZI to NRZ converter to convert analog signals to digital bit-stream, and a PLL circuit to clock data bits with minimum bit error rate. A de-scrambler, 5B/4B decoder, and serial-to-parallel conversion circuits are followed by the PLL circuit. Finally, the converted parallel data is fed into the MAC.

8.6. 10Base-T Transmit Function

The output 10Base-T waveform is Manchester-encoded before it is driven onto the network media. The internal filter shapes the driven signals to reduce EMI emissions, eliminating the need for an external filter.

8.7. 10Base-T Receive Function

The Manchester decoder converts the incoming serial stream to NRZ data when the squelch circuit detects the signal level is above squelch level.

8.8. Auto-Negotiation for UTP

The RTL8213B obtains the states of duplex, speed, and flow control ability for each port in UTP mode through the auto-negotiation mechanism defined in the IEEE 802.3 specifications. During auto-negotiation, each port advertises its ability to its link partner and compares its ability with advertisements received from its link partner. By default, the RTL8213B advertises full capabilities (1000Full, 100Full, 100Half, 10Full, 10Half) together with flow control ability.

8.9. Crossover Detection and Auto Correction

The RTL8213B automatically determines whether or not it needs to crossover between pairs (see Table 11) so that an external crossover cable is not required. When connecting to another device that does not perform MDI crossover, when necessary, the RTL8213B automatically switches its pin pairs to communicate with the remote device. When connecting to another device that does have MDI crossover capability, an algorithm determines which end performs the crossover function.

The crossover detection and auto correction function can be disabled via register configuration. The pin mapping in MDI and MDI Crossover mode is given below.

Table 11. Media Dependent Interface Pin Mapping

Pairs	MDI			MDI Crossover		
	1000Base-T	100Base-TX	10Base-T	1000Base-T	100Base-TX	10Base-T
A	A	TX	TX	B	RX	RX
B	B	RX	RX	A	TX	TX
C	C	Unused	Unused	D	Unused	Unused
D	D	Unused	Unused	C	Unused	Unused

8.10. Polarity Correction

The RTL8213B automatically corrects polarity errors on the receiver pairs in 1000Base-T and 10Base-T modes. In 100Base-TX mode, the polarity is irrelevant.

In 1000Base-T mode, receive polarity errors are automatically corrected based on the sequence of idle symbols. Once the de-scrambler is locked, the polarity is also locked on all pairs. The polarity becomes unlocked only when the receiver loses lock.

In 10Base-T mode, polarity errors are corrected based on the detection of valid spaced link pulses. The detection begins during the MDI crossover detection phase and locks when the 10Base-T link is up. The polarity becomes unlocked when the link is down.

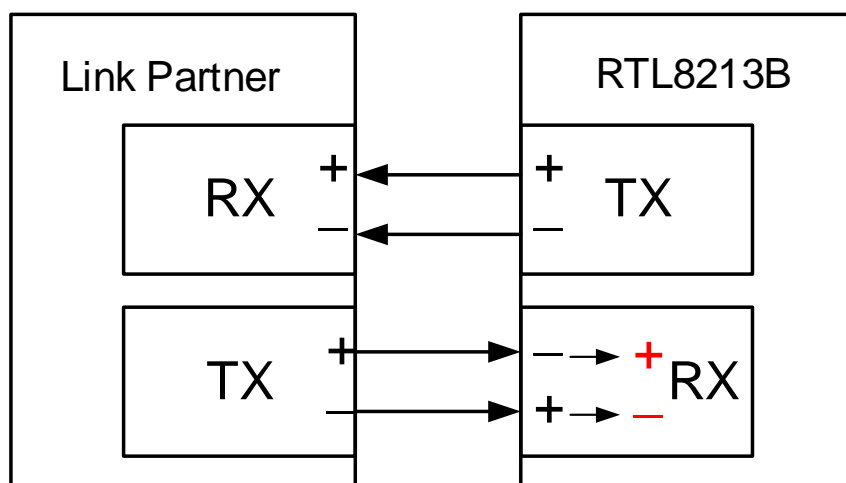


Figure 4. Conceptual Example of Polarity Correction

9. General Function Descriptions

9.1. Reset

9.1.1. Hardware Reset

In a power-on reset, an internal power-on reset pulse is generated and the RTL8213B will start the reset initialization procedures. These are:

- Determine various default settings via the hardware strap pins at the end of the nRESET signal
- Auto-load the configuration from EEPROM if EEPROM is detected
- Complete the embedded SRAM BIST process
- Initialize the packet buffer descriptor allocation
- Initialize the internal registers and prepare them to be accessed by the external CPU

9.1.2. Software Reset

The RTL8213B supports two software resets; a chip reset and a soft reset.

9.1.2.1 CHIP_RESET

When CHIP_RESET is set to 0b1 (write and self-clear), the chip will take the following steps:

1. Download configuration from strap pin and EEPROM
2. Start embedded SRAM BIST (Built-In Self Test)
3. Clear all the Lookup and VLAN tables
4. Reset all registers to default values
5. Restart the auto-negotiation process

9.1.2.2 SOFT_RESET

When SOFT_RESET is set to 0b1 (write and self-clear), the chip will take the following steps:

1. Clear the FIFO and re-start the packet buffer link list
2. Restart the auto-negotiation process

9.2. IEEE 802.3x Full Duplex Flow Control

The RTL8213B supports IEEE 802.3x flow control in 10/100/1000M modes. Flow control can be decided in two ways:

- When Auto-Negotiation is enabled, flow control depends on the result of NWay
- When Auto-Negotiation is disabled, flow control depends on register definition

9.3. Half Duplex Flow Control

In half duplex mode, the CSMA/CD media access method is the means by which two or more stations share a common transmission medium. To transmit, a station waits (defers) for a quiet period on the medium (that is, no other station is transmitting) and then sends the intended message in bit-serial form. If the message collides with that of another station, then each transmitting station intentionally transmits for an additional predefined period to ensure propagation of the collision throughout the system. The station remains silent for a random amount of time (backoff) before attempting to transmit again.

When a transmission attempt has terminated due to a collision, it is retried until it is successful. The scheduling of the retransmissions is determined by a controlled randomization process called ‘Truncated Binary Exponential Backoff’. At the end of enforcing a collision (jamming), the switch delays before attempting to retransmit the frame. The delay is an integer multiple of slot time (512 bit times). The number of slot times to delay before the *n*th retransmission attempt is chosen as a uniformly distributed random integer ‘*r*’ in the range:

$$0 \leq r < 2^k$$

where:

$k = \min(n, \text{backoffLimit})$. The backoffLimit for the RTL8213B is 9.

The half duplex back-off algorithm in the RTL8213B does not have the maximum retry count limitation of 16 (as defined in IEEE 802.3). This means packets in the switch will not be dropped if the back-off retry count is over 16.

9.3.1. Back-Pressure Mode

In Back-Pressure mode, the RTL8213B sends a 4-byte jam pattern (data=0xAA) to collide with incoming packets when congestion control is activated. The Jam pattern collides at the fourth byte counted from the preamble. The RTL8213B supports 48PASS1, which receives one packet after 48 consecutive jam collisions (data collisions are not included in the 48). Enable this function to prevent port partition after 63 consecutive collisions (data collisions + consecutive jam collisions).

9.4. Search and Learning

Search

When a packet is received, the RTL8213B uses the destination MAC address, Filtering Identifier (FID) and Enhanced Filtering Identifier (EFID) to search the 2048-entry look-up table. The 48-bit MAC address, 4-bit FID and 3-bit EFID use a hash algorithm, to calculate an 11-bit index value. The RTL8213B uses the index to compare the packet MAC address with the entries (MAC addresses) in the look-up table. This is the 'Address Search'. If the destination MAC address is not found, the switch will broadcast the packet according to VLAN configuration.

Learning

The RTL8213B uses the source MAC address, FID, and EFID of the incoming packet to hash into a 9-bit index (4-entry). It then compares the source MAC address with the data (MAC addresses) in this index. If there is a match with one of the entries, the RTL8213B will update the entry with new information. If there is no match and the 4 entries are not all occupied by other MAC addresses, the RTL8213B will record the source MAC address and ingress port number into an empty entry. This process is called 'Learning'.

Address aging is used to keep the contents of the address table correct in a dynamic network topology. The look-up engine will update the time stamp information of an entry whenever the corresponding source MAC address appears. An entry will be invalid (aged out) if its time stamp information is not refreshed by the address learning process during the aging time period. The aging time of the RTL8213B is between 200 and 400 seconds (typical is 300 seconds).

9.5. SVL and IVL/SVL

The RTL8213B supports a 16-group Filtering Identifier (FID) for L2 search and learning. In default operation, all VLAN entries belong to the same FID. This is called Shared VLAN Learning (SVL). If VLAN entries are configured to different FIDs, then the same source MAC address with multiple FIDs can be learned into different look-up table entries. This is called Independent VLAN Learning and Shared VLAN Learning (IVL/SVL).

9.6. Illegal Frame Filtering

Illegal frames such as CRC error packets, runt packets (length <64 bytes), and oversize packets (length >maximum length) will be discarded by the RTL8213B. The maximum packet length may be set from 1518 bytes to 16K bytes.

9.7. IEEE 802.3 Reserved Group Addresses Filtering Control

The RTL8213B supports the ability to drop/forward IEEE 802.3 specified reserved group MAC addresses: 01-80-C2-00-00-00 to 01-80-C2-00-00-2F. The default setting enables forwarding of these reserved group MAC address control frames. Frames with group MAC address 01-80-C2-00-00-01 (802.3x Pause) will always be filtered. Table 12 shows the Reserved Multicast Address (RMA) configuration mode from 01-80-C2-00-00-00 to 01-80-C2-00-00-2F.

Table 12. Reserved Multicast Address Configuration Table

Assignment	Value
Bridge Group Address	01-80-C2-00-00-00
IEEE Std 802.3, 1988 Edition, Full Duplex PAUSE Operation	01-80-C2-00-00-01
IEEE Std 802.3ad Slow Protocols-Multicast Address	01-80-C2-00-00-02
IEEE Std 802.1X PAE Address	01-80-C2-00-00-03
Provider Bridge Group Address	01-80-C2-00-00-08
Undefined 802.1 Address	01-80-C2-00-00-04 ~ 01-80-C2-00-00-07 & 01-80-C2-00-00-09 ~ 01-80-C2-00-00-0C & 01-80-C2-00-00-0F
Provider Bridge MVRP Address	01-80-C2-00-00-0D
IEEE Std 802.1AB Link Layer Discovery Protocol Address	01-80-C2-00-00-0E
All LANs Bridge Management Group Address	01-80-C2-00-00-10
Load Server Generic Address	01-80-C2-00-00-11
Loadable Device Generic Address	01-80-C2-00-00-12
Undefined 802.1 Address	01-80-C2-00-00-13 ~ 01-80-C2-00-00-17 & 01-80-C2-00-00-19 & 01-80-C2-00-00-1B ~ 01-80-C2-00-00-1F
Generic Address for All Manager Stations	01-80-C2-00-00-18
Generic Address for All Agent Stations	01-80-C2-00-00-1a
GMRP Address	01-80-C2-00-00-20
GVRP Address	01-80-C2-00-00-21
Undefined GARP Address	01-80-C2-00-00-22 01-80-C2-00-00-2F
CDP (Cisco Discovery Protocol)	01-00-0C-CC-CC-CC
CSSTP (Cisco Shared Spanning Tree Protocol)	01-00-0C-CC-CC-CD
LLDP	(01:80:c2:00:00:0e or 01:80:c2:00:00:03 or 01:80:c2:00:00:00) && ethertype = 0x88CC

9.8. Broadcast/Multicast/Unknown DA Storm Control

The RTL8213B enables or disables per-port broadcast/multicast/unknown DA storm control by setting registers (default is disabled). After the receiving rate of broadcast/multicast/unknown DA packets exceeds a reference rate (number of Kbps per second or number of packets per second), all other broadcast/multicast/unknown DA packets will be dropped. The reference rate is set via register configuration.

9.9. Port Security Function

The RTL8213B supports three types of security function to prevent malicious attacks:

- Per-port enable/disable SA auto-learning for an ingress packet
- Per-port enable/disable look-up table aging update function for an ingress packet
- Per-port enable/disable drop all unknown DA packets

9.10. MIB Counters

The RTL8213B supports a set of counters to support management functions.

- MIB-II (RFC 1213)
- Ethernet-Like MIB (RFC 3635)
- Interface Group MIB (RFC 2863)
- RMON (RFC 2819)
- Bridge MIB (RFC 1493)
- Bridge MIB Extension (RFC 2674)

9.11. Port Mirroring

The RTL8213B supports one set of port mirroring functions for all ports. The TX, or RX, or both TX/RX packets from multiple mirrored port can be mirrored to one monitor port.

9.12. VLAN Function

The RTL8213B supports 4096 VLAN groups. These can be configured as port-based VLANs, IEEE 802.1Q tag-based VLANs, and Protocol-based VLANs. Two ingress-filtering and egress-filtering options provide flexible VLAN configuration:

Ingress Filtering

- The acceptable frame type of the ingress process can be set to ‘Admit All’, ‘Admit only Untagged’ or ‘Admit only Tagged’
- ‘Admit’ or ‘Discard’ frames associated with a VLAN for which that port is not in the member set

Egress Filtering

- ‘Forward’ or ‘Discard’ Leaky VLAN frames between different VLAN domains
- ‘Forward’ or ‘Discard’ Multicast VLAN frames between different VLAN domains

The VLAN tag can be inserted or removed at the output port. The RTL8213B will insert a Port VID (PVID) for untagged frames, or remove the tag from tagged frames. The RTL8213B also supports a special insert VLAN tag function to separate traffic from the WAN and LAN sides in Router and Gateway applications.

9.12.1. Port-Based VLAN

This default configuration of the VLAN function can be modified via an attached Slave I2C-like serial Interface, or Slave Media Independent Interface Management (MIIM) Interface. The 4096-entry VLAN Table designed into the RTL8213B provides full flexibility for users to configure the input ports to associate with different VLAN groups. Each input port can join with more than one VLAN group.

Port-based VLAN mapping is the simplest implicit mapping rule. Each ingress packet is assigned to a VLAN group based on the input port. It is not necessary to parse and inspect frames in real-time to determine their VLAN association. All the packets received on a given input port will be forwarded to this port’s VLAN members.

9.12.2. IEEE 802.1Q Tag-Based VLAN

The RTL8213B supports 4096 VLAN entries to perform 802.1Q tag-based VLAN mapping. In 802.1Q VLAN mapping, the RTL8213B uses a 12-bit explicit identifier in the VLAN tag to associate received packets with a VLAN. The RTL8213B compares the explicit identifier in the VLAN tag with the 4096 VLAN Table to determine the VLAN association of this packet, and then forwards this packet to the member set of that VLAN. Two VIDs are reserved for special purposes. One of them is all 1’s, which is reserved and currently unused. The other is all 0’s, which indicates a priority tag. A priority-tagged frame should be treated as an untagged frame.

Two VLAN ingress filtering functions are supported in registers by the RTL8213B. One is the ‘VLAN tag admit control, which provides the ability to receive VLAN-tagged frames only. Untagged or priority tagged (VID=0) frames will be dropped. The other is ‘VLAN member set ingress filtering’, which will drop frames if the ingress port is not in the member set.

9.12.3. Protocol-Based VLAN

The RTL8213B supports a 4-group Protocol-based VLAN configuration. The packet format can be RFC 1042, LLC, or Ethernet, as shown in Figure 5. There are 4 configuration tables to assign the frame type and

corresponding field value. Taking IP packet configuration as an example, the user can configure the frame type to be ‘Ethernet’, and value to be ‘0x0800’. Each table will index to one of the entries in the 4096-entry VLAN table. The packet stream will match the protocol type and the value will follow the VLAN member configuration of the indexed entry to forward the packets.

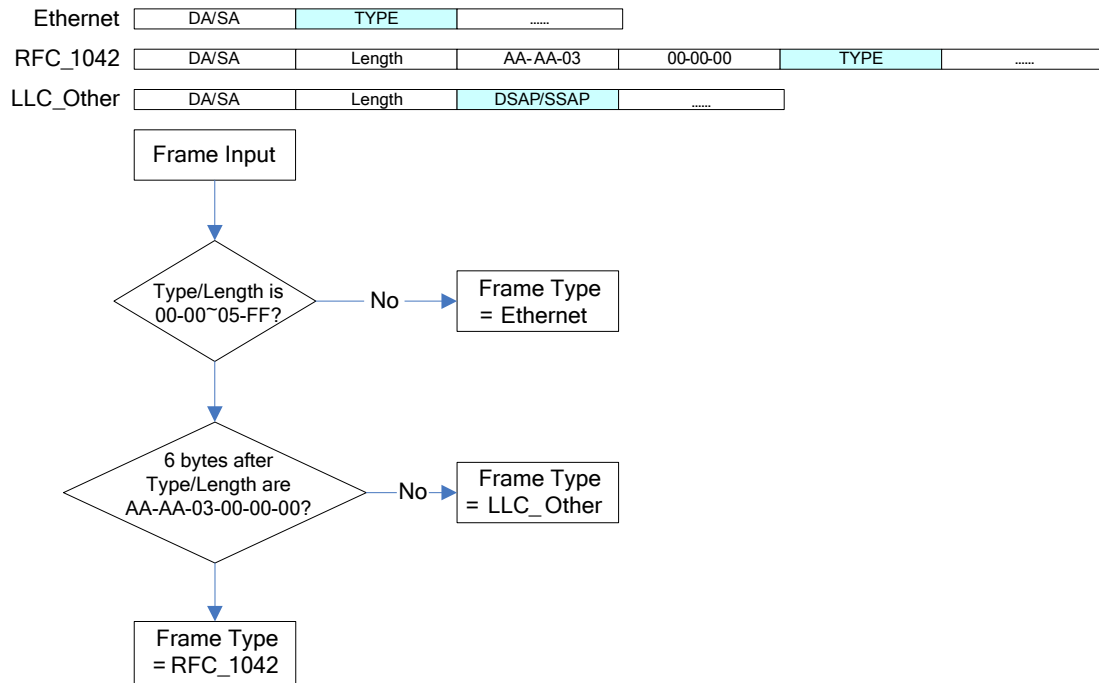


Figure 5. Protocol-Based VLAN Frame Format and Flow Chart

9.13. QoS Function

The RTL8213B supports 8 priority queues and input bandwidth control. Packet priority selection can depend on Port-based priority, 802.1p/Q Tag-based priority, IPv4/IPv6 DSCP-based priority, and ACL-based priority. When multiple priorities are enabled in the RTL8213B, the packet’s priority will be assigned based on the priority selection table.

Each queue has one leaky bucket for Average Packet Rate. Per-queue in each output port can be set as Strict Priority (SP) or Weighted Round Robin (WRR), or Weighted Fair Queue (WFQ) for packet scheduling algorithm.

9.13.1. Input Bandwidth Control

Input bandwidth control limits the input bandwidth. When input traffic is more than the RX Bandwidth parameter, this port will either send out a ‘pause ON’ frame, or drop the input packet depending on register setup. Per-port input bandwidth control rates can be set from 8Kbps to 1Gbps (in 8Kbps steps).

9.13.2. Priority Assignment

Priority assignment specifies the priority of a received packet according to various rules. The RTL8213B can recognize the QoS priority information of incoming packets to give a different egress service priority.

The RTL8213B identifies the priority of packets based on several types of QoS priority information:

- Port-based priority
- 802.1p/Q-based priority
- IPv4/IPv6 DSCP-based priority
- ACL-based priority
- VLAN-based priority
- MAC-based priority
- SVLAN-based priority

9.13.3. Priority Queue Scheduling

The RTL8213B supports MAX-MIN packet scheduling.

Packet scheduling offers two modes:

- Average Packet Rate (APR) leaky bucket, which specifies the average rate of one queue
- Weighted Fair Queue (WFQ), which decides which queue is selected in one slot time to guarantee the minimal packet rate of one queue
- Weighted Round Robin (WRR)

In addition, each queue of each port can select Strict Priority or WFQ or WRR packet scheduling according to packet scheduling mode.

9.13.4. IEEE 802.1p/Q and DSCP Remarking

The RTL8213B supports the IEEE 802.1p/Q and IP DSCP (Differentiated Services Code Point) remarking function. When packets egress from one of the 8 queues, the packet's 802.1p/Q priority and IP DSCP can optionally be remarked to a configured value. 802.1p/Q priority & IP DSCP value can be remarked based on internal priority or original 802.1p/Q priority & IP DSCP value in packets.

9.13.5. ACL-Based Priority

The RTL8213B supports 48-entry ACL (Access Control List) rules. When a packet is received, its physical port, Layer2, Layer3, and Layer4 information are recorded and compared to ACL entries. If a received packet matches multiple entries, the entry with the lowest address is valid. If the entry is valid, the action bit will be applied to which related action bit is enable.

If a packet hits an ACL rule and the priority action bit is 'enable', then this packet gets a 3-bit ACL-priority from the ACL module.

9.14. IEEE 802.1x Function

The RTL8213B supports IEEE 802.1x Port-based/MAC-based Access Control.

- Port-Based Access Control for each port
- Authorized Port-Based Access Control for each port
- Port-Based Access Control Direction for each port
- MAC-Based Access Control for each port
- MAC-Based Access Control Direction
- Optional Unauthorized Behavior

9.14.1. Port-Based Access Control

Each port of the RTL8213B can be set to 802.1x port-based authenticated checking function usage and authorized status. Ports with 802.1X unauthorized status will drop received/transmitted frames.

9.14.2. Authorized Port-Based Access Control

If a dedicated port is set to 802.1x port-based access control, and passes the 802.1x authorization, then its port authorization status can be set to authorized.

9.14.3. Port-Based Access Control Direction

Ports with 802.1X unauthorized status will drop received/transmitted frames only when port authorization direction is 'BOTH'. If the authorization direction of an 802.1X unauthorized port is IN, incoming frames to that port will be dropped, but outgoing frames will be transmitted.

9.14.4. MAC-Based Access Control

MAC-Based Access Control provides authentication for multiple logical ports. Each logical port represents a source MAC address. There are multiple logical ports for a physical port. When a logical port or a MAC address is authenticated, the relevant source MAC address has the authorization to access the network. A frame with a source MAC address that is not authenticated by the 802.1x function will be dropped or trapped to the CPU.

9.14.5. MAC-Based Access Control Direction

Unidirectional and Bi-directional control are two methods used to process frames in 802.1x. As the system cannot predict which port the DA is on, a system-wide MAC-based access control direction setup is provided for determining whether receiving or bi-direction should be authorized.

If MAC-based access control direction is BOTH, then received frames with unauthenticated SA or unauthenticated DA will be dropped. When MAC-based access control direction is IN, only received frames with unauthenticated SA will be dropped.

9.14.6. Optional Unauthorized Behavior

Port-Based Network Access Control and MAC-Based Access Control offer a whole system control to determine unauthorized frame dropping, or trapping to CPU.

9.15. IEEE 802.1D Function

When using IEEE 802.1D, the RTL8213B supports 16 sets and four status' for each port for CPU implementation 802.1D (STP) and 802.1s (MSTP) function:

- Disabled: The port will not transmit/receive packets, and will not perform learning
- Blocking: The port will only receive BPDU spanning tree protocol packets, but will not transmit any packets, and will not perform learning
- Learning: The port will receive any packet, including BPDU spanning tree protocol packets, and will perform learning, but will only transmit BPDU spanning tree protocol packets
- Forwarding: The port will transmit/receive all packets, and will perform learning

The RTL8213B also supports a per-port transmission/reception enable/disable function. Users can control the port state via register.

9.16. Realtek Cable Test (RTCT)

The RTL8213B physical layer transceivers use DSP technology to implement the Realtek Cable Test (RTCT) feature. The RTCT function can be used to detect short, open or impedance mismatch in each differential pair. The RTL8213B also provides LED support to indicate test status and results.

9.17. LED Indicators

The RTL8213B supports parallel LEDs for each port. Port 3 has three LED indicator pins, LED0, LED1, LED2, and Port 6 has two LED indicator pins, LED0, LED1. Each pin may have different indicator information (defined in Table 13). Refer to section 7.4 LED Pins, page 9 for pin details.

Table 13. LED Definitions

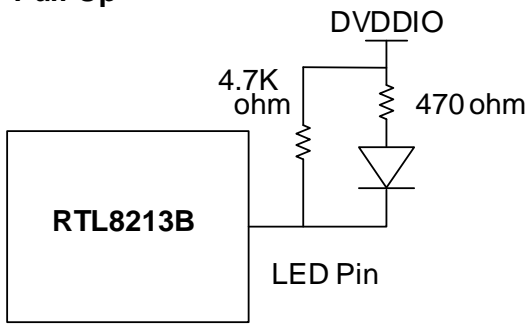
LED Status	Description
LED_Off	LED Output off.
Dup/Col	Duplex/Collision Indicator. Blinking when collision occurs. Low for full duplex, and high for half duplex mode.
Link/Act	Link, Activity Indicator. Low for link established. Link/Act Blinking when the corresponding port is transmitting or receiving.
Spd1000	1000Mbps Speed Indicator. Low for 1000Mbps.
Spd100	100Mbps Speed Indicator. Low for 100Mbps.
Spd10	10Mbps Speed Indicator. Low for 10Mbps.
Spd1000/Act	1000Mbps Speed/Activity Indicator. Low for 1000Mbps. Blinking when the corresponding port is transmitting or receiving.
Spd100/Act	100Mbps Speed/Activity Indicator. Low for 100Mbps. Blinking when the corresponding port is transmitting or receiving.
Spd10/Act	10Mbps Speed/Activity Indicator. Low for 10Mbps. Blinking when the corresponding port is transmitting or receiving.
Spd100 (10)/Act	10/100Mbps Speed/Activity Indicator. Low for 10/100Mbps. Blinking when the corresponding port is transmitting or receiving.
Act	Activity Indicator. Act blinking when the corresponding port is transmitting or receiving.

The LED pin also supports pin strapping configuration functions. The PnLED0, PnLED1, and PnLED2 pins are dual-function pins: input operation for configuration upon reset, and output operation for LED after reset. When the pin input is pulled high upon reset, the pin output is active low after reset. When the pin input is pulled down upon reset, the pin output is active high after reset (see Figure 6 and Figure 7). Typical values for pull-up/pull-down resistors are 4.7K Ω .

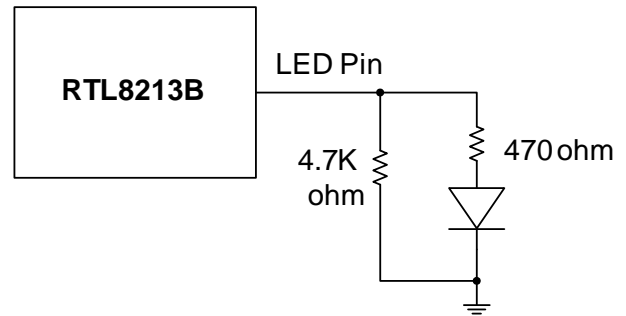
The PnLED1 can be combined with PnLED0 or PnLED2 as a Bi-color LED.

The PnLED1 should operate with the same polarity as other Bi-color LED pins. For example:

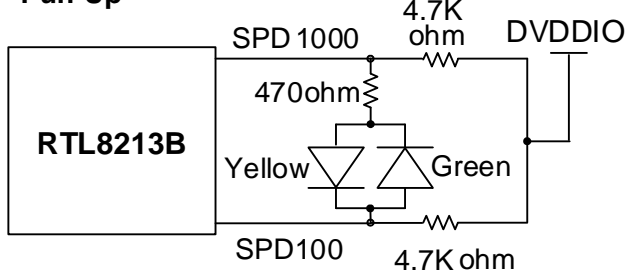
- P3LED1 should pull up upon reset if P3LED1 is combined with P3LED2 as a Bi-color LED, and P3LED2 input is pulled high upon reset. In this configuration, the output of these pins is active low after reset
- P3LED1 should be pulled down upon reset if P3LED1 is combined with P3LED2 as a Bi-color LED, and P3LED2 input is pulled down upon reset. In this configuration, the output of these pins is active high after reset

Pull-Up


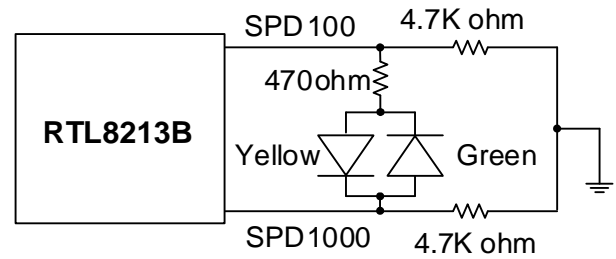
LED Pins Output Active Low

Pull-Down


LED Pins Output Active High

Figure 6. Pull-Up and Pull-Down of LED Pins for Single-Color LED
Pull-Up


LED Pins Output Active Low

Pull-Down


LED Pins Output Active High

Figure 7. Pull-Up and Pull-Down of LED Pins for Bi-Color LED

9.18. Green Ethernet

9.18.1. Link-On and Cable Length Power Saving

The RTL8213B provides link-on and dynamic detection of cable length and dynamic adjustment of power required for the detected cable length. This feature provides high performance with minimum power consumption.

9.18.2. Link-Down Power Saving

The RTL8213B implements link-down power saving on a per-port basis, greatly cutting power consumption when the network cable is disconnected. After it detects an incoming signal, it wakes up from link-down power saving and operates in normal mode.

9.19. Regulator

The RTL8213B embeds a 3.3V-1.1V switch regulator to simplify the power solution. The 1.1V output power is used for the digital core and analog circuits. Do not use the regulator for other chips, even if the rating is enough.

10. Interface Descriptions

10.1. Master I2C for EEPROM Auto-load

The EEPROM interface of the RTL8213B uses the serial I2C bus to read the serial EEPROM. When the RTL8213B is powered up, it drives SCK and SDA to read the configuration data from the EEPROM by strapping configuration.

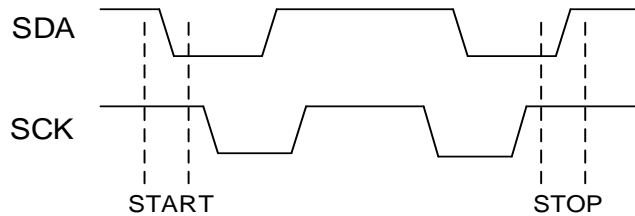


Figure 8. SMI Start and Stop Command

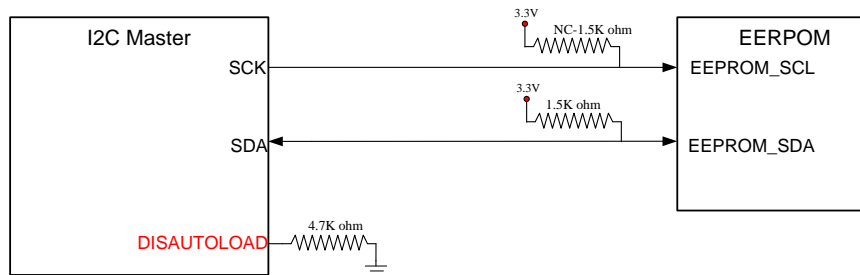


Figure 9. Master I2C for EEPROM Auto-load Interface Connection Example

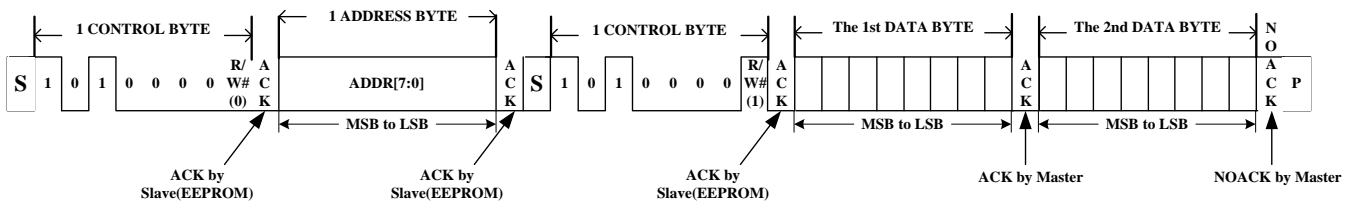


Figure 10. 8-Bit EEPROM Sequential Read

10.2. Realtek Slave I2C-Like Interface for External CPU to Access the RTL8213B

When EEPROM auto-load is complete, the RTL8213B registers can be accessed through SCK and SDA via an external CPU. The device address of the RTL8213B is 0x4. For the start and end of a write/read command, SCK needs one extra clock before/after the start/stop signals.

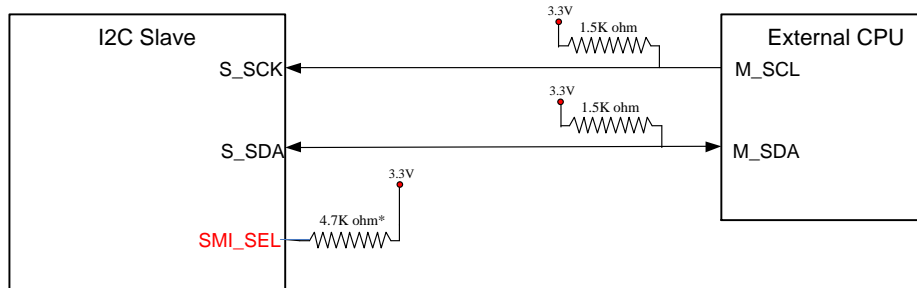


Figure 11. Realtek Slave I2C-Like for External CPU Access Interface Connection Example

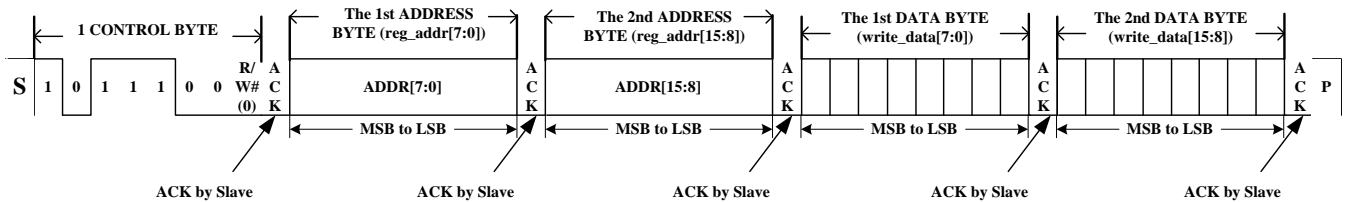


Figure 12. Realtek Slave I2C-Like Interface Write Command

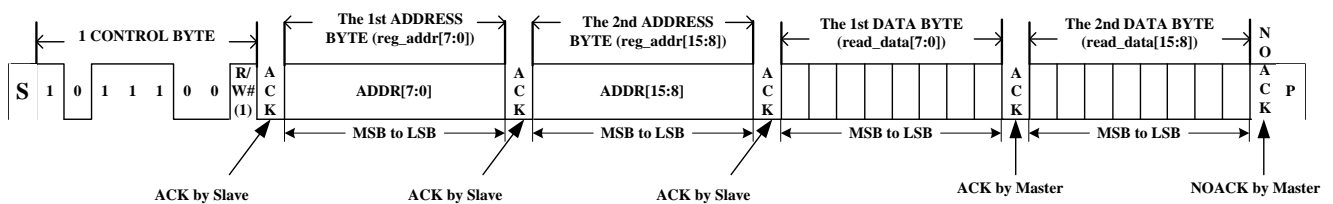


Figure 13. Realtek Slave I2C-Like Interface Read Command

10.3. Slave MII Management SMI Interface for External CPU to Access RTL8213B

The RTL8213B registers can be accessed via Slave MDC and MDIO via an external CPU (Decided by Strapping Configuration).

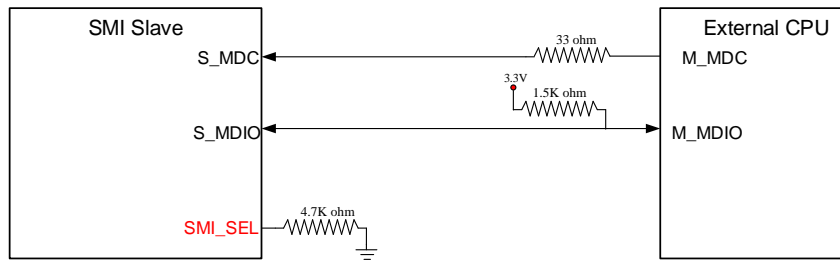


Figure 14. Slave MII Management SMI Interface Connection Example

Table 14. Slave MII Management SMI Access Format

	Management Frame Fields							
	PRE	ST	OP	DEVAD	REGAD	TA	DATA	IDLE
Read	1...1	01	10	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDDDD	Z
Write	1...1	01	01	AAAAA	RRRRR	10	DDDDDDDDDDDDDDDDDD	Z

Note: By default the Slave needs no less than 32bit Preambles (PRE) before accessing the slave via the Slave SMI interface. An external CPU can configure the Slave to enable the preamble suppression function. When preamble suppression is enabled the Slave does not need preamble before accessing the slave.

11. Electrical Characteristics

11.1. Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltages are specified reference to GND unless otherwise specified.

Table 15. Absolute Maximum Ratings

Parameter	Min	Max	Units
Junction Temperature (Tj)	-	+125	°C
Storage Temperature	-45	+125	°C
DVDDIO, AVDDH, HV_SWR Supply Referenced to GND, AGND, and GND_SWR	GND-0.3	+3.63	V
DVDDL, AVDDL, SVDDL, PLLVDDL Supply Referenced to GND, AGND, and GND_SWR	GND-0.3	+1.21	V
Digital Input Voltage	GND-0.3	VDDIO+0.3	V

11.2. Recommended Operating Range

Table 16. Recommended Operating Range

Parameter	Min	Typical	Max	Units
Ambient Operating Temperature (Ta)	0	-	70	°C
DVDDIO Supply Voltage Range	3.135	3.3	3.465	V
AVDDH and HV_SWR Supply Voltage Range	3.135	3.3	3.465	V
DVDDL, AVDDL, SVDDL, and PLLVDDL Supply Voltage Range	1.045	1.1	1.155	V

11.3. Thermal Characteristics

11.3.1. Assembly Description

Table 17. Assembly Description

Package	Type	QFN-40
	Dimension (L×W)	5×5 mm ²
	Thickness	0.85 mm
PCB	PCB Dimension (L×W)	78.1×61.4 mm ²
	PCB Thickness	1.6 mm
	Number of Cu Layer-PCB	4-Layer: - 1st layer (1oz): 20% coverage of Cu - 2nd layer (1oz): 80% coverage of Cu - 3rd layer (1oz): 80% coverage of Cu - 4th layer (1oz): 75% coverage of Cu

11.3.2. Material Properties

Table 18. Material Properties

	Item	Material	Thermal Conductivity K (W/m-k)
Package	Die	Si	147
	Silver Paste	1033BF	2.5
	Lead Frame	CDA7025	168
	Mold Compound	7372	0.9
PCB		Cu	400
		FR4	0.2

11.3.3. Simulation Conditions

Table 19. Simulation Conditions

Input Power	0.52W
Test Board (PCB)	4L (2S2P) / 2L (1S1P)
Control Condition	Air Flow = 0m/s

11.3.4. Thermal Performance of QFN-56 on PCB Under Still Air Convection

Table 20. Thermal Performance of QFN-56 on PCB Under Still Air Convection

	θ_{JA}	θ_{JB}	θ_{JC}	Ψ_{JT}
4L PCB	30.9	6.59	15.4	0.30
2L PCB	42.2	7.93	17.6	0.42

Note:

θ_{JA} : Junction to ambient thermal resistance

θ_{JB} : Junction to board thermal resistance

θ_{JC} : Junction to case thermal resistance

Ψ_{JT} : Junction-to-top-center thermal characterization parameter

11.4. DC Characteristics

Table 21. DC Characteristics

Parameter	SYM	Min	Typical	Max	Units
System Idle (All UTP Ports Link Down, and Extension Port Link Down, without LEDs)					
Power Supply Current for VDDH	I_{DVDDIO}, I_{AVDDH}	-	13	-	mA
Power Supply Current for VDDL	$I_{DVDDL}, I_{AVDDL}, I_{SVDDL}, I_{PLLVDDL}$	-	132	-	mA
1000M Active (All UTP Ports 1000M Link/Active, and Extension Port Link/Active as 1000Base-X, without LEDs)					
Power Supply Current for VDDH	I_{DVDDIO}, I_{AVDDH}	-	70	-	mA
Power Supply Current for VDDL	$I_{DVDDL}, I_{AVDDL}, I_{SVDDL}, I_{PLLVDDL}$	-	218	-	mA
VDDIO=3.3V					
TTL Input High Voltage	V_{ih}	2.0	-	-	V
TTL Input Low Voltage	V_{il}	-	-	0.7	V
Output High Voltage	V_{oh}	2.7	-	-	V
Output Low Voltage	V_{ol}	-	-	0.6	V

Note: Power Consumption test condition, DVDDIO=3.3V, AVDDH=3.3V, DVDDL=1.1V, AVDDL=1.1V, SVDDL=1.1V, and PLLVDDL=1.1V. Embedded Switch Regulator disabled.

11.5. Switch Regulator

Table 22. Switch Regulator

Symbol	Parameter	Min	Typ	Max	Units
F_{sw}	Oscillator Frequency	-	2	-	MHz
T_{ss}	Soft-Start Time	-	1.5	-	ms

11.6. AC Characteristics

11.6.1. Master I2C for EEPROM Auto-load Interface Timing Characteristics

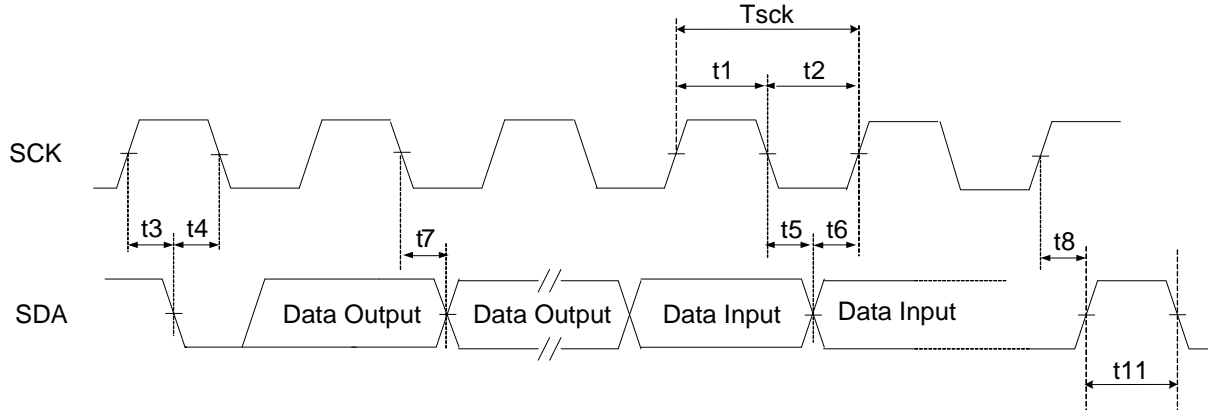


Figure 15. Master I2C for EEPROM Auto-load Timing Characteristics

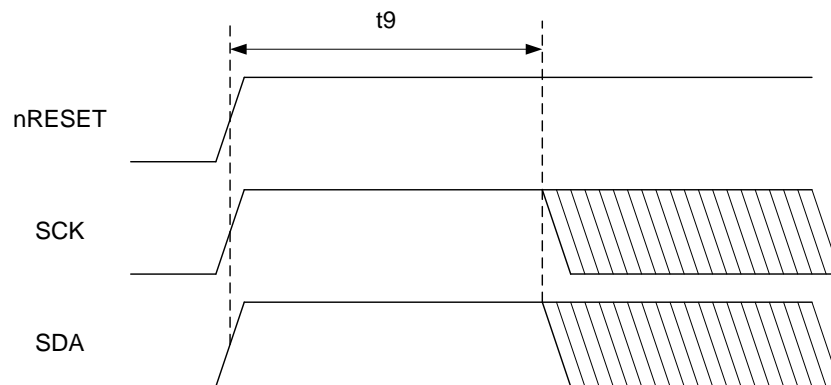


Figure 16. SCK/SDA Power on Timing

Table 23. Master I2C for EEPROM Auto-load Timing Characteristics

Symbol	Description	Type	Min	Typical	Max	Units
T_{sck}	SCK Clock Period	O	-	9	-	μs
t_1	SCK High Time	O	4.05	4.5	-	μs
t_2	SCK Low Time	O	4.05	4.5	-	μs
t_3	START Condition Setup Time	O	2	-	-	μs
t_4	START Condition Hold Time	O	2	-	-	μs
t_5	Data Input Hold Time	O	0	-	-	μs
t_6	Data Input Setup Time	O	10	-	-	μs
t_7	Data output delay	O	2.15	-	2.35	μs
t_8	STOP Condition Setup Time	O	2	-	-	μs
t_9	SCK/SDA Active from Reset Ready	O	-	76.8	-	ms

Symbol	Description	Type	Min	Typical	Max	Units
t11	Time the bus free before new START	O	10	-	-	μs
-	SCK Rise Time (10% to 90%)	O	-	-	100	ns
-	SCK Fall Time (90% to 10%)	O	-	-	100	ns
-	Duty Cycle	O	40	50	60	%

11.6.2. Slave I2C-like Mode Timing Characteristics

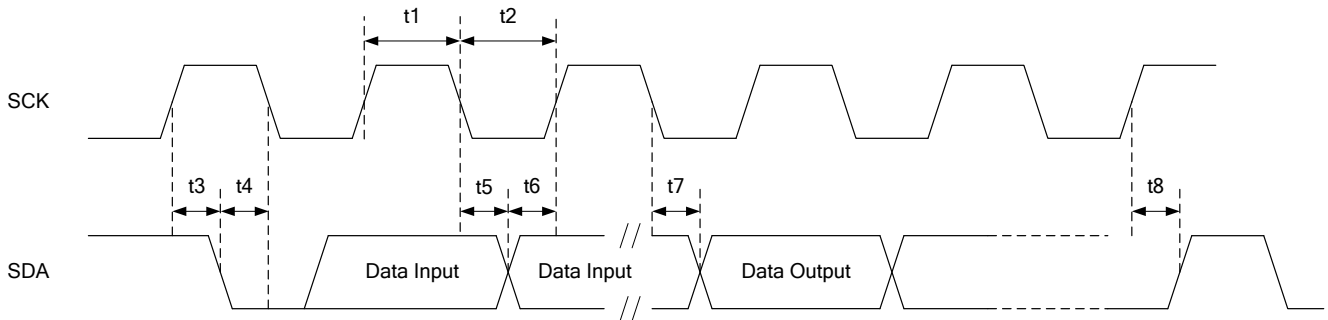


Figure 17. Slave I2C-like Mode Timing Characteristics

Table 24. Slave I2C-like Mode Timing Characteristics

Symbol	Description	Type	Min	Typical	Max	Units
t1	SCK High Time	I	250	-	-	ns
t2	SCK Low Time	I	250	-	-	ns
t3	START Condition Setup Time	I	150	-	-	ns
t4	START Condition Hold Time	I	150	-	-	ns
t5	Data Hold Time	I	150	-	-	ns
t6	Data Setup Time	I	150	-	-	ns
t7	Clock to Data Output Delay	O	10	-	100	ns
t8	STOP Condition Setup Time	I	150	-	-	ns

11.6.3. Slave MII Management SMI for External CPU Access Interface Timing Characteristics

The RTL8213B supports MDIO slave mode. The Master (CPU) can access the Slave (RTL8213B) registers via the MDIO interface. The MDIO is a bi-directional signal that can be sourced by the Master or the Slave. In a write command, the master sources the MDIO signal. In a read command, the slave sources the MDIO signal.

- The timing characteristics t1, t2, and t3 (Table 25) of the Master (the RTL8213B link partner CPU) are provided by the Master when the Master sources the MDIO signal (Write command)
- The timing characteristic t4 (Table 25) of the Slave (RTL8213B) are provided by the RTL8213B when the RTL8213B sources the MDIO signal (Read command)

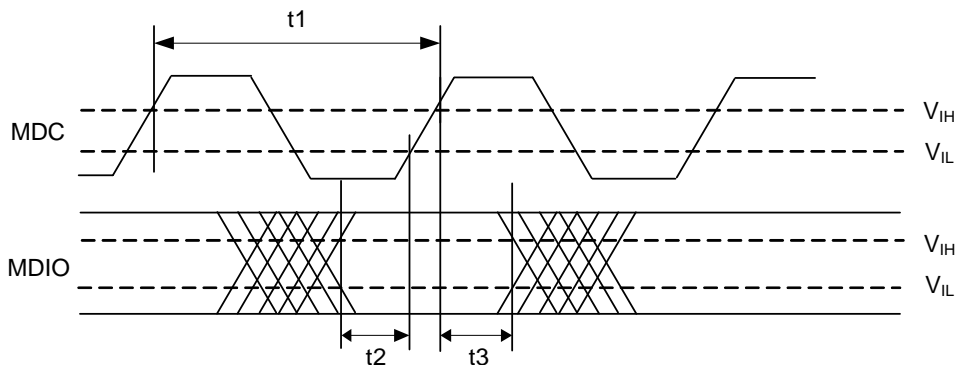


Figure 18. MDIO Sourced by the Master

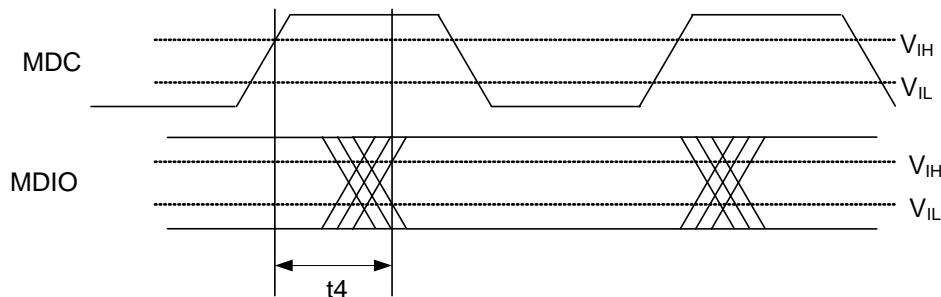


Figure 19. MDIO Sourced by the RTL8213B (Slave)

Table 25. MDIO Timing Characteristics and Requirement

Parameter	SYM	Description/Condition	Type	Min	Typical	Max	Units
MDC Clock Period	t1	Clock Period	I	125	-	-	ns
MDIO to MDC Rising Setup Time (Write Data)	t2	Input Setup Time	I	8	-	-	ns
MDIO to MDC Rising Hold Time (Write Data)	t3	Input Hold Time	I	8	-	-	ns
MDC to MDIO Delay Time (Read Data)	t4	Clock (Rising Edge) to Data Delay Time	O	0	-	80	ns

11.6.4. SGMII/1000Base-X Characteristics

Table 26. SGMII/1000Base-X Differential Transmitter Characteristics

Parameter	SYM	Min	Typ	Max	Units	Notes
Unit Interval	UI	799.92	800	800.08	ps	800ps ± 100ppm
Eye Mask	T_X1	-	-	0.15	UI	-
Eye Mask	T_X2	-	-	0.4	UI	-
Eye Mask	T_Y1	150	-	-	mV	-
Eye Mask	T_Y2	-	-	600	mV	-
Output Differential Voltage	V _{TX-DIFFp-p}	300	700	800	mV	-
Minimum TX Eye Width	T _{TX-EYE}	0.7	-	-	UI	-
Output Jitter	T _{TX-JITTER}	-	-	0.3	UI	T _{TX-JITTER-MAX} = 1 - T _{TX-EYE-MIN} = 0.30UI
Data dependent jitter		-	0.0875	-	UI	
Output Rise Time	T _{TX-RISE}	0.125	-	0.25	UI	20% ~ 80%
Output Fall Time	T _{TX-FALL}	0.125	-	0.25	UI	20% ~ 80%
Output impedance	R _{TX}	40	-	140	ohm	single-end
AC Coupling Capacitor	C _{TX}	80	100	120	nF	-
Transmit Length in PCB	L _{TX}	-	-	10	inch	-

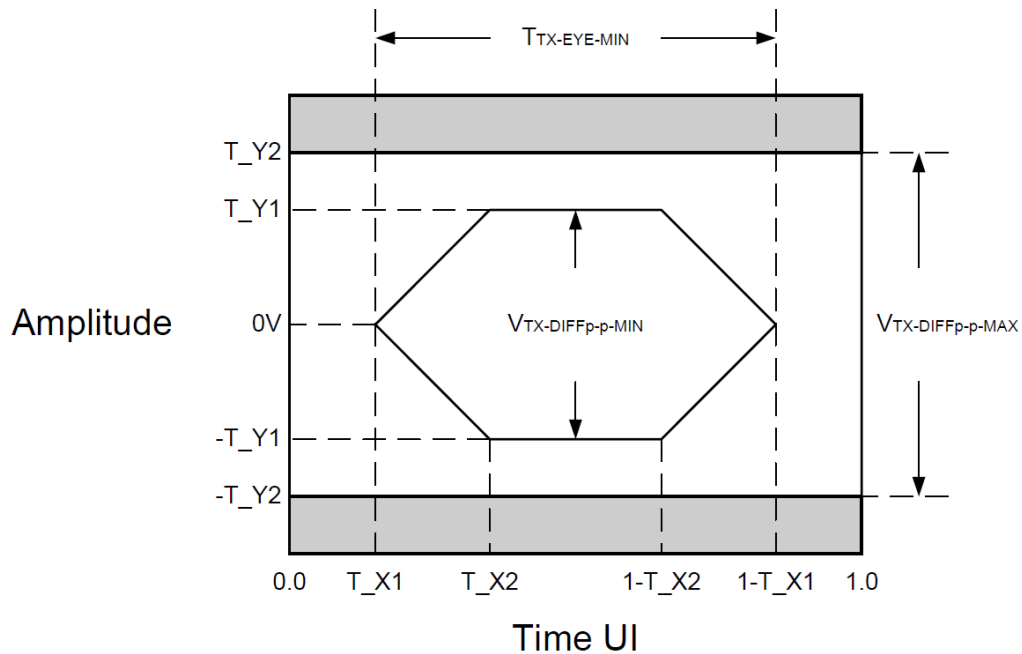
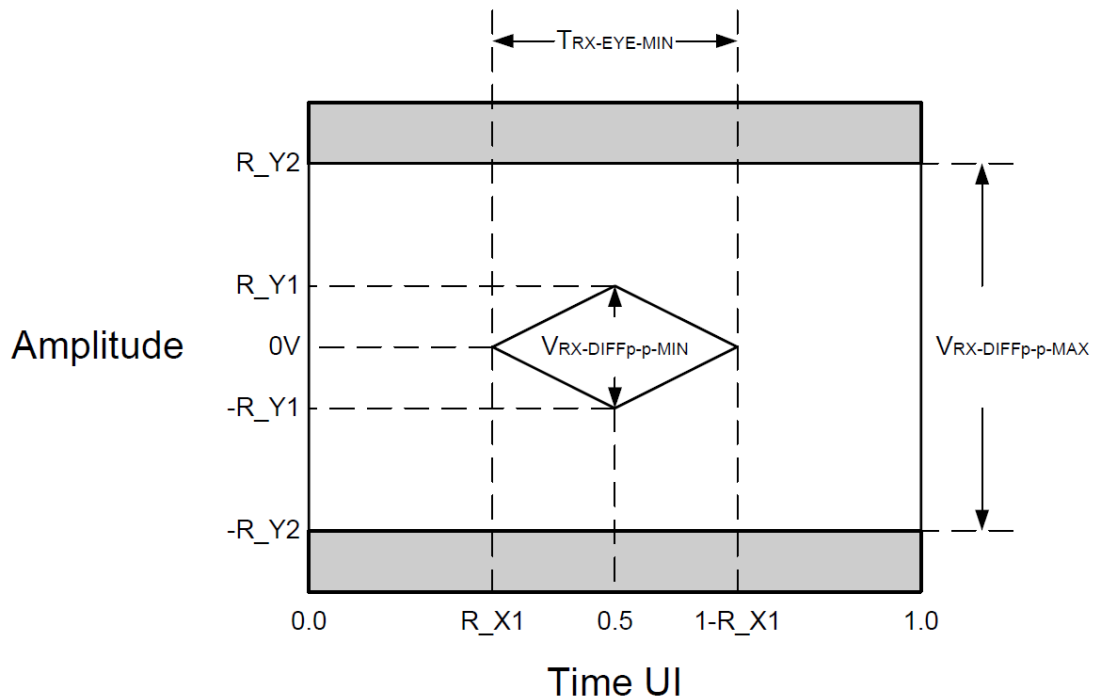

Figure 20. SGMII/1000Base-X Differential Transmitter Eye Diagram

Table 27. SGMII/1000Base-X Differential Receiver Characteristics

Parameter	SYM	Min	Typ	Max	Units	Notes
Unit Interval	UI	799.92	800	800.08	ps	800ps ± 100ppm
Eye Mask	R_X1	-	-	0.15	UI	-
Eye Mask	R_Y1	100	-	-	mV	-
Eye Mask	R_Y2	-	-	600	mV	-
Input Differential Voltage	V _{RX-DIFFp-p}	200	-	1200	mV	-
Minimum RX Eye Width	T _{RX-EYE}	0.4	-	-	UI	-
Input Jitter Tolerance	T _{RX-JITTER}	-	-	0.6	UI	T _{RX-JITTER-MAX} = 1 - T _{RX-EYE-MIN} = 0.6UI
Differential Resistance	R _{RX}	80	100	120	ohm	-


Figure 21. SGMII/1000Base-X Differential Receiver Eye Diagram

11.6.5. Power and Reset Characteristics

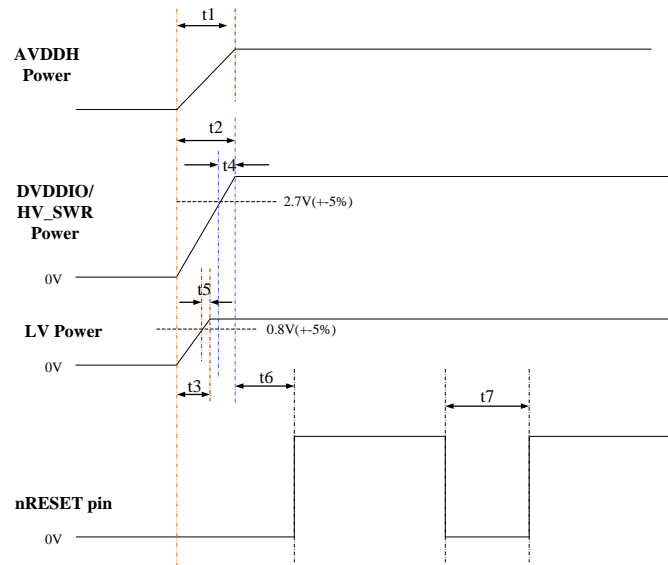


Figure 22. Power and Reset Characteristics

Table 28. Power and Reset Characteristics

Parameter	SYM	Description/Condition	Type	Min	Typical	Max	Units
AVDDH Rising Time	t1	AVDDH power rise settling time	I	0.5	-	-	ms
HV Power Rising Time	t2	DVDDIO, HV_SWR(If embedded SWR be used) power rise settling time	I	0.5	-	-	ms
LV Power Rising Time	t3	DVDDL and AVDDL power rise settling time	I	0.1	-	-	ms
HV Power Ready Time after more than HV POR threshold	t4	The duration from HV power more than HV POR threshold to HV power ready	I	-	-	10	ms
LV Power Ready Time after more than LV POR threshold	t5	The duration from LV power more than LV POR threshold to LV power ready	I	-	-	10	ms
Reset Delay Time	t6	The duration from 'all power steady' to the reset signal released to high	I	10	-	-	ms
Reset Low Time	t7	The duration of reset signal remaining low time before issuing a reset to RTL8213B	I	10	-	-	ms

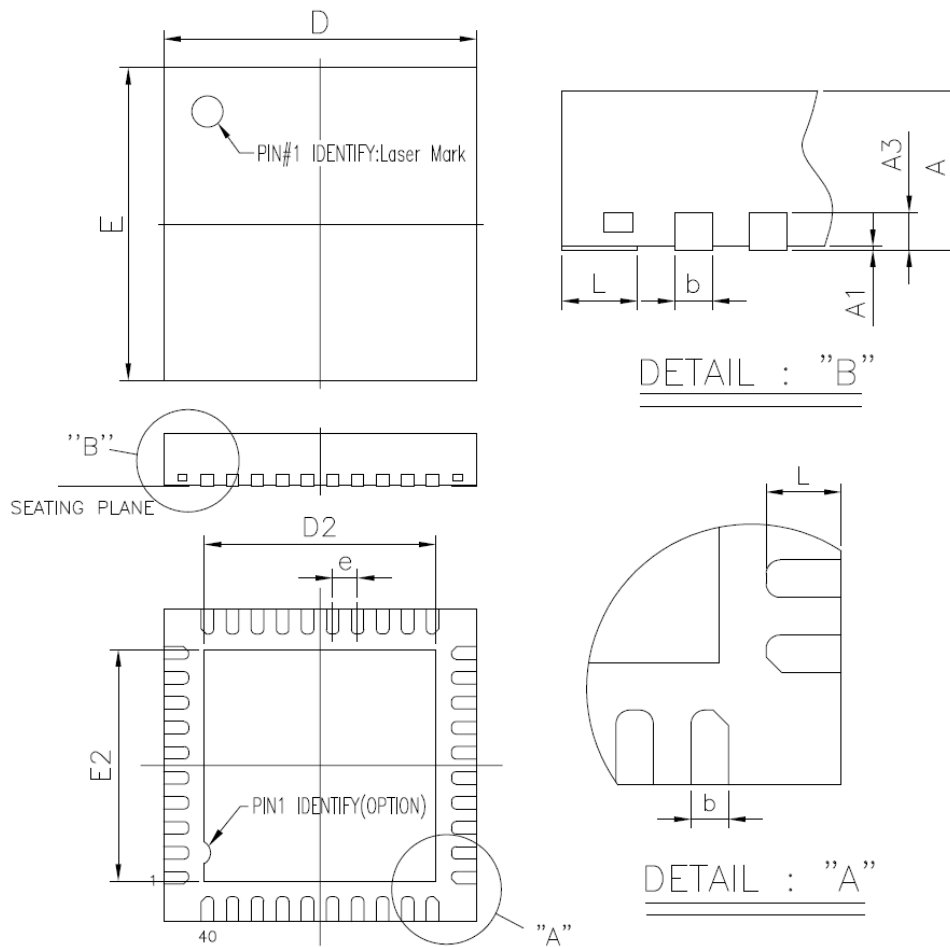
Note 1: If the powers supply voltage of the RTL8213B lower than normal operation condition happened, the Power On Reset (POR) or Pin Reset is needed for normal operation of the RTL8213B.

Note 2: DVDDIO power must be ready no later than HV_SWR power if embedded SWR be used.

Note 3: AVDDH power must be ready no later than DVDDIO power.

12. Mechanical Dimensions

Plastic Quad Flat No Lead Package 40 Leads 5x5mm² Outline



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E	5.00 BSC			0.197 BSC		
D2/E2	3.45	3.70	3.75	0.136	0.146	0.147
e	0.40 BSC			0.016 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020

Notes :

1. CONTROLLING DIMENSION : MILLIMETER(mm).
2. REFERENCE DOCUMENTL : JEDEC MO-220.

13. Ordering Information

Table 29. Ordering Information

Part Number	Package	Status
RTL8213B-CG	QFN 40-Pin 'Green' Package	Mass Production

Note: See page 7 for package identification.

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[KSZ8061MNXI](#) [KSZ8061RNBW](#) [KSZ8462FH LI](#) [KSZ9031RN XCC](#) [KSZ9031RN XIC](#) [KSZ8081RNDIA-TR](#) [KSZ8091RNAIA TR](#)
[KSZ9897RTXC](#)