RTL8812BU

Single-Chip 802.11a/b/g/n/ac 2T2R WLAN with USB3.0 Interface

DATASHEET

(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
0.1	2015/10/15	Preliminary release.
0.2	2015/10/19	1.) Modify RF-related pin description 2.) Modify Mechanical Dimensions
0.3	2015/10/20	Modify general description and features
0.4	2015/03/29	1.) Modify the RF block diagram 2.) Modify the RF pin description

Notice:

This Data Sheet is the preliminary release for the product specification reference. The specification will be adjusted by the actual product specification and function in the mass production without further notice.

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1. General Description

The Realtek RTL8812BU is a highly integrated single-chip that support 2-stream 802.11ac solutions with Multi-user MIMO (Multiple-Input, Multiple-Output) with Wireless LAN (WLAN) USB3.0 network interface controller .It combines a WLAN MAC, a 2T2R capable WLAN baseband, and RF in s single chip. The RTL8812BU provides a complete solution for a high-performance integrated wireless device.

The RTL8812BU baseband implements Multi-user Multiple Input, Multiple Output (MU-MIMO) Orthogonal Frequency Division Multiplexing (OFDM) with two transmit and two receive paths (2T2R). Features include two spatial stream transmissions, short Guard Interval (GI) of 400ns, spatial spreading, and support for variant channel bandwidth. Moreover, RTL8812B provides one spatial stream space-time block code (STBC), Transmit Beamforming (TxBF) and Low Density Parity Check (LDPC) to extend the range of transmission. At the receiver, extended range and good minimum sensitivity is achieved by having receiver diversity up to 2 antennas. As the recipient, the RTL8812BU also supports explicit sounding packet feedback that helps senders with beamforming capability.

For legacy compatibility, Direct Sequence Spread Spectrum (DSSS), Complementary Code Keying (CCK) and OFDM baseband processing are included to support all IEEE 802.11b, 802.11g and 802.11a data rates. Differential phase shift keying modulation schemes, DBPSK and DQPSK with data scrambling capability are available, and CCK provides support for legacy data rates, with long or short preamble. The high speed FFT/IFFT paths, combined with BPSK, QPSK, 16QAM, 64QAM and 256QAM modulation of the individual subcarriers, and rate compatible coding rate of 1/2, 2/3, 3/4, and 5/6, provide up to 866.7Mbps for IEEE 802.11ac MIMO OFDM.

The RTL8812BU builds in an enhanced signal detector, an adaptive frequency domain equalizer, and a soft-decision Viterbi decoder to alleviate severe multi-path effects and mutual interference in the reception of multiple streams. For better detection quality, receive diversity with Maximal-Ratio-Combine (MRC) applying up to two receive paths is implemented.

Receive vector diversity for multi-stream application is implemented for efficient utilization of the MIMO channel. Efficient IQ-imbalance, DC offset, phase noise, frequency offset, and timing offset compensations are provided for the radio frequency front-end.

The RTL8812BU supports fast receiver Automatic Gain Control (AGC) with synchronous and asynchronous control loops among antennas, antenna diversity functions, and adaptive transmit power control functions to obtain better performance in the analog portions of the transceiver.

The RTL8812BU MAC supports 802.11e for multimedia applications, 802.11i and WAPI (Wireless Authentication Privacy Infrastructure) for security, and 802.11n/802.11ac for enhanced MAC protocol efficiency. Using packet aggregation techniques such as A-MPDU with BA and A-MSDU, protocol efficiency is significantly improved. Power saving mechanisms such as Legacy Power Save, U-APSD, and MIMO power saving reduce the power wasted during idle time, and compensate for the extra power required to transmit MIMO OFDM.

2. Features

General

- TFBGA 6.5x6.5mm package
- CMOS MAC, Baseband PHY and RF in a single chip for IEEE 802.11a/b/g/n/ac compatible WLAN
- Support 802.11ac 2x2,Wave-2 compliant with MU-MIMO
- Complete 802.11n MIMO solution for 2.4GHz and 5GHz band
- Maximum PHY data rate up to 173.3Mbps using 20MHz bandwidth, 400Mbps using 40MHz bandwidth, and 866.7Mbps using 80MHz bandwidth.
- Backward compatible with 802.11a/b/g devices while operating at 802.11n data rates
- Backward compatible with 802.11a/n devices while operating at 802.11ac data rates.

Host Interface

- Complies with USB3.0 for WLAN controller
- USB LPM and USB Selective Suspend supported

Standards Supported

- IEEE 802.11a/b/g/n/ac compatible WLAN
- IEEE 802.11e QoS Enhancement (WMM)
- IEEE 802.11i (WPA, WPA2). Open, shared key, and pair-wise key authentication services
- IEEE 802.11h DFS, TPC, Spectrum Measurement
- IEEE 802.11k Radio Resource Measurement
- WAPI (Wireless Authentication Privacy Infrastructure) certified

MAC Features

- Frame aggregation for increased MAC efficiency (A-MSDU, A-MPDU)
- Low latency immediate Block Acknowledgement (BA)
- Long NAV for media reservation with CF-End for NAV release
- PHY-level spoofing to enhance legacy compatibility
- MIMO power saving mechanism
- Channel management
- Multiple BSSID feature allows the RTL8822B to assume multiple MAC identities when used as a wireless bridge
- Transmit Opportunity (TXOP) Short Inter-Frame Space (SIFS) bursting for higher multimedia bandwidth
- WiFi Direct supports wireless peer to peer applications.

Other Features

- Supports Wake-On-WLAN via Magic Packet and Wake-up frame
- Transmit Beamforming

Peripheral Interfaces

- Up to 15 General Purpose Input/Output pins
- Generates 40MHz clock for peripheral chip.

PHY Features

- IEEE 802.11ac MIMO OFDM
- IEEE 802.11n MIMO OFDM
- Two Transmit and Two Receive paths
- 5MHz / 10MHz / 20MHz / 40MHz / 80MHz bandwidth transmission
- Support 2.4Ghz and 5Ghz band channels
- Short Guard Interval (400ns)
- Sounding packet.
- DSSS with DBPSK and DQPSK, CCK modulation with long and short preamble
- OFDM with BPSK, QPSK, 16QAM, 64QAM and 256QAM modulation. Convolutional Coding Rate: 1/2, 2/3, 3/4, and 5/6
- CCA on secondary through RTS/CTS handshake.
- Support TCP/UDP/IP checksum offload
- Single external power source 3.3V only
- Maximum data rate 54Mbps in 802.11g, 300Mbps in 802.11n and 866.7bps in 802.11ac.
- OFDM receive diversity with MRC using up to 2 receive paths. Switch diversity used for DSSS/CCK
- Support STBC
- Support LDPC
- Hardware antenna diversity
- Fast receiver Automatic Gain Control (AGC)
- On-chip ADC and DAC
- Build-in both 2.4GHz and 5GHz PA
- Build-in both 2.4GHz and 5GHz LNA

3. Application Diagrams

3.1. 11ac Dual-Band 2x2 RF Application

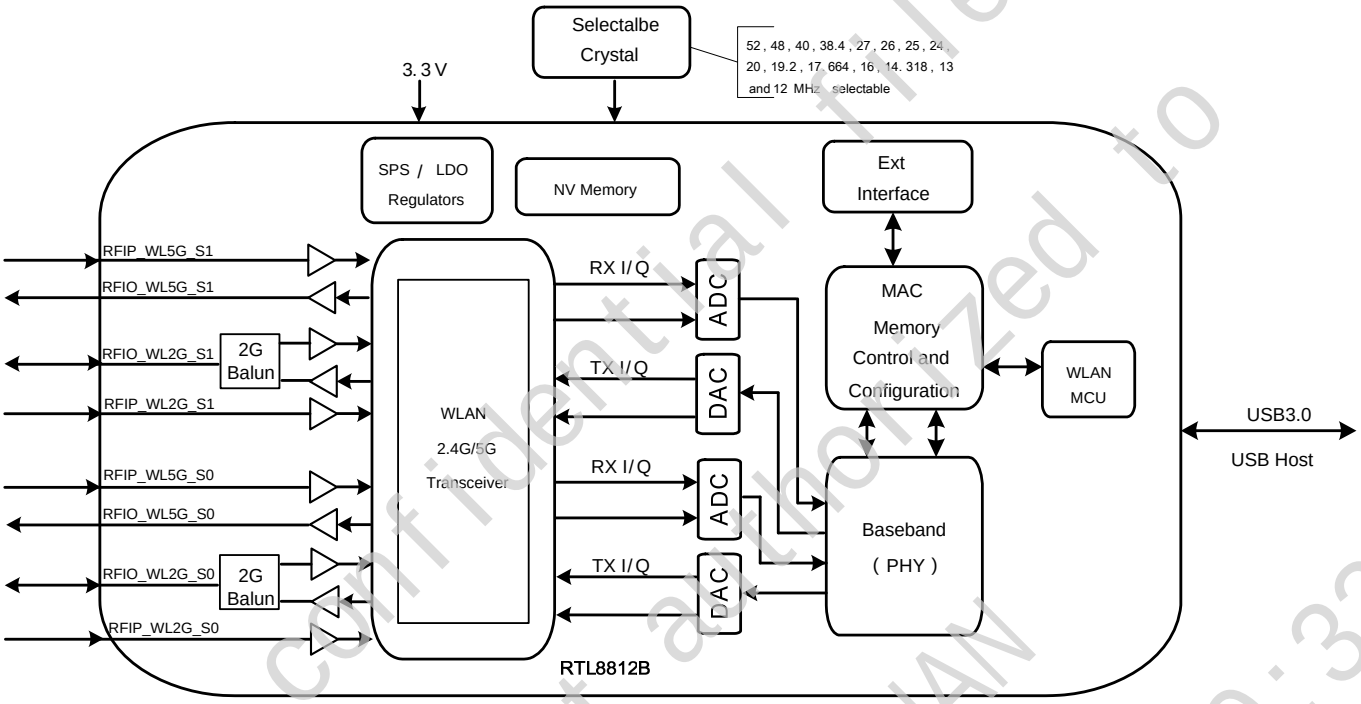


Figure 1. Dual-Band MIMO 2x2 Solution(11ac 2x2 MAC/BB/RF+PA) Solution --- RTL8812B

4. TFPGA Ball Assignments

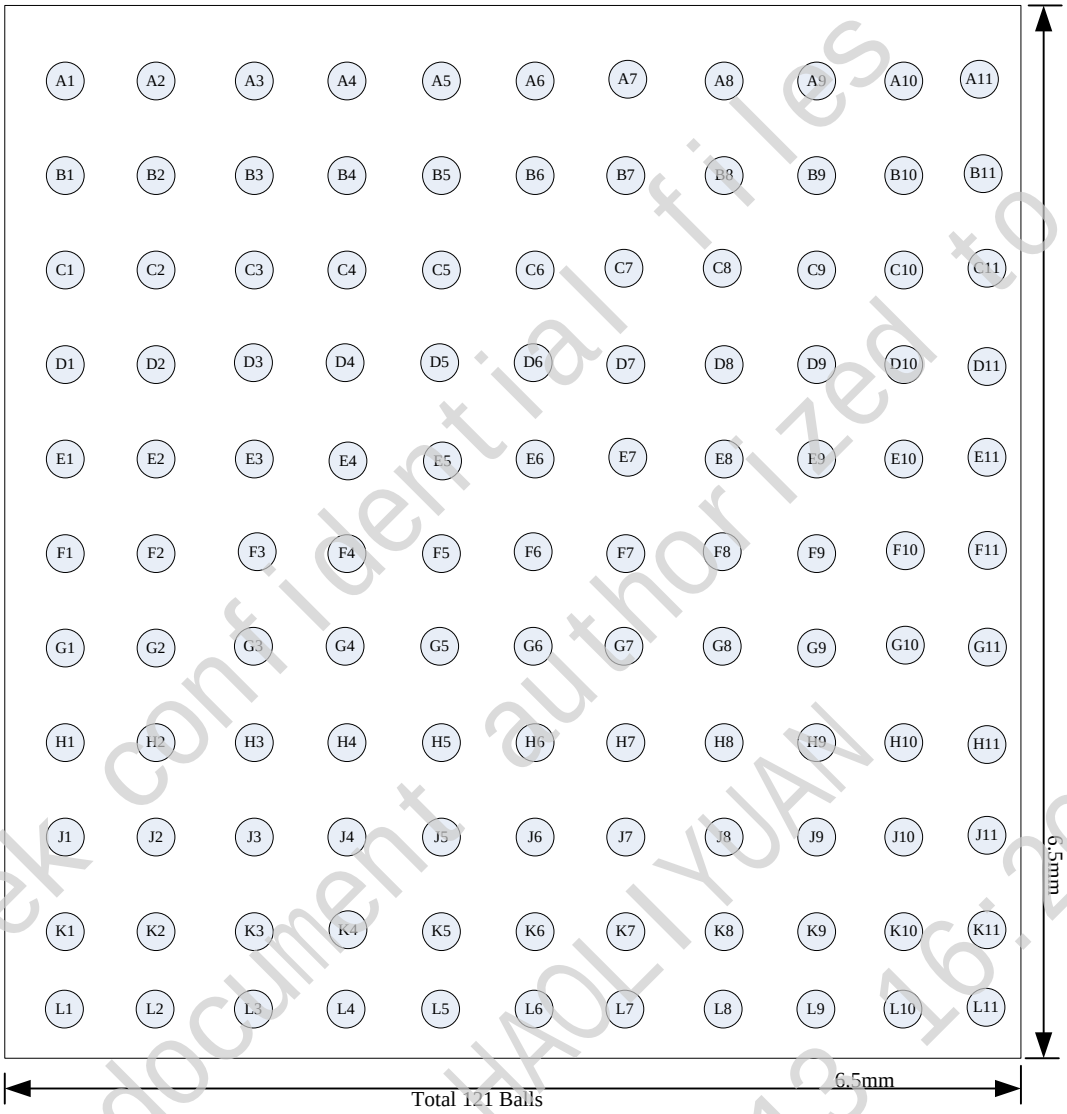


Figure 2. TFBGA Ball Assignments

4.1. Package Identification

Green package is indicated by a 'G' in the location marked 'T' in Figure2..

5. Ball Descriptions

The following signal type codes are used in the tables:

I:	Input	O:	Output
T/S:	Tri-State bi-directional input/output pin	S/T/S:	Sustained Tri-State
O/D:	Open Drain	P:	Power pin
N/A:	No Bonding pin		

5.1. Power On Trap Pin

Table 1. Power-On Trap Pins

Symbol	Type	Ball No	Description
TEST_MODE_SEL	I	H7	Shared with GPIO4 0: Normal operation mode 1: Test/debug mode
SPS_LDO_SEL	I	J9	Shared with GPIO5 0: Internal switching regulator select 1: Internal LDO select
EEPROM_SEL	I	J10	Shared with EESK pin 0: Internal NV memory select 1: External EEPROM select

5.2. USB 3.0 Transceiver Interface

Table 2. USB 3.0 Transceiver Interface

Symbol	Type	Ball No	Description
HSIP/HSIN	I	B11,C11	USB 3.0 Receive Differential Pair
HSOP/HSON	O	D11,E11	USB 3.0 Transmit Differential Pair
HSDP/HSDM	I/O	A11,A10	USB 2.0 Transceiver Differential Pair

5.3. EEPROM Interface

Table 3. EEPROM Interface

Symbol	Type	Ball No	Description
EECS	O	C9	External EEPROM Chip Select
EESK	O	J10	External EEPROM Clock

5.4. RF Interface

Table 4. RF Interface

Symbol	Type	Ball No	Description
BT RFIO	I/O	A2	BT RF I/O
RFIP_WL5G_S1	I	C1	WLAN 5G RF input
RFIO_WL5G_S1	O	D1	WLAN 5G RF output
RFIO_WL2G_S1	I/O	F1	WLAN 2G RF input/output
RFIP_WL2G_S1	I	G1	WLAN 2G RF input (efuse configuration needed)
RFIP_WL5G_S0	I	H1	WLAN 5G RF input
RFIO_WL5G_S0	O	J1	WLAN 5G RF output
RFIO_WL2G_S0	I/O	L1	WLAN 2G RF input/output
RFIP_WL2G_S0	I	L2	WLAN 2G RF input (efuse configuration needed)
S1_TSSI	I	D5	TSSI input from external PA
S0_PAPE_5G	I	G6	GPIO for RF switch control. (refer to HDK for actual assignment)
ANTSW	O	D4	GPIO for RF switch control. (refer to HDK for actual assignment)
ANTSWB	O	E4	GPIO for RF switch control. (refer to HDK for actual assignment)
S1_PAPE_2G	O	E5	GPIO for RF switch control. (refer to HDK for actual assignment)
S1_PAPE_5G	O	D6	GPIO for RF switch control. (refer to HDK for actual assignment)
S1_TRSW	O	F6	GPIO for RF switch control. (refer to HDK for actual assignment)
S1_TRSWB	O	F5	GPIO for RF switch control. (refer to HDK for actual assignment)
S0_TSSI	I	G5	TSSI input from external PA
S0_PAPE_2G	O	H5	GPIO for RF switch control. (refer to HDK for actual assignment)
S0_TRSW	O	K7	GPIO for RF switch control. (refer to HDK for actual assignment)

5.5. LED Interface

Table 5. LED Interface

Symbol	Type	Ball No	Description
LED2	O	E7	LED Pin (Active Low), shared with GPIO8

5.6. Power Management Handshake Interface

Table 6. Power Management Handshake Interface

Symbol	Type	Ball No	Description
CHIP_EN	I	F9	This Pin Can Externally Shutdown the RTL8812BU (No Extra Power Switch Required). When this function is not required, external pull high is required.
WL_DIS#	I	C8	Shared with GPIO9. This pin can externally shut down the RTL8812BU WLAN function when WL_DIS# is pulled low. This pin can also be configured as the WLAN Radio-off function with host interface remaining connected.

5.7. Clock and Other Pins

Table 7. Clock and Other Pins

Symbol	Type	Ball No	Description
XI	I	L5	40MHz OSC Input 40MHz crystal reference clock input
XO	O	L6	40MHz Crystal reference clock output
GPIO0	IO	J8	General Purpose Input/Output Pin
GPIO1	IO	H8	General Purpose Input/Output Pin
GPIO2	IO	H9	General Purpose Input/Output Pin
GPIO3	IO	H10	General Purpose Input/Output Pin
GPIO4	IO	H7	General Purpose Input/Output Pin
GPIO5	IO	J9	General Purpose Input/Output Pin
GPIO6	IO	D7	General Purpose Input/Output Pin
GPIO7	IO	D8	General Purpose Input/Output Pin
GPIO8	IO	E7	General Purpose Input/Output Pin
GPIO9	IO	C8	General Purpose Input/Output Pin
GPIO12	IO	D9	General Purpose Input/Output Pin
GPIO13	IO	D10	General Purpose Input/Output Pin
GPIO14	IO	E9	General Purpose Input/Output Pin
RSVD		F11, G11,F7,F8, G7,G8	Reserved

5.8. Power Pins

Table 8. Power Pins

Symbol	Type	Ball No	Description
LX_SPS	P	K10,K11	Switching Regulator Output
VD33_SPS	P	L11	Switching Regulator Input Or Linear Regulator input from 3.3V to 1.5V
VD33_IO	P	L10	VDD3.3V for Digital IO
VD33_IO	P	A7	VDD3.3V for Digital IO
VDD_IO_2	P	L8	VDD for GPIO0 to GPIO5 and EESK
VDD_IO_1	P	B7	VDD for GPIO6,GPIO7,GPIO9,GPIO11,GPIO12 and EECS.
VD10D_WL	P	H11	1.05V for WLAN digital power
VD10D_FB_WL	P	L9	1.05V for WLAN digital power
GND_SPS	P	J11	Switching Regulator Ground
GND_HCI	P	B10	Ground for host interface
RREF	P	A9	Precision Resistor for Bandgap
VD1_VDDTX/ VD1_VDDRX	P/I	C10,B9	1.05V for analog circuits in interface
V33_USB	P	A8	3.3V for USB
VD1_USB	P	B8	1.05V for USB
GND_CORE	P	B6,C6,G10,G9, K8,K9	Digital GND
VD1_RF_WLS1	P	B1	VDD 1.05V for WLAN RF
VD33_PA_WLS1	P	E1	VDD 3.3V for WLAN PA
VD33_PAD_WLS1	P	E2	VDD 3.3V for WLAN PAD
VD1_RF_WLS0	P	G2	VDD 1.05V for WLAN RF
VD33_PA_WLS0	P	K1	VDD 3.3V for WLAN PA
VD33_PAD_WLS0	P	J2	VDD 3.3V for WLAN PAD
GND_RF1_WL	P	C2,C3	Ground of WLAN RF
GND_RF2_WL	P	D2,D3,E3,F2,F3, F4,G4	Ground of WLAN RF
GND_RF3_WL	P	G3	Ground of WLAN RF
GND_RF4_WL	P	H2,H3,H4,J3,J4, K2K3	Ground of WLAN RF
VD1_SYN_WL	P	L3	VDD 1.05V for WLAN SYN
VD33_SYN_WL	P	L4	VDD 3.3V for WLAN SYN
GND_SYN_WL	P	K4	Ground for WL synthesizer
VD1_AFE_WL	P	L7	VDD 1.05V for WLAN AFE
GND_AFE_WL	P	J6,J7	Ground for WLAN AFE
VD33X	P	K6	VDD 3.3V for Crystal
GND_XTAL	P	K5	Ground for Crystal
CAP_XTAL	P	J5	LDO output . External CAP 1uF is needed.

6. Electrical and Thermal Characteristics

6.1. Temperature Limit Ratings

Table 9. Temperature Limit Ratings

Parameter	Minimum	Maximum	Units
Storage Temperature	-55	+125	°C
Ambient Operating Temperature	0	70	°C
Junction Temperature	0	125	°C

6.2. DC Characteristics

6.2.1. Power Supply Characteristics

Table 10. DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Units
VD33	3.3V I/O Supply Voltage	3.0	3.3	3.6	V
VD10	1.05V Core Supply Voltage	0.945	1.05	1.155	V

6.2.2. Digital IO Pin DC Characteristics

Table 11. 3.3V GPIO DC Characteristics

Symbol	Parameter	Minimum	Normal	Maximum	Units
V_{IH}	Input high voltage	2.0	3.3	3.6	V
V_{IL}	Input low voltage	--	0	0.9	V
V_{OH}	Output high voltage	2.97	--	3.3	V
V_{OL}	Output low voltage	0	--	0.33	V

PS. 3.3V and 1.2V ripple < 100mV

7. Interface Timing Specification

7.1. USB Bus during Power On Sequence

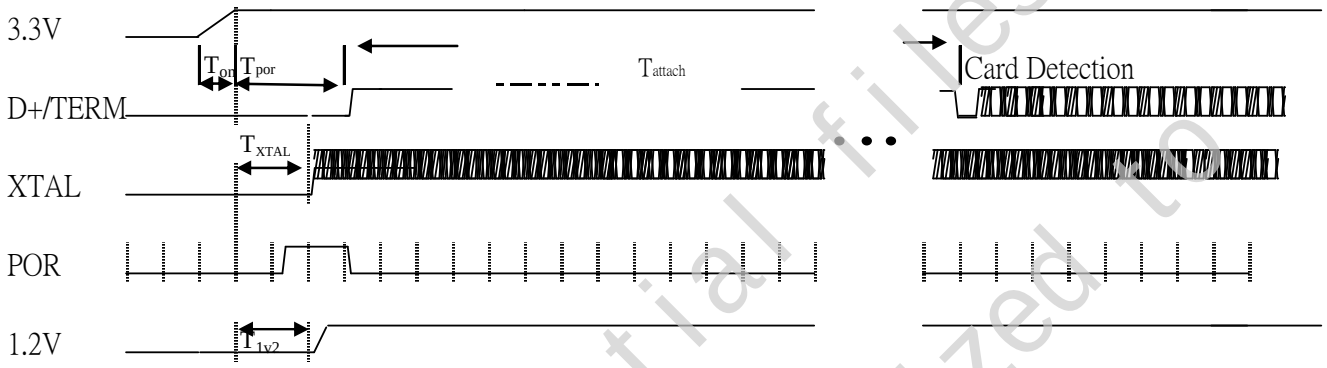


Figure 3. RTL8812BU USB Bus Power On Sequence

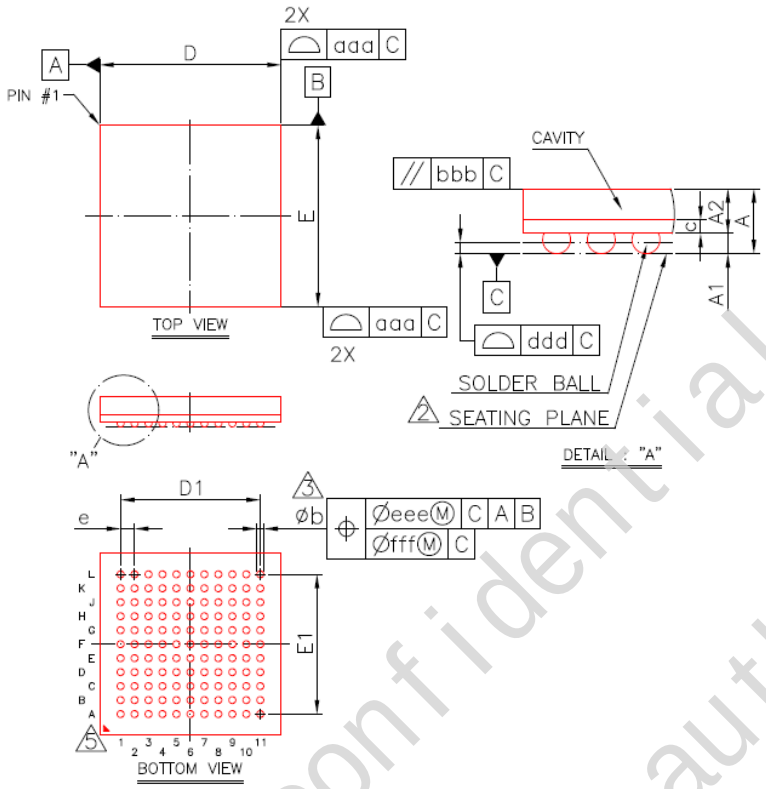
T_{on}: The main power ramp up duration
T_{por}: The power on reset releases and power management unit executes power on tasks
T_{attach}: USB attach state. The duration from resistor attached to USB host starting card detection procedure
T_{xtal}: XTAL starts

The power on flow description:
After main 3.3V ramp up, the internal power on reset is released by power ready detection circuit and the power management unit will be enabled. The power management unit enables the internal regulator and clock circuits.
The power management unit also enables the USB circuits.
USB analog circuits attach resisters to indicate the insertion of the USB device

Table 10. The typical timing range

	Unit	Min	Typical	Max
T_{on}	ms	--	1.5	5
T_{por}	ms	--	2	20
T_{xtal}	ms	--	1.5	8
T_{attach}	ms	100	250	--
T_{1v2}	ms	-	3	11

8. Mechanical Dimensions



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.00	1.07	1.14	0.039	0.042	0.045
A1	0.11	0.16	0.21	0.004	0.006	0.008
A2	0.86	0.91	0.96	0.034	0.036	0.038
c	0.22	0.26	0.30	0.009	0.010	0.012
D	6.40	6.50	6.60	0.252	0.256	0.260
E	6.40	6.50	6.60	0.252	0.256	0.260
D1	---	5.00	---	---	0.197	---
E1	---	5.00	---	---	0.197	---
e	---	0.50	---	---	0.020	---
b	0.20	0.25	0.30	0.008	0.010	0.012
aaa		0.15			0.006	
bbb		0.10			0.004	
ddd		0.08			0.003	
eee		0.15			0.006	
fff		0.05			0.002	
MD/ME		11/11				

NOTE :

1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. SPECIAL CHARACTERISTICS C CLASS: bbb,ddd
5. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.

9. Ordering Information

Table 12. Ordering Information

Part Number	Package	Status
RTL8812BU	TFBGA121 , 'Green' Package	To be available

Realtek Semiconductor Corp.
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