 Lead Free Package and Finish

Applications:

- Switch Mode Power Supply(SMPS)
- Uninterruptible Power Supply(UPS)
- Power Factor Correction (PFC)

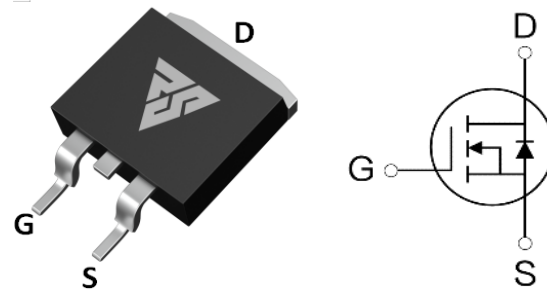
I_D	$R_{DS(ON)}(Typ)$	V_{DSS}
9A	0.95Ω	650V

Features:

- Fast switching speed
- 100% avalanche tested
- Improved dv/dt capability

Ordering Information

Part Number	Package	Marking
RS9N65D	TO-252	RS9N65D



TO-252

Not to Scale

Absolute Maximum Ratings $T_c=25$ unless otherwise specified

Symbol	Parameter	RS9N65D	Units
V_{DSS}	Drain-to-Source Voltage	650	V
I_D	Continuous Drain Current	9	A
I_{DM}	Pulsed Drain Current (Note*1)	36	
PD	Power Dissipation	170	W
VGS	Gate-to-Source Voltage	±30	V
EAS	Single Pulse Avalanche Energy L=10mH VDD=50V RG=25Ω TJ=25	215	mJ
IAS	Avalanche Current (Note*1)	6.2	A
E_{AR}	Repetitive Avalanche Energy (Note*1)	0.84	mJ
TL TPKG	Maximum Temperature for Soldering	300 260	
	Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds		
T_J and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

* Drain Current Limited by Maximum Junction Temperature

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	RS9N65D	Units	Test Conditions
$R_{\theta JC}$	Junction-to-Case	0.7	/ W	Drain lead soldered to water cooled heatsink, PD adjusted for a peak junction temperature of +150
$R_{\theta JA}$	Junction-to-Ambient	62.5		1 cubic foot chamber, free air.

OFF Characteristics $T_J=25^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV _{DSS}	Drain-to-source Breakdown Voltage	650	--	--	V	V _{GS} =0V, I _D =250 μ A
I _{DSS}	Drain-to-Source Leakage Current	--	--	1.0	μ A	V _{DS} =650V, V _{GS} =0V
I _{GSS}	Gate-to-Source Forward Leakage	--	--	100	nA	V _{GS} =30V, V _{DS} =0V
	Gate-to-Source Reverse Leakage	--	--	-100		V _{GS} =-30V, V _{DS} =0V

ON Characteristics $T_J=25^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
R _{DS(on)}	Static Drain-to-Source On-Resistance (Note*2)	--	0.95	1.05	Ω	V _{GS} =10V, I _D =4.5A
V _{GS(TH)}	Gate Threshold Voltage	3.0	--	4.0	V	V _{GS} =V _{DS} , I _D =250 μ A

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
t _{d(ON)}	Turn-on Delay Time	--	43	--	nS	V _{DS} =325V I _D =9A R _G =25 Ω
t _{rise}	Rise Time	--	16.5	--		
t _{d(OFF)}	Turn-OFF Delay Time	--	125	--		
t _{fall}	Fall Time	--	37	--		

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
C _{iss}	Input Capacitance	--	1246	--	pF	V _{GS} =0V V _{DS} =25V f=1.0MHz
C _{oss}	Output Capacitance	--	104	--		
C _{rss}	Reverse Transfer Capacitance	--	0.5	--		
Q _g	Total Gate Charge	--	22	--	nC	V _{DS} =520V I _D =9A V _{GS} =10V
Q _{gs}	Gate-to-Source Charge	--	6	--		
Q _{gd}	Gate-to-Drain("Miller") Charge	--	8	--		

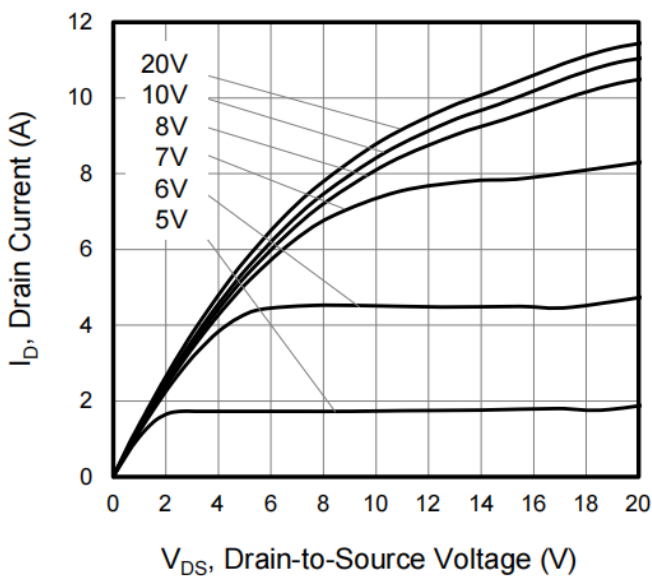
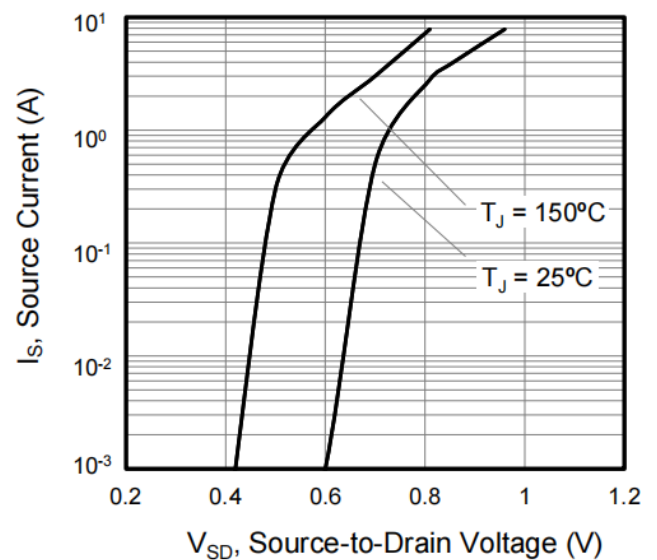
Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I _S	Continuous Source Current	--	--	9	A	Integral pn-diode in MOSFET
I _{SM}	Maximum Pulsed Current	--	--	36	A	
V _{SD}	Diode Forward Voltage	--	--	1.4	V	I _S =5A, V _{GS} =0V
t _{rr}	Reverse Recovery Time	--	360	--	nS	V _{GS} =0V I _S =9A, di/dt=100A/μs
Q _{rr}	Reverse Recovery Charge	--	3.9	--	μC	

Notes:

*1. Repetitive rating; pulse width limited by maximum junction temperature.

*2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 1%

Typical Feature curve
Figure 1. Output Characteristics (T_J = 25°C)

Figure 2. Body Diode Forward Voltage


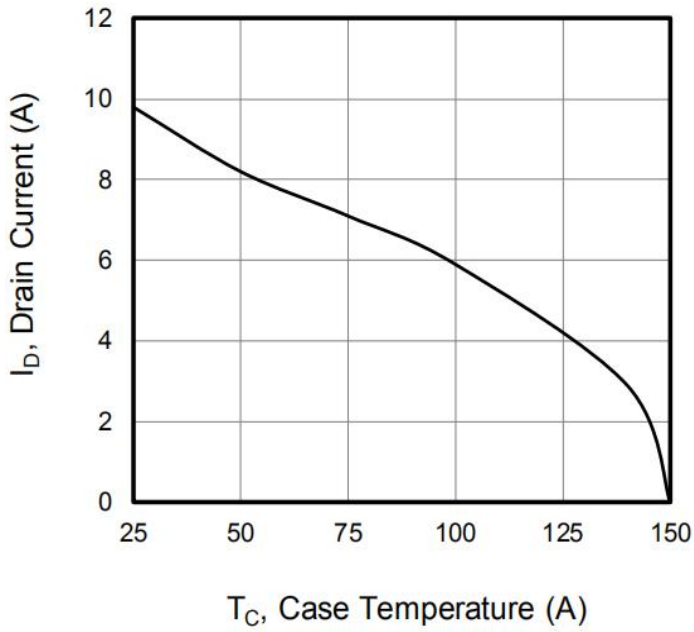


Figure 4. BV_{DSS} Variation vs. Temperature

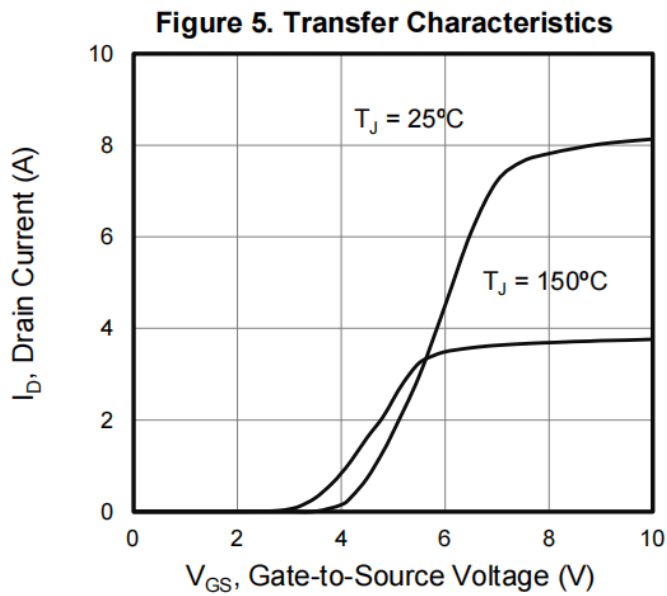
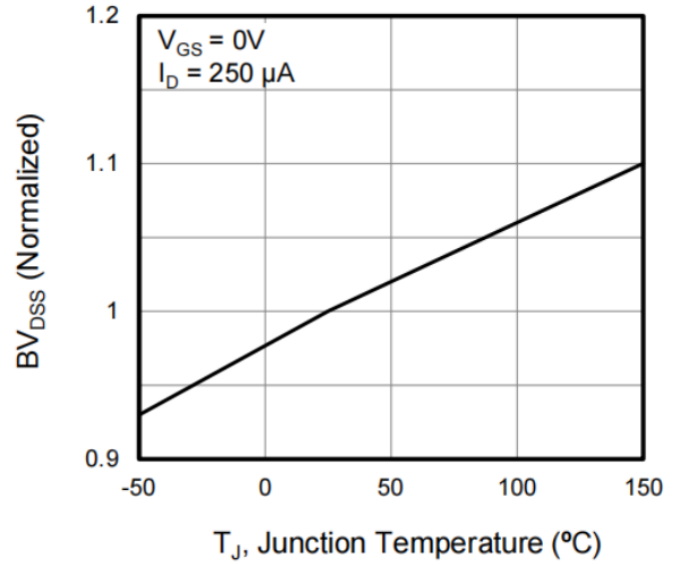


Figure 5. Transfer Characteristics

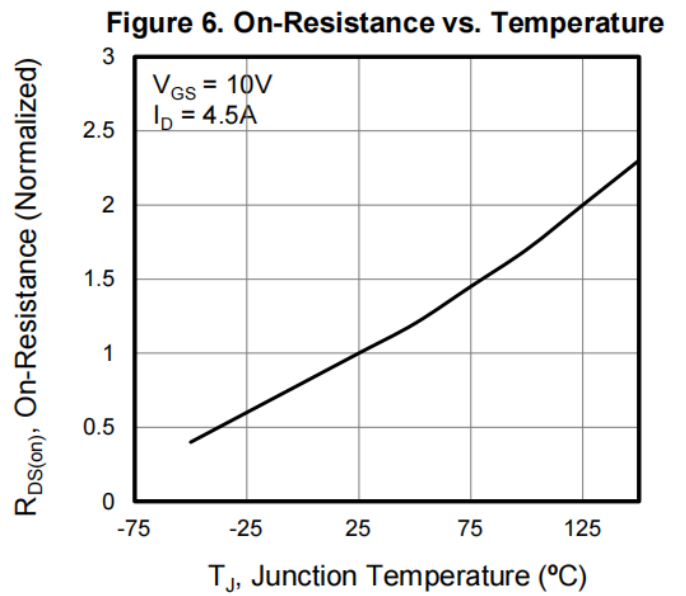


Figure 6. On-Resistance vs. Temperature

Figure 7. Capacitance

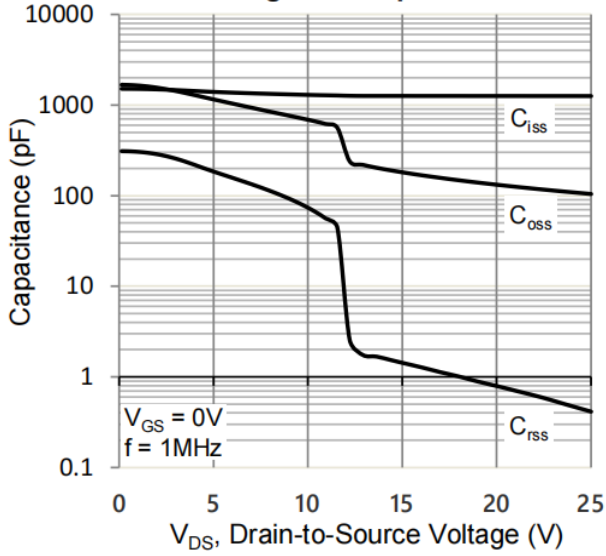


Figure 8. Gate Charge

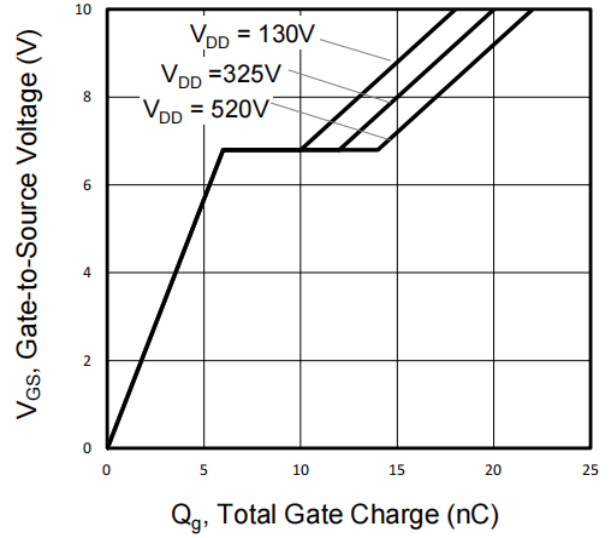
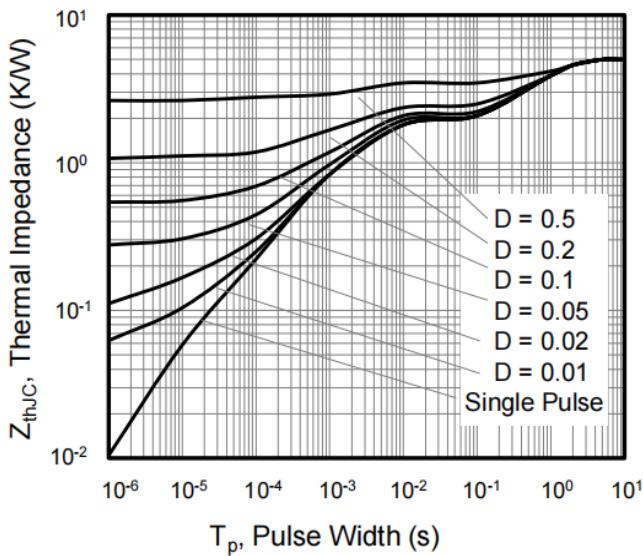


Figure 9. Transient Thermal Impedance



Test Circuits and Waveforms

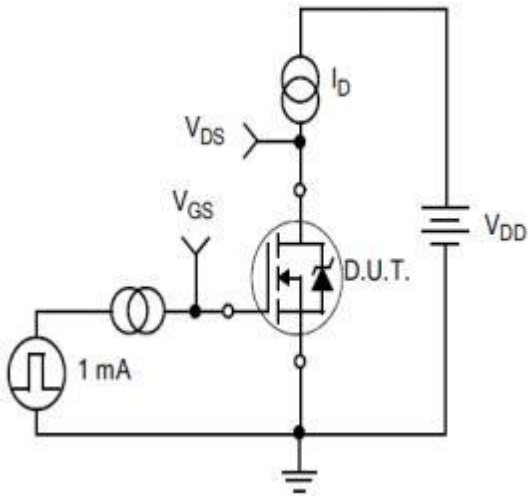


Figure A.
Gate Charge Test Circuit

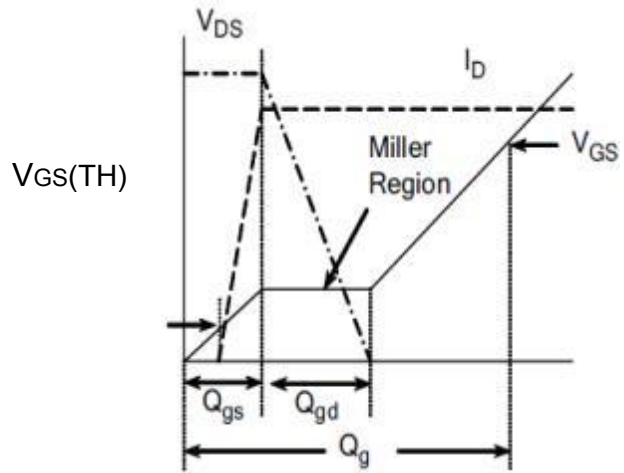


Figure B.
Gate Charge Waveform

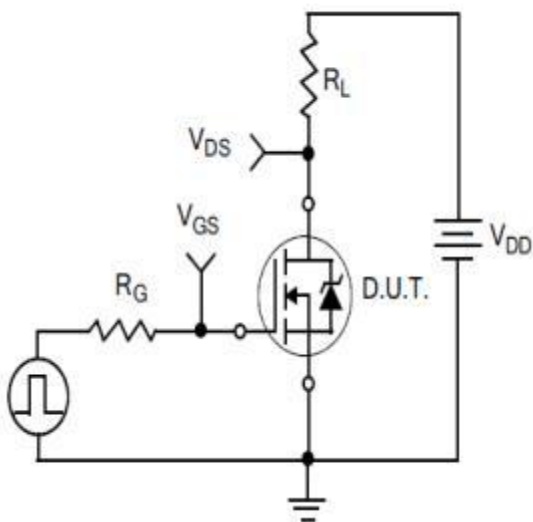


Figure C.
Resistive Switching Test Circuit

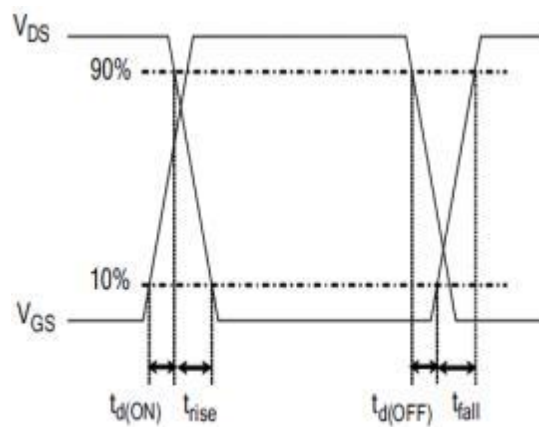


Figure D.
Resistive Switching Waveforms

Test Circuits and Waveforms

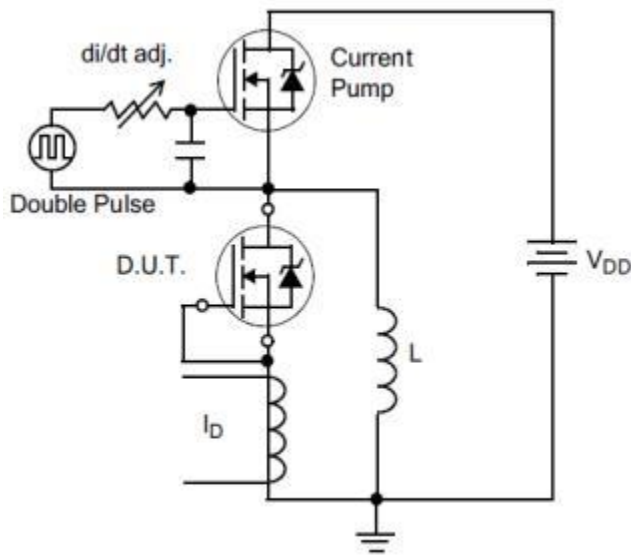


Figure E. Diode Reverse Recovery Test Circuit

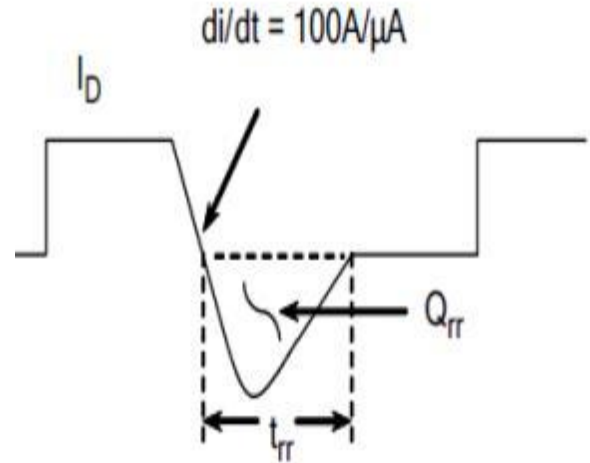


Figure F. Diode Reverse Recovery Waveform

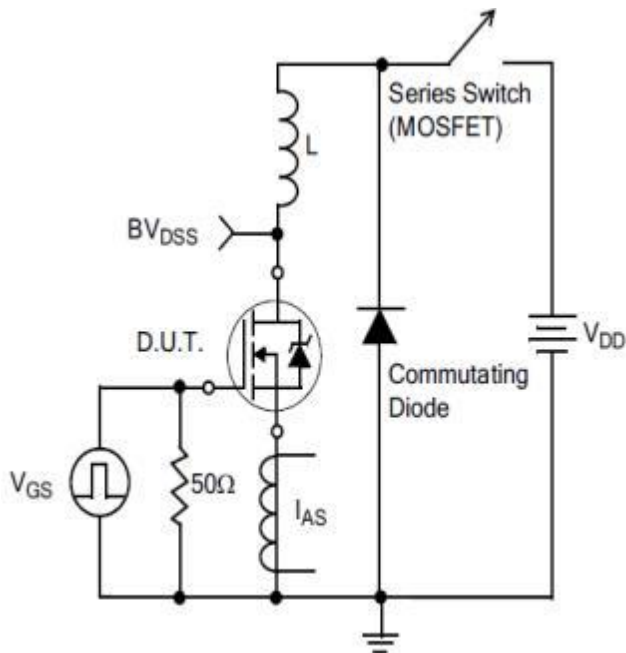
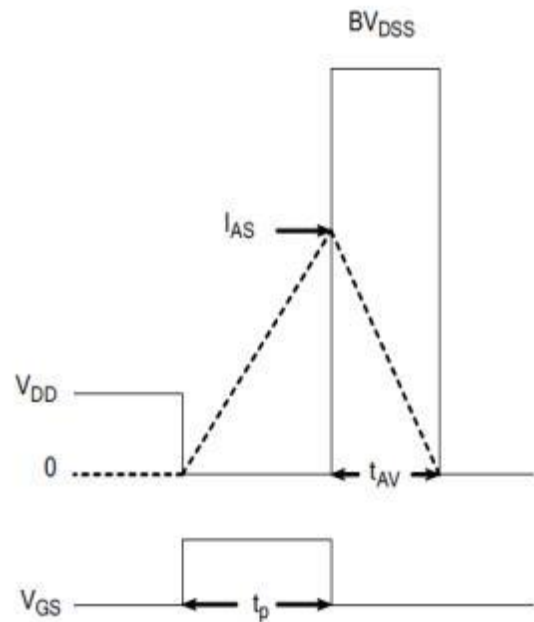


Figure G. Unclamped Inductive Switching Test Circuit

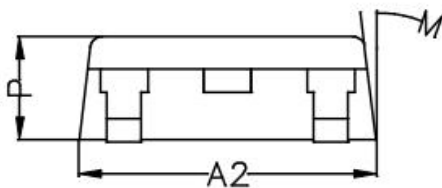
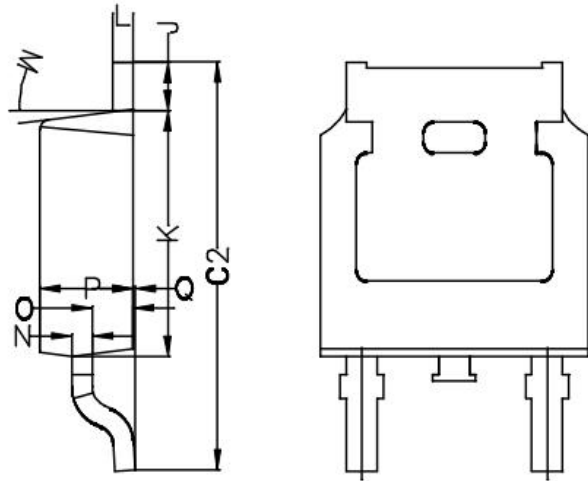
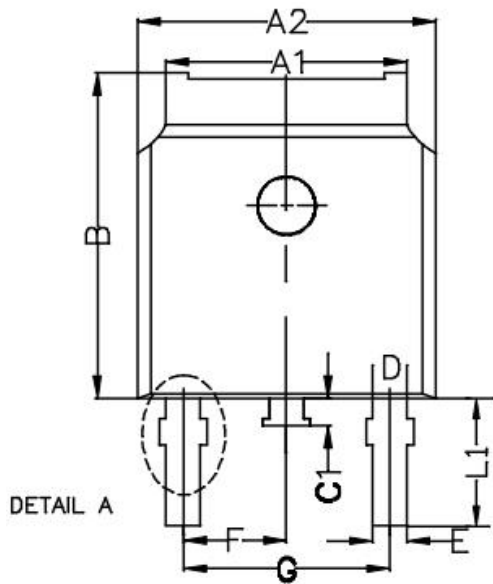


$$E_{AS} = \frac{I_{AS}^2 L}{2}$$

Figure H. Unclamped Inductive Switching Waveforms

Package outline drawing

Unit:mm



Symbol	Min	Non	Max
A1	5.22	5.32	5.42
A2	6.55	6.60	6.65
B	7.05	7.10	7.15
C1	0.70	0.80	0.90
C2	9.70	9.90	10.10
D	1.00 REF.		
E	0.76 REF.		
F	2.286 REF.		
G	4.572 REF.		
J	0.95	1.00	1.05
K	6.05	6.10	6.15
L	0.508 REF.		
L1	2.65	2.80	2.95
M	7° REF.		
N	0.508 REF.		
O	0.96	1.01	1.06
P	2.25	2.30	2.35
Q	0.00	0.05	0.10

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