

RSU12N65F

Multi-Epi Super Junction MOSFETs

Applications:

- •Switch Mode Power Supply(SMPS)
- Uninterruptible Power Supply(UPS)
- •PFC stages for server & telecom
- •Consumer

Features:

- •New revolutionary high voltage technology
- •Better RDS(on) in TO-220F
- •Ultra Low Gate Charge cause lower driving requirements
- •Periodic avalanche rated
- •Ultra low effective capacitances

Ordering Information

Part Number	Package	Marking
RSU12N65F	TO-220F	RSU12N65F

Absolute Maximun Ratings Tc=25°C unless otherwise specified

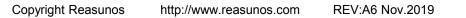
Symbol	Parameter	RSU12N65F	Units
VDSS	Drain-to-Source Voltage	650	V
10	Continuous Drain Current (TC = 25°C)	12	
ID	Continuous Drain Current (TC = 100℃)	7	A
DM	Pulsed Drain Current (Note*1)	44	
PD	Power Dissipation(Tc=25 °C)	31	W
VGS	Gate-to-Source Voltage	±30	V
EAS	Single Pulse Avalanche Engergy (Note*2)	120	mJ
lar	Avalanche Current (Note*1)	1.8	A
Ear	Repetitive Avalanche Engergy (Note*1)	0.32	mJ
	Maximum Temperature for Soldering		
TL TPKG	Leads at 0.063in(1.6mm)from Case for 10 seconds	300 260	°C
	Package Body for 10 seconds		
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

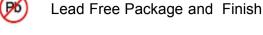
*Drain Current Limited by Maximum Junction Temperature

Caution:Stresses greater than those listed in the "Absolute Maximum Ratings" Table may cause permanent damage to the device.

Thermal Resistance

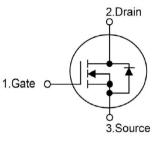
Symbol	Parameter	RSU12N65F	Units	Test Conditions
RθJC	Junction-to-Case	4	°C/W	Drain lead soldered to water cooled heatsink,PD Adjusted for a peak junction temperature of +150℃.
RθJA	Junction-to-Ambient	78		1 cubic foot chamber,free air.





lр	RDS(ON)(Max.)	Vdss
12A	420mΩ	650V







Pb



OFF Characteristics TJ=25 $^\circ\!\!\!\mathrm{C}$ unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
BVDSS	Drain-to-source Breakdown Voltage	650		-	V	VGS = 0V, ID = 250µA, TJ= 25℃
			650		V	VGS = 0V, ID = 250µA, TJ= 150℃
IDSS	Drain-to-Source Leakage Current			1.0	μA	VDS=650V,VGS=0V
IGSS	Gate-to-Source Forward Leakage			100	-	VGS=+30V VDS=0V
	Gate-to-Source Reverse Leakage			-100	nA	VGS=-30V VDS=0V

ON Characteristics TJ=25°C unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
RDS(on)	Static Drain-to-Source On-Resistance		380	420	mΩ	VGS=10V,ID=6A
VGS(TH)	Gate Threshold Voltage	3.5	4	4.5	V	VGS=VDS,ID=250µA
gfs	Transconductance		40		S	VDS=20V,ID=6A

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
td(ON)	Turn-on Delay Time		21			VDS=400V
trise	Rise Time		20			ID=6A
td(OFF)	Turn-OFF Delay Time		51		ns	RG=25Ω
tfall	Fall Time		40			VGS=10V

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
Ciss	Input Capacitance		850			VGS=0V
Coss	Output Capacitance		35		pF	VDS=100V
Crss	Reverse Transfer Capacitance		5			f=1.0MHz
Qg	Total Gate Charge		19			VDS=520V
Qgs	Gate-to-Source Charge		6		nC	ID=12A VGS=10V
Qgd	Gate-to-Drain("Miller")Charge		6			



Source-Drain Diode Characteristics

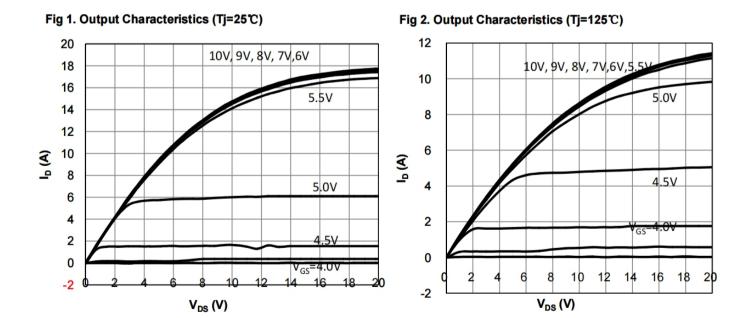
Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
IS	Continuous Source Current			12	А	Integral pn-diode
ISM	Maximum Pulsed Current			44	А	in MOSFET
VSD	Diode Forward Voltage		0.9	1.2	V	IS=12A,VGS=0V Tj=25℃
trr	Reverse Recovery Time		212		nS	VR=400V,VGS=0V
Qrr	Reverse Recovery Charge		2.28		μC	IS=12A,di/dt=100A/µs

Notes:

*1.Repetitive rating; pulse width limited by maximum junction temperature.

*2. IAS = 1.8A, VDD = 50V, RG = 25Ω , Starting TJ = 25° CPulse width tp limited by Tj,max

Typical Feature curve T_J=25℃, unless otherwise noted



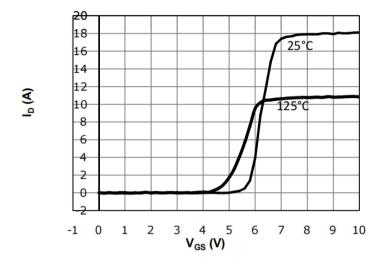
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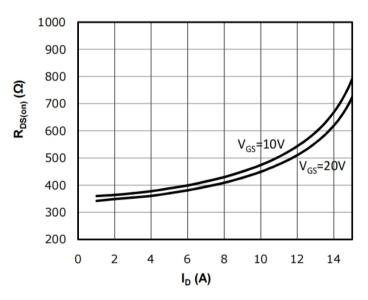
RSU12N65F

Fig 3: Transfer Characteristics

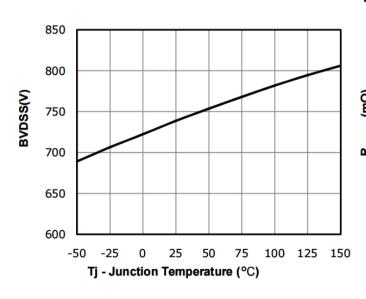
Fig 4: V_{TH} Vs Tj Temperature Characteristics

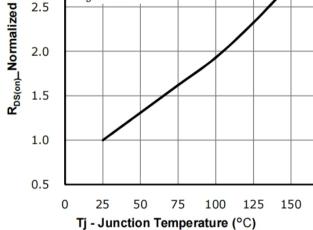


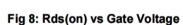


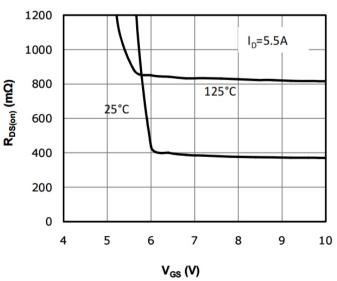














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Fig 6: Rds(on) vs. Temperature

V_{GS}=10V

I_D=5.5A

3.0

2.5

2.0

1.5

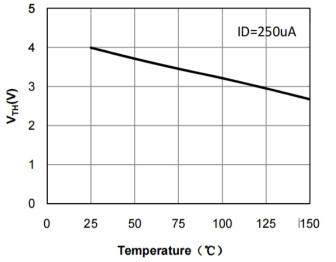
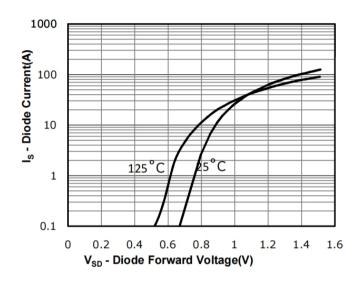
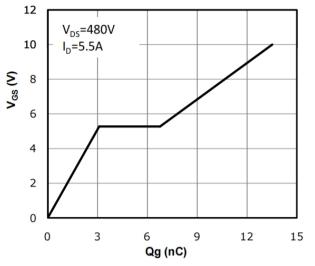


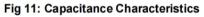


Fig 9: Body-diode Forward Characteristics

Fig 10: Gate Charge Characteristics

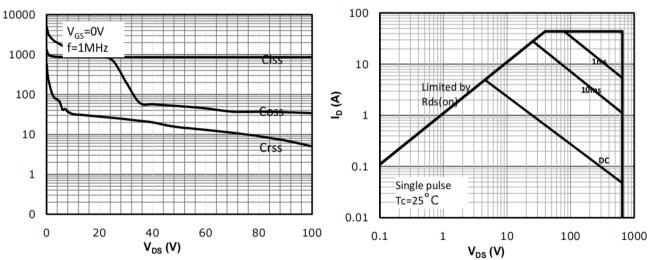






C - Capacitance (PF)

Fig 12: Safe Operating Area





Test Circuits and Waveforms

Figure A: Gate Charge Test Circuit and Waveform

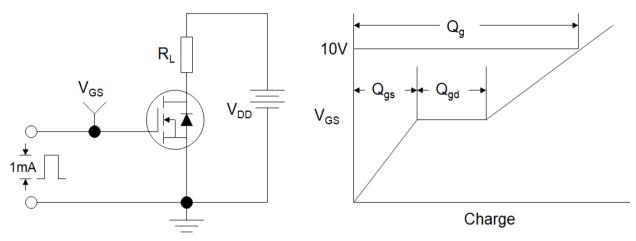


Figure B: Resistive Switching Test Circuit and Waveform

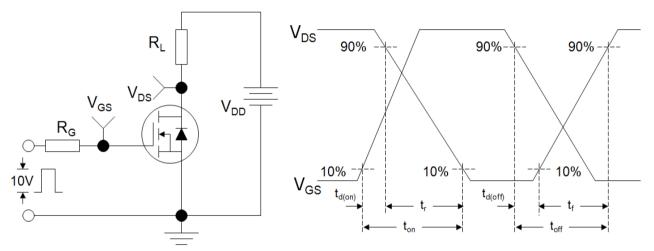
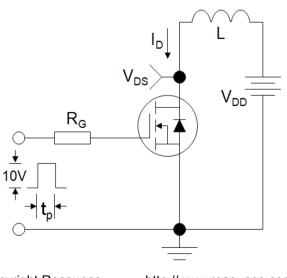
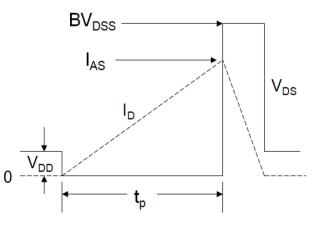


Figure C: Unclamped Inductive Switching Test Circuit and Waveform





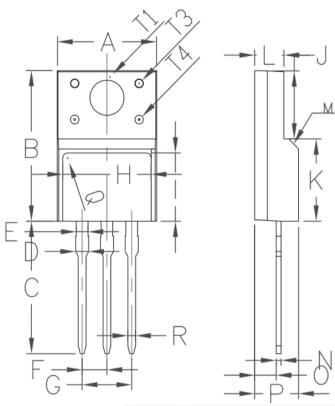
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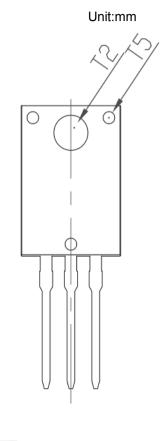
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Package outline drawing





Symbol	Min	Non	Max
A	9.96	10.16	10.36
В	15.67	15.87	16.07
С	13.14	13.34	13.54
D	1.20	1.30	1.40
E		1.20	
F		2.54	
G		5.08	
Н	7.60	7.80	8.00
I	7.10	7.30	7.50
J	6.48	6.68	6.88
K	8.99	9.19	9.39
L	2.34	2.54	2.74
M		45°	
N	0.49	0.50	0.52
0	2.15	2.35	2.55
Р	4.50	4.70	4.90
Q		0.50	
S	4°	4.5°	5°
T1		3.45	
T2		3.18	
T3		1.50	
T4		1.20	
T5		1.50	
R	0.77	0.8	0.83

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