by

XpressGX5LP-QE

Reference Manual

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XpressGX5LP-QE

Reference Manual

Document Change History

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November 2015	2.0.0	P133_v1.0.0	• ReFLEX CES Update
October 2014	1.0.0	P133_v1.0.0	• First release

Proprietary Notice

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Preface

About this Document

This document has been written for design managers, system engineers, and designers of ASICs and FPGAs who are evaluating or using the ReFLEX CES XpressGX5LP-QE board. Prior knowledge of PCI Express is assumed.

Additional Reading

ReFLEX CES periodically updates its documentation. Please contact ReFLEX CES Technical Support or check the Web site at http://www.reflexces.com for current versions.

Please refer to the following documents for information on specification standards:

- *PCI Express™ Specification, Revision 3.0*
- *PCI Express Card Electromechanical Specification, Revision 2.0*

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- the page number to which your comments refer
- a description of your comments

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Chapter 1 Introduction

1.1 Purpose of the Board

The XpressGX5LP-QE board is designed to enable all engineers, even those with little PCI Express experience, to design complex applications using PCIe and 10 Gigabit Ethernet as their main communication interfaces.

The XpressGX5LP-QE is a low-profile, highly-integrated PCI Express FPGA board with quad-10 G or 40 G Ethernet channels engineered for both prototyping and field deployment.

The board is based on the Altera Stratix V GX in the FBGA 1517 package and is available with either the 5SGXEA7K2F40C2N or the 5SGXEA4K2F40C2N FPGA.

1.2 Features List

- PCI Express x8 2.5/5.0/8.0 Gbps (Gen 1, 2 or 3)
  - PCI Express edge connector
- Stratix V GX FPGA
  - 5SGXEA7K2F40C2N or 5SGXEA4K2F40C2N
- Two QSFP+ connectors
  - Up to eight 1G/10G Ethernet or any high-speed link via QSFP+ to SPF+ splitter cable
  - or up to two 40Gbs links
- Board configuration module
  - Power monitoring
    - Power-Up and reset controller
  - IP protection (ReFLEX CES Protocore)
  - FPGA configuration functionality supports
    - Complete FPGA configuration from Flash Devices
    - Flash image boot management
    - FPGA re-load functionality
- PPS interface on MicroBNC connector for time stamping
- Clock circuitry
  - FPGA configuration (Flash): 50 MHz
  - PCIe: 100 MHz
  - DDR3: 200 MHz
  - QSF+/extension interface: 8 similar clocks (max skew=40ps) with 644.53125MHz or I^2C PLL output
- Memories
  - Two 4 GB DDR3L-1333 SDRAM with 72-bit data path (2x8GB capable)
  - 512 MB Flash
  - Two 256Kbit I2C EEPROMs
- Extension Serial link
  - Board capabilities extension or board-to-board connection over SAMTEC LSHM connector
- General I/Os
  - Eight user LEDs
  - Four FPGA configuration LEDs
  - One reset button
  - One FPGA configuration reload button
  - One FPGA image boot selector
  - Three user switches
  - Board-to-board Interface (8 GXB Rx/Tx + 10 LVCMOS)

- Power supply
  - PCI Express edge connector power (12 V and 3.3 V)
    - Power derived directly from PCI Express slot
- Mechanical
  - Low profile PCI Express height

A detailed description of board features can be found in Section 2.3.

1.3 System Requirements

To use XpressGX5LP-QE board features, you must install the **ReFLEX CES Software Tools**. The ReFLEX CES Software Tools can be downloaded from ReFLEX CES's extranet site. You can log in to the extranet from ReFLEX CES's web site www.reflexces.com.

1.4 Board Configuration Requirements

- Altera USB-Blaster
- Altera Quartus 13.0

Chapter 2 XpressGX5LP-QE Architecture

The XpressGX5LP-QE board is supplied by both the 12 V and 3.3 V of the PCI Express slot. The PCI Express 12 V generates 1.35 V, 1.8 V, 2.5 V, and 0.9 V voltages, while the 3.3 V generates 3.0 V voltages.

These voltages are available on the mezzanine power supply daughter card, which is mounted on the XpressGX5LP-QE by default. This daughter card is supplied with the XpressGX5LP-QE board. See Section 3.16 for more information.

The XpressGX5LP-QE is delivered with a fansink mounted on the FPGA.

2.1 XpressGX5LP-QE Layout

The following figure shows the component side of the XpressGX5LP-QE board without the mezzanine power supply daughter card:

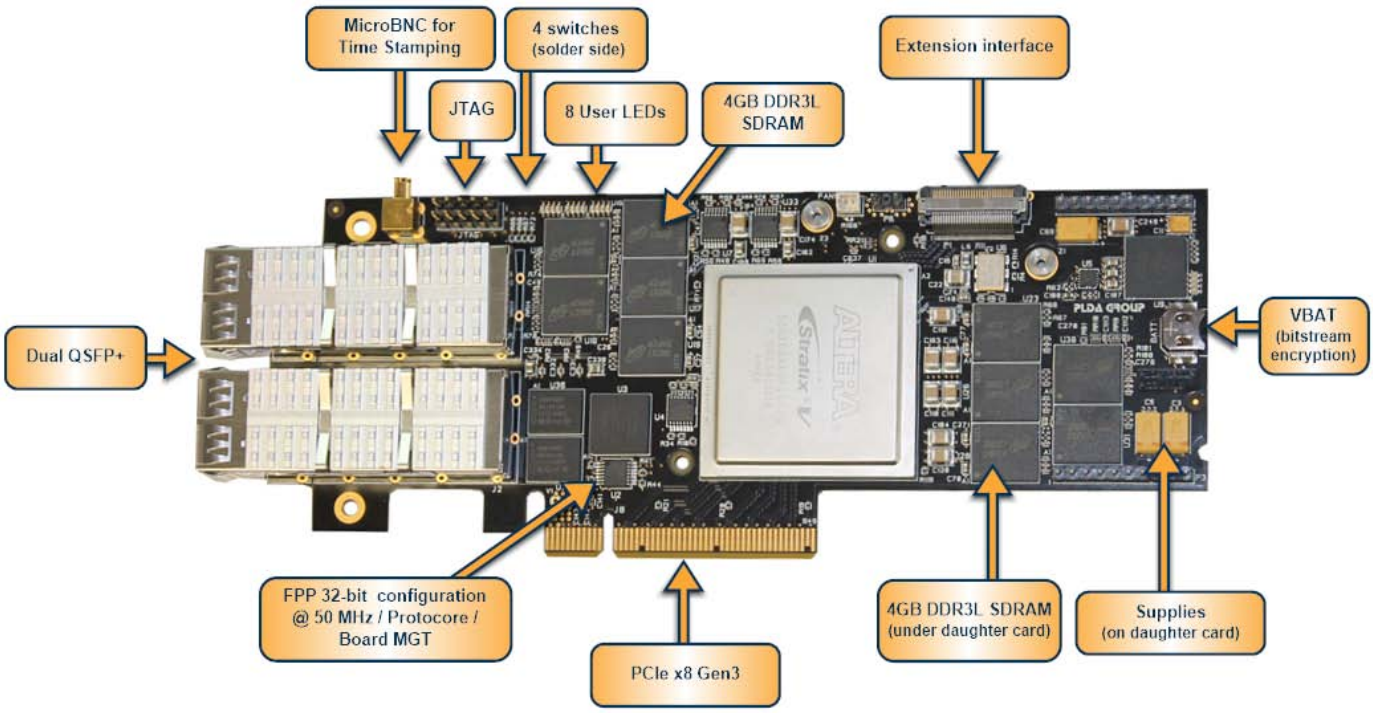


Figure 1: XpressGX5LP-QE layout

2.2 Block Diagram of the Board

The XpressGX5LP-QE board is based on an Altera Stratix V GX FPGA, as shown below:

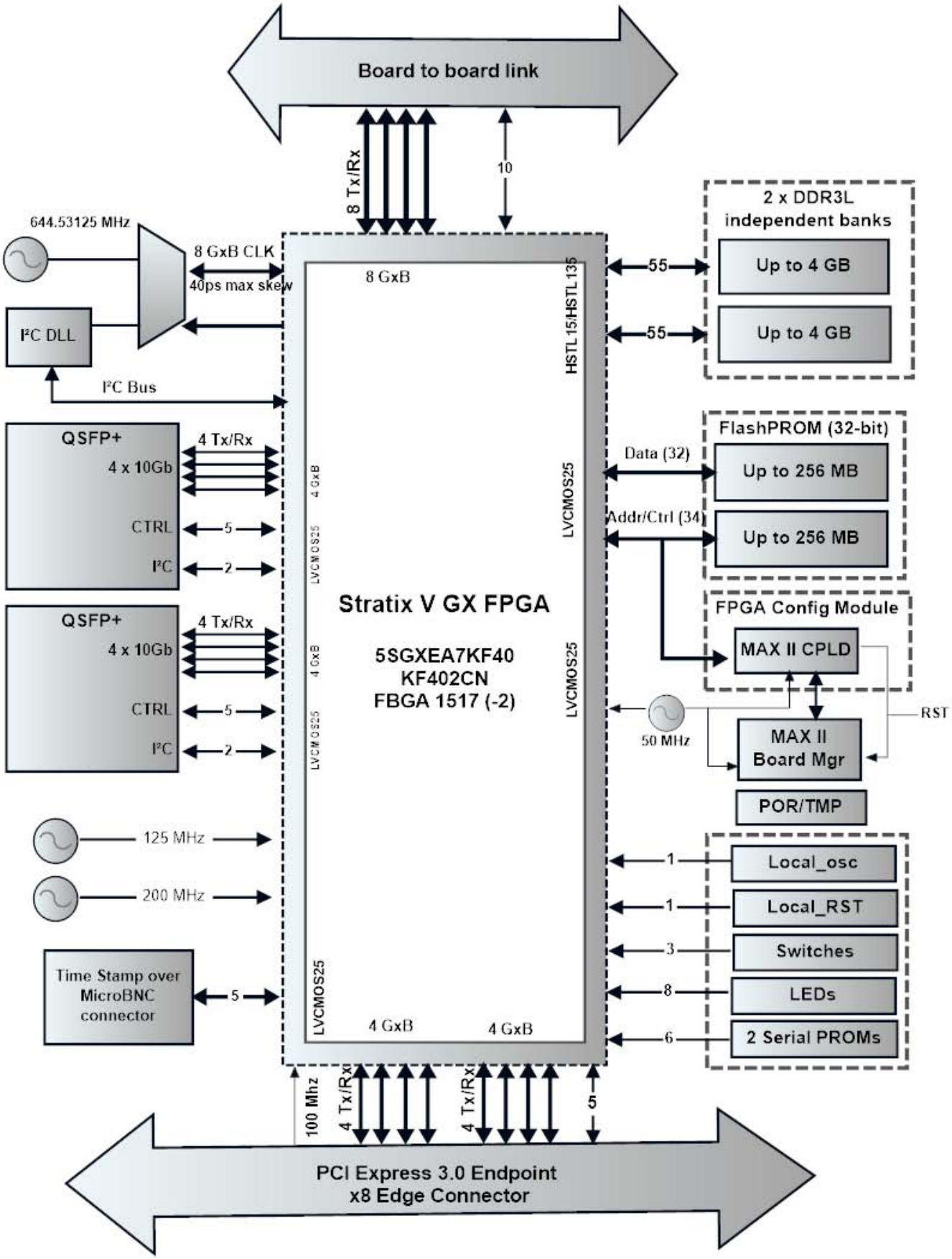


Figure 2: XpressGX5LP-QE block diagram

2.3 Board Features

The following table describes XpressGX5LP-QE board features:

Feature name	Description	For more information, see ...
FPGA configuration module	A 32-bit configuration module (50 MHz) is available to configure the FPGA at each board power-up. This module consists of two 2 Gbit Numonyx Flash devices and an Altera CPLD. The Flash devices can be programmed using ReFLEX CES's FlashPCI software. Each device is directly connected to FPGA pins.	Section 3.2
JTAG connector	The JTAG connector enables FPGA configuration via an Altera USB-Blaster and Quartus.	
Max II Board Manager	This MAX II Board Manager CPLD is dedicated to IP protection, CvP, partial reconfiguration, and power and temperature management.	Section 3.3
x8 PCI Express 3.0 male connector	This connector supports PCI Express at 2.5, 5.0, and 8.0 Gbps for x8, x4, and x1 link width. PCI Express is provided via FPGA transceivers.	Section 3.6
DDR3L SDRAM	Two independent banks of DDR3L-SDRAM are available. Each bank consists of 9 x 4 Gb (8-bit wide) chips, which feature: • Up to 4 Gbytes density (4 Gbytes are mounted by default) • 72-bit data path • Up to 800 MHz clock frequency • Maximum throughput of 12.8 Gbytes per bank	Section 3.7
QSFP+ interfaces	Two QSPF+ interfaces connected to eight FPGA transceivers to enable 2 x 40Gbs links or up to 8 x 10Gbs links. All links have the same reference clock.	Section 3.8
Time stamping (PPS) on Micro BNC	The board provides a Time Stamping feature via a MicroBNC connector. Time Stamping can be effected using one of three electrical formats: • Schmitt trigger • ADC converter (serial bus) • Basic comparator	Section 3.9
Extension interface	The extension interface provides access to eight Rx/Tx GxB transceivers to enable board-to-board data transfers up to 80 Gbps. This interface also provides 10 other LVCMOS25 signals data transfer of up to 40 Gbps.	--
LEDs	8 user LEDs are available on the component side of the board.	Section 3.11
Reset button	1 local power-on reset button on the component side of the board.	Section 3.12
Switches	3 micro switches on the component side.	Section 3.13
EEPROMs	Two 256k-bit Serial FlashPROMs are available for data storage via two I²C links	Section 3.14
Power supply	Power is provided via a daughter card supplied by the PCIe slot (12/3.3 V).	Section 3.16

Table 1: Board features description

2.4 Mechanical Description

The following diagram illustrates the mechanical architecture of the XpressGX5LP-QE board without the fansink mounted.

Note: The overall height of the board, that is, the height of the highest component, is 14mm.

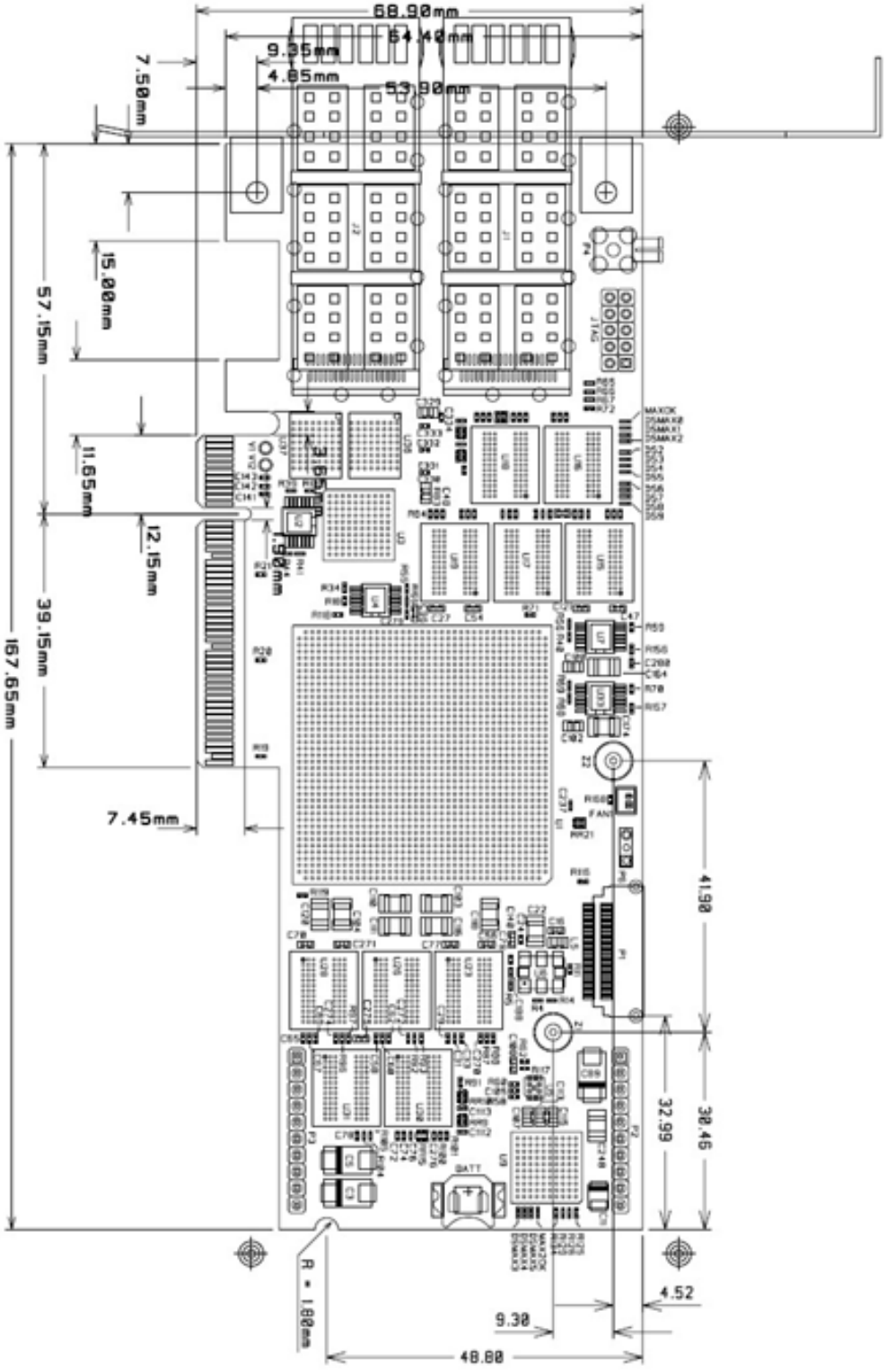


Figure 3: XpressGX5LP-QE mechanical architecture

Chapter 3 XpressGX5LP-QE Features

3.1 Stratix V GX FPGA Device

The XpressGX5LP-QE board can be mounted with either the Altera 5SGXEA7K2F40C2N or the 5SGXEA4K2F40C2N FPGA. The following table shows the resources of each available Stratix V GX FPGA:

FPGA	LEs	Registers	M20K RAM Blocks	M20K Memory	18x18 Multipliers	27x27 Multipliers	PLL
5SGXA4	420 K	634 K	1900	37 Mbits	512	512	24
5SGXA7	622 K	939 K	2560	50 Mbits	256	256	28

Table 2: Stratix V GX FPGA Resources

3.2 Board Configuration Module

The XpressGX5LP uses an EPM570F100 Max II CPLD as a 32-bit FPP Configuration Module.

The FPP module consists of 2 x 256MB PC28F00BP30 Micron 16-bit FlashPROMs that are directly connected to the FPGA on the FPP 32-bit interface.

At FPGA power-up, the CPLD acts as an address counter to configure the FPGA.

Both FlashPROMs are directly accessible via the FGPA, and the address bus and control signals are shared between the FPGA and the CPLD.

MSEL signals available on the CPLD enable the FPGA configuration type to be modified.

The SW1-4 switch enables you to select a boot sector (0 or 1), while the push button BPCONF on the solder side enables you to reconfigure the FPGA with one of the two Flash boot sectors (depending on the position of SW1-4).

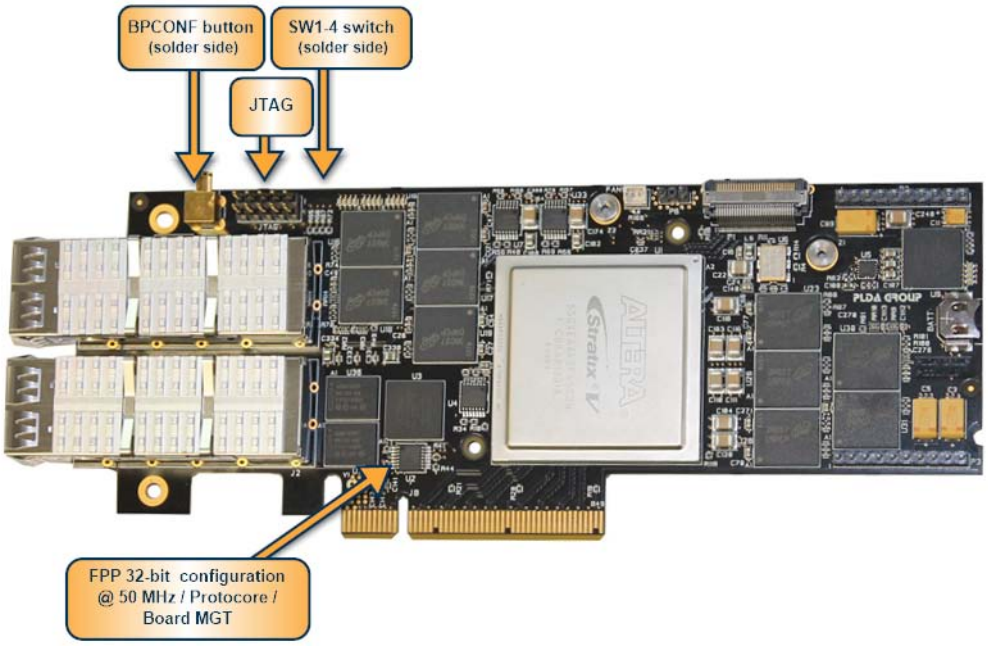


Figure 4: Board Configuration component side

The BPCONF button and SW1-4 switch on the solder side of the board are shown below:

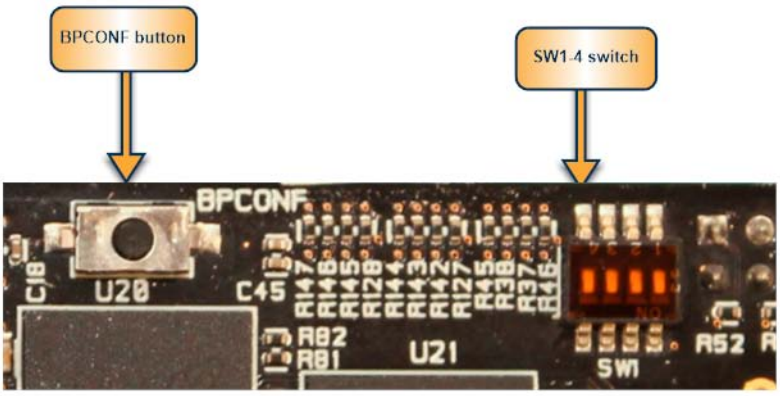


Figure 5: Board configuration solder side

The following diagram shows the board configuration module:

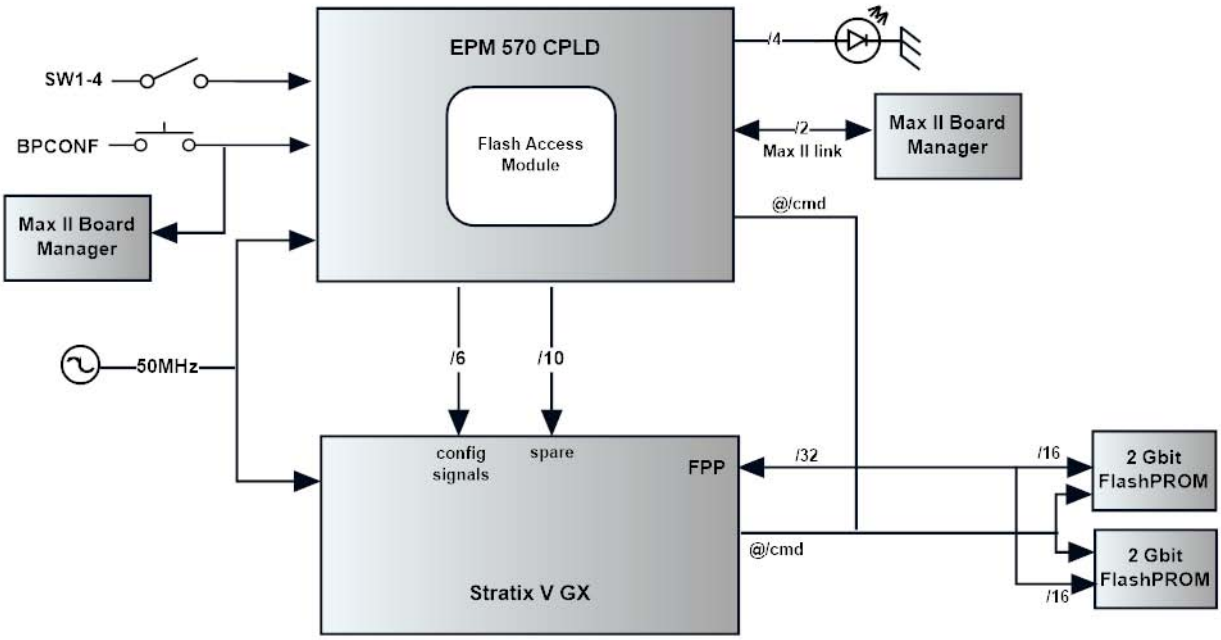


Figure 6: Max II EPM 570 board configuration module

The following table shows pin assignments for the FlashPROMs on the FPGA:

Flash Data		Flash Address		Flash Control	
flash_data00	AP33	flash_ad00	AM28	flash_oe0#	AT24
flash_data01	AT33	flash_ad01	AL27	flash_rst0#	AV23
flash_data02	AR33	flash_ad02	AM29	flash_ce0#	AT23
flash_data03	AU34	flash_ad03	AW26	flash_wp0#	AU23
flash_data04	AU33	flash_ad04	AN27	flash_adv0#	AU24
flash_data05	AN31	flash_ad05	AN25	flash_we0#	AP25
flash_data06	AM31	flash_ad06	AL26	flash_wait0	AW23

Table 3: FlashPROM pin assignments on the FPGA

Flash Data		Flash Address		Flash Control	
flash_data07	AU32	flash_ad07	AK29	--	--
flash_data08	AT32	flash_ad08	AM25	flash_oe1#	AV25
flash_data09	AR31	flash_ad09	AM26	flash_rst1#	AN28
flash_data10	AP31	flash_ad10	AL29	flash_ce1#	AK30
flash_data11	AW34	flash_ad11	AL30	flash_wp1#	AP27
flash_data12	AV34	flash_ad12	AR27	flash_adv1#	AR28
flash_data13	AW31	flash_ad13	AT27	flash_we1#	AU25
flash_data14	AV31	flash_ad14	AN24	flash_wait1	AU26
flash_data15	AW32	flash_ad15	AK27	--	--
flash_data16	AV32	flash_ad16	AJ27	flash_clk	AU27
flash_data17	AJ33	flash_ad17	AN26	--	--
flash_data18	AH33	flash_ad18	AP28	--	--
flash_data19	AL33	flash_ad19	AT26	--	--
flash_data20	AK33	flash_ad20	AJ29	--	--
flash_data21	AK32	flash_ad21	AL28	--	--
flash_data22	AJ32	flash_ad22	AW25	--	--
flash_data23	AH31	flash_ad23	AR25	--	--
flash_data24	AG31	flash_ad24	AK26	--	--
flash_data25	AF31	flash_ad25	AV26	--	--
flash_data26	AE31	flash_ad26	AL25	--	--
flash_data27	AJ30	--	--	--	--
flash_data28	AH30	--	--	--	--
flash_data29	AR30	--	--	--	--
flash_data30	AP30	--	--	--	--
flash_data31	AU30	--	--	--	--

Table 3: FlashPROM pin assignments on the FPGA

The following table shows the pin assignments of the FlashPROMs and FPGA configuration signals on the CPLD.

Flash Address		Flash Control		FPGA Configuration		CPLD Status/Control + FPGA		
flash_ad00	J3	flash_clk	E3	msel0	J9	osc_config_cpld	E2	
flash_ad01	J4	--	--	msel1	J8	--	--	
flash_ad02	K3	flash_adv0#	B6	msel2	K10	max_sw0	A10	
flash_ad03	K5	flash_wp0#	B8	msel3	J10	--	--	
flash_ad04	K4	flash_ce0#	C8	msel4	H9	max_confdone	B9	

Table 4: FlashPROM pin assignments + FPGA configuration signals on the CPLD

Flash Address		Flash Control		FPGA Configuration		CPLD Status/Control + FPGA		
flash_ad05	J6	flash_rst0#	C7	--	--	max_leduser0	C9	
flash_ad06	J5	flash_wait0	B7	nconfig	K1	max_leduser1	B10	
flash_ad07	G2	flash_oe0#	A7	init_done	K2	max_leduser2	C10	
flash_ad08	H7	flash_we0#	A6	dclk_cpld	A8	--	--	
flash_ad09	H4	--	--	clrconfig#	A9	conf_rfu0	G9	AV22
flash_ad10	G3	flash_adv1#	C2	nstatus	G10	conf_rfu1	D9	AR24
flash_ad11	F2	flash_wp1#	D1	conf_done	H10	conf_rfu2	F9	AR22
flash_ad12	D2	flash_ce1#	F1	--	--	conf_rfu3	F10	AV21
flash_ad13	D3	flash_rst1#	F3	--	--	conf_rfu4	H8	AM23
flash_ad14	E8	flash_wait1	A3	--	--	conf_rfu5	D8	AW22
flash_ad15	B1	flash_oe1#	A4	--	--	conf_rfu6	G8	AL24
flash_ad16	A2	flash_we1#	B5	--	--	conf_rfu7	D10	AP24
flash_ad17	C4	--	--	--	--	conf_rfu8	K8	AN23
flash_ad18	C1	--	--	--	--	conf_rfu9	E9	AT21
flash_ad19	B3	--	--	--	--	--	--	
flash_ad20	A1	--	--	--	--	--	--	
flash_ad21	B2	--	--	--	--	--	--	
flash_ad22	K6	--	--	--	--	--	--	
flash_ad23	A5	--	--	--	--	--	--	
flash_ad24	C3	--	--	--	--	--	--	
flash_ad25	B4	--	--	--	--	--	--	
flash_ad26	K7	--	--	--	--	--	--	

Table 4: FlashPROM pin assignments + FPGA configuration signals on the CPLD

Note: In the table above, RFU signifies signals that are reserved for future use.

Configuration MAX is the first device available on the JTAG chain. This device must never be deleted.

The following table shows the memory mapping for the Flash Access Module:

Name	Size	Address
FPGA Sector 1 or User Sector (SW1-4 = 1)	64MB	7FF FFFF 400 0000
Sector 0 (SW1-4 = 0)	64MB	3FF FFFF 000 0000

Table 5: Flash Memory Mapping

3.3 Board Manager

A second Max II CPLD is dedicated to IP protection, Configuration via Protocol (CvP), Partial Reconfiguration, and power and temperature management.

The following figure shows the Max II board manager:

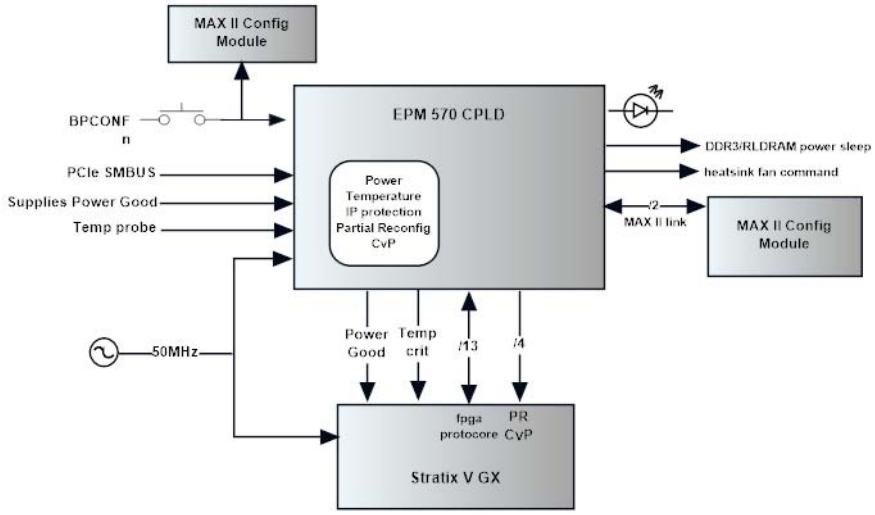


Figure 7: Max II board manager

The following table shows the pin assignments of the management signals on the CPLD and other components:

Signal	CPLD Pin	FPGA or Component Pin	Comment
Protocore			
osc_config_proto	E10	Na	MAX Main clock input (50MHz)
--	--	--	--
proto_led0	B1	DSMAX3 (Red LED)	MAX LEDs: NDY
proto_led1	C2	DSMAX4 (Green LED)	
proto_led2	C1	DSMAX5 (Orange LED)	
proto_led3	D1	MAX2OK (Green LED)	
--	--	--	--
prot0_out	D9	FGPA: AC24	Protocore reset
--	--	--	--
prot1_in0	B8	FPGA: AE21	IP protection # 1
prot1_in1	G9	FPGA: AD22	
prot1_out	D8	FPGA: AE20	
--	--	--	--
prot2_in0	C8	FPGA: AD21	IP protection #2
prot2_in1	G10	FPGA: AD23	
prot2_out	H9	FPGA: AG22	
--	--	--	--

Table 6: Management signals pin assignments

Signal	CPLD Pin	FPGA or Component Pin	Comment
fpga_proto_misc0	G8	FPGA: AG21	IP protection misc signals
fpga_proto_misc1	E8	FPGA: AD20	
fpga_proto_misc2	B7	FPGA: AH21	
fpga_proto_misc3	E9	FPGA: AF22	
fpga_proto_misc4	C7	FPGA: AJ21	
fpga_proto_misc5	F10	FPGA: AB24	
POR			
por_VCCR_GXB	B6	--	Power good from GXB DC/DC converters
por_VCCA_GXB	J6	--	
ddr3_pgood	J10	--	Power good from DDR3L termination managers
--	--	--	--
ddr3_slp_s3	H10	--	Sleep mode input of DDR3L termination managers
--	--	--	--
fpga_power_good	F9	FPGA: AE22	Global power good
Temp MGT/PCIe SMBU			
smb_temp_d	K3	LM83: 12	Temperature Data information inputs
smb_temp_clk	K4	LM83: 14	
--	--	--	--
temp_int#	J3	LM83 : 11	Heat sink command output Temperature critical warning
temp_crit#	J4	LM83 : 16	
--	--	--	--
pcie_sm_dat	H8	PCIe connector: JB6	NDY
pcie_sm_clk	J8	PCIe connector: JB5	NDY
Partial Reconfig/CVP			
pr_error	C9	FPGA: AU29	Partial reconfiguration control pins: RFU
pr_ready	D10	FPGA: AN29	
pr_request	B9	FPGA: AN30	
pr_done	B10	FPGA: AT30	
--	--	--	
cvp_confdone	C10	FPGA: AT29	
max2_link0	A10	CONF_CPLD: G1	Link between the two MAX II CPLDs for POR signals.
max2_link1	B2	CONF_CPLD: H1	
clrconfig	E3	CONF_CPLD: A9	Reset push button

Table 6: Management signals pin assignments

Note: This device is the last device on the JTAG chain.

3.4 Dedicated Clocks

The following table describes clock assignments for the board.

Signal	FPGA Pin	Type	Comment
osc_config_FPGA	AV29	LVCMOS25	Single-ended 50MHz clock used for the Max II CPLDs.
Osc3 p/n	AK23/AL23	LVDS	125 MHz CLK used for PCIe Hard IP.
Osc5 p/n	E34/D34	LVDS	200 MHz CLK dedicated to DDR3L Bank1.
Osc7 p/n	AR8/AT8	LVDS	200 MHz CLK dedicated to DDR3L Bank0.
Osc8 p/n	G7/G6	LVDS	200 MHz CLK dedicated to QDR2 banks.
GXB Transceiver Clock Inputs			
Qsfp1_refclk0_p/n	AF6/AF5	LVDS	644.53125MHz or I²C PLL clock for QSFP+ and extension interface connectors. Max skew between the 8 clocks is 40ps. See Section 3.5 for more information.
Qsfp1_refclk1_p/n	AD7/AD6	LVDS	
Qsfp2_refclk2_p/n	AB6/AB5	LVDS	
Qsfp2_refclk3_p/n	Y7/Y6	LVDS	
Herma1_refclk4_p/n	V6/V5	LVDS	
Herma1_refclk5_p/n	T7/T6	LVDS	
Herma2_refclk6_p/n	V34/V35	LVDS	
Herma2_refclk7_p/n	T33/T34	LVDS	
Pcie_clk_100MHz p/n	AF34/AF35	HCSL	100 MHz Transceiver RefCLK for PCIe Gen2.

Table 7: XpressGX5LP-QE clock assignments

3.5 Transceiver Clock Tree

The QSFP+ and Extension interface links are connected to four different GxB transceivers, each featuring two reference clock inputs.

These eight clock inputs are fed by the same clock frequency with a maximum skew of 40ps.

The clock frequency can either be a fixed 644.53125MHz/50ppm frequency or a user-defined clock from an I²C PLL (Si570FBB0042DG). The clock type can be selected via a signal coming from the FPGA.

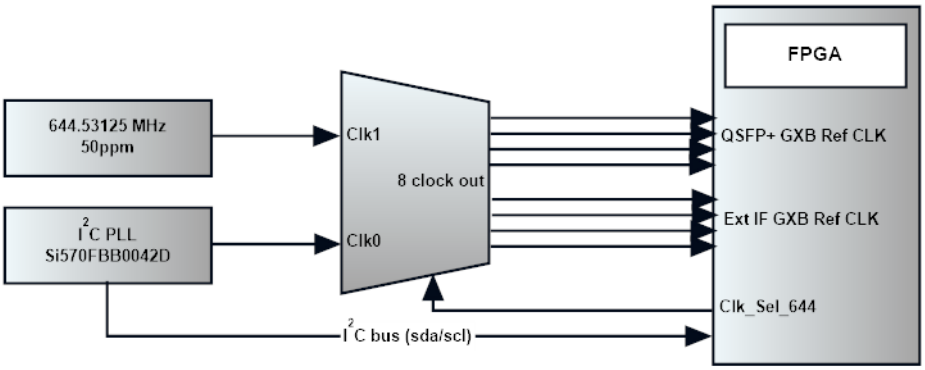


Figure 8: Reference Clock inputs

Signal	FPGA Pin	Type	Comment
Clk_sel_644	B11	LVCMOS25	Select the ‘’2 to 8’’ multiplexer input. Logical ‘0’ will set I²C PLL, and Logical ‘1’ will set a fixed 644.53125MHz frequency (default) as the clock input.
SDA	A11	LVCMOS25	I²C data line
SCL	A10	LVCMOS25	I²C clock line

Table 8: Transceiver clock tree pin assignment

3.6 PCI Express Endpoint Connector

The PCI Express male connector enables access to Endpoint PCI Express components as a x1, x4, or x8 PCI Express 2.0/3.0 Link.

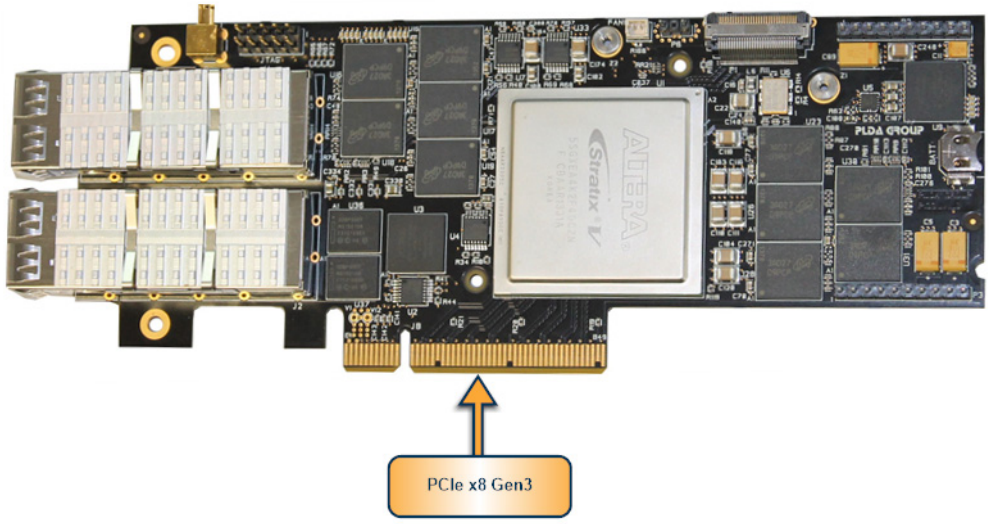


Figure 9: PCI Express connector

The table below describes pin assignments for the PCI Express Endpoint connector. Shaded signals are defined as optional by the *PCI Express Card Electromechanical Specification 2.0*, and signals that appear bold are active signals implemented on the XpressGX5LP-QE.

Side B			Side A		
PCI Express Pin	**FPGA Pin**	**Signal**	**PCI Express Pin**	**FPGA Pin**	**Signal**
1	--	+12V	1	connected to mPRSNT#2	mPRSNT1#
2	--	+12V	2	--	+12V
3	--	+12V	3	--	+12V
4	--	GND	4	--	GND
5	MAX2 - J8	Sm_clk	5	nc	JTAG2
6	MAX2 - H8	Sm_dat	6	nc	JTAG3
7	--	GND	7	nc	JTAG4
8	--	+3.3V	8	nc	JTAG5
9	nc	JTAG1	9	--	+3.3V
10	Linked to 3.3V via a jumper	3.3Vaux	10	--	+3.3V
11	nc	mWAKE#	11	AC28	**mPERST#**
--	--	--	--	--	--
12	--	RSVD	12	--	GND
13	--	GND	13	AF34	PCIe_CLKp
14	AV38	mPERp0	14	AF35	PCIe_CLKn
15	AV39	mPERn0	15	--	GND

Table 9: Pin assignments for the PCI Express endpoint connector

Side B			Side A		
PCI Express Pin	FPGA Pin	Signal	PCI Express Pin	FPGA Pin	Signal
16	--	GND	16	AU36	mPETp0
17	connected to mPRSNT#1	mPRSNT2#	17	AU37	mPETn0
18	--	GND	18	--	GND
19	AT38	mPERp1	19	--	RSVD
20	AT39	mPERn1	20	--	GND
21	--	GND	21	AR36	mPETp1
22	--	GND	22	AR37	mPETn1
23	AP38	mPERp2	23	--	GND
24	AP39	mPERn2	24	--	GND
25	--	GND	25	AN36	mPETp2
26	--	GND	26	AN37	mPETn2
27	AM38	mPERp3	27	--	GND
28	AM39	mPERn3	28	--	GND
29	--	GND	29	AL36	mPETp3
30	--	RSVD	30	AL37	mPETn3
31	connected to mPRSNT#1	mPRSNT#2	31	--	GND
32	--	GND	32	--	RSVD
33	AH38	mPERp4	33	--	RSVD
34	AH39	mPERn4	34	--	GND
35	--	GND	35	AG36	mPETp4
36	--	GND	36	AG37	mPETn4
37	AF38	mPERp5	37	--	GND
38	AF39	mPERn5	38	--	GND
39	--	GND	39	AE36	mPETp5
40	--	GND	40	AE37	mPETn5
41	AD38	mPERp6	41	--	GND
42	AD39	mPERn6	42	--	GND
43	--	GND	43	AC36	mPETp6
44	--	GND	44	AC37	mPETn6
45	AB38	mPERp7	45	--	GND
46	AB39	mPERn7	46	--	GND
47	--	GND	47	AA36	mPETp7

Table 9: Pin assignments for the PCI Express endpoint connector

Side B			Side A		
PCI Express Pin	FPGA Pin	Signal	PCI Express Pin	FPGA Pin	Signal
48	connected to mPRSNT#1	mPRSNT#2	48	AA37	mPETn7
49	--	GND	49	--	GND

Table 9: Pin assignments for the PCI Express endpoint connector

3.7 DDR3L SDRAM

The XpressGX5LP-QE features 2 independent banks of DDR3L SDRAM, each capable of addressing 4 GB in a 72-bit wide datapath. The 18 mounted devices are Micron MT41K512M8RA-125.

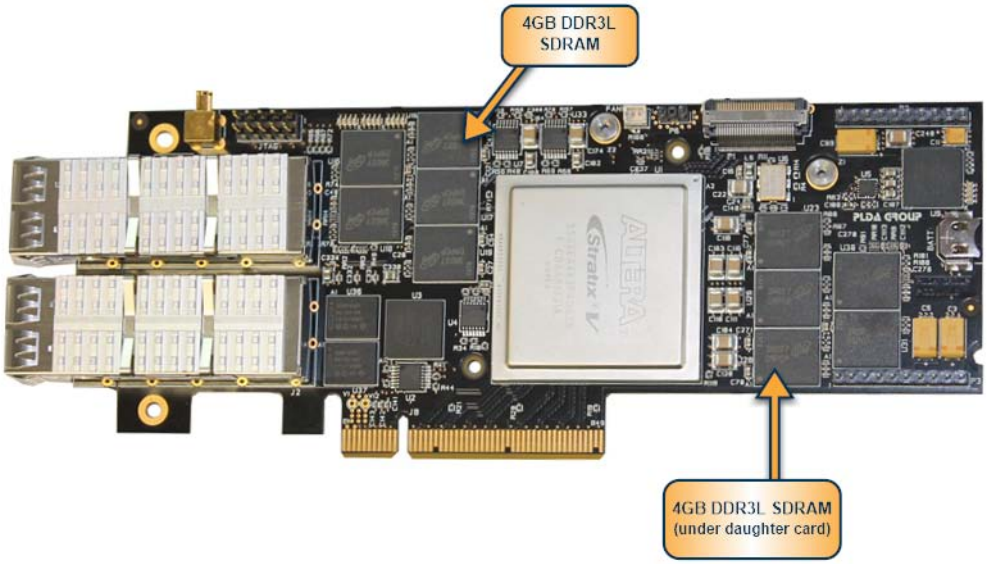


Figure 10: DDR3L SDRAM

The following table shows pin assignments for the DDR3L SDRAM:

Bank 0		Bank 1	
FPGA Pin	**Signal**	**FPGA Pin**	**Signal**
ddr3_Bank0_a00	AM17	ddr3_Bank1_a00	C22
ddr3_Bank0_a01	AR18	ddr3_Bank1_a01	E20
ddr3_Bank0_a02	AF16	ddr3_Bank1_a02	E23
ddr3_Bank0_a03	AM16	ddr3_Bank1_a03	A23
ddr3_Bank0_a04	AR19	ddr3_Bank1_a04	G20
ddr3_Bank0_a05	AG16	ddr3_Bank1_a05	F23
ddr3_Bank0_a06	AP19	ddr3_Bank1_a06	K22
ddr3_Bank0_a07	AW17	ddr3_Bank1_a07	G23
ddr3_Bank0_a08	AM19	ddr3_Bank1_a08	K21
ddr3_Bank0_a09	AT17	ddr3_Bank1_a09	D21
ddr3_Bank0_a10	AT18	ddr3_Bank1_a10	F20
ddr3_Bank0_a11	AP18	ddr3_Bank1_a11	J22
ddr3_Bank0_a12	AU18	ddr3_Bank1_a12	F21
ddr3_Bank0_a13	AW16	ddr3_Bank1_a13	E21
ddr3_Bank0_a14	AV17	ddr3_Bank1_a14	J21
ddr3_Bank0_a15	AL18	ddr3_Bank1_a15	G22

Table 10: DDR3L SDRAM pin assignments

Bank 0		Bank 1	
FPGA Pin	**Signal**	**FPGA Pin**	**Signal**
ddr3_Bank0_ba0	AL16	ddr3_Bank1_ba0	B23
ddr3_Bank0_ba1	AV19	ddr3_Bank1_ba1	G21
ddr3_Bank0_ba2	AU16	ddr3_Bank1_ba2	B20
ddr3_Bank0_cas#	AR17	ddr3_Bank1_cas#	D22
ddr3_Bank0_cke0	AW19	ddr3_Bank1_cke0	H20
ddr3_Bank0_cke1	AN8	ddr3_Bank1_cke1	H22
ddr3_Bank0_CKn	AN18	ddr3_Bank1_CKn	N21
ddr3_Bank0_CKp	AN19	ddr3_Bank1_CKp	N20
ddr3_Bank0_cs0#	AN17	ddr3_Bank1_cs0#	K24
ddr3_Bank0_cs1#	AJ6	ddr3_Bank1_cs1#	H23
ddr3_Bank0_d00	AJ15	ddr3_Bank1_d00	C24
ddr3_Bank0_d01	AG14	ddr3_Bank1_d01	C25
ddr3_Bank0_d02	AB16	ddr3_Bank1_d02	G24
ddr3_Bank0_d03	AB15	ddr3_Bank1_d03	D25
ddr3_Bank0_d04	AH15	ddr3_Bank1_d04	D24
ddr3_Bank0_d05	AG15	ddr3_Bank1_d05	F24
ddr3_Bank0_d06	AD16	ddr3_Bank1_d06	H25
ddr3_Bank0_d07	AC15	ddr3_Bank1_d07	G25
ddr3_Bank0_d08	AH19	ddr3_Bank1_d08	J25
ddr3_Bank0_d09	AJ18	ddr3_Bank1_d09	P26
ddr3_Bank0_d10	AE18	ddr3_Bank1_d10	K25
ddr3_Bank0_d11	AK18	ddr3_Bank1_d11	P25
ddr3_Bank0_d12	AG19	ddr3_Bank1_d12	M26
ddr3_Bank0_d13	AJ19	ddr3_Bank1_d13	N25
ddr3_Bank0_d14	AE19	ddr3_Bank1_d14	L26
ddr3_Bank0_d15	AH18	ddr3_Bank1_d15	N26
ddr3_Bank0_d16	AE9	ddr3_Bank1_d16	H26
ddr3_Bank0_d17	AC10	ddr3_Bank1_d17	C26
ddr3_Bank0_d18	AC9	ddr3_Bank1_d18	J26
ddr3_Bank0_d19	AB10	ddr3_Bank1_d19	C27
ddr3_Bank0_d20	AD9	ddr3_Bank1_d20	F26
ddr3_Bank0_d21	AJ10	ddr3_Bank1_d21	D27
ddr3_Bank0_d22	AB9	ddr3_Bank1_d22	G26

Table 10: DDR3L SDRAM pin assignments

Bank 0		Bank 1	
FPGA Pin	**Signal**	**FPGA Pin**	**Signal**
ddr3_Bank0_d23	AH10	ddr3_Bank1_d23	E27
ddr3_Bank0_d24	AU9	ddr3_Bank1_d24	K27
ddr3_Bank0_d25	AM10	ddr3_Bank1_d25	R27
ddr3_Bank0_d26	AT9	ddr3_Bank1_d26	M27
ddr3_Bank0_d27	AL10	ddr3_Bank1_d27	T27
ddr3_Bank0_d28	AP9	ddr3_Bank1_d28	P28
ddr3_Bank0_d29	AR9	ddr3_Bank1_d29	J27
ddr3_Bank0_d30	AU10	ddr3_Bank1_d30	N27
ddr3_Bank0_d31	AN9	ddr3_Bank1_d31	L27
ddr3_Bank0_d32	AA12	ddr3_Bank1_d32	D30
ddr3_Bank0_d33	AD14	ddr3_Bank1_d33	H31
ddr3_Bank0_d34	AA13	ddr3_Bank1_d34	F30
ddr3_Bank0_d35	AH13	ddr3_Bank1_d35	E31
ddr3_Bank0_d36	AC13	ddr3_Bank1_d36	E30
ddr3_Bank0_d37	AJ13	ddr3_Bank1_d37	G31
ddr3_Bank0_d38	AB13	ddr3_Bank1_d38	G30
ddr3_Bank0_d39	AC14	ddr3_Bank1_d39	C30
ddr3_Bank0_d40	AV14	ddr3_Bank1_d40	N30
ddr3_Bank0_d41	AP13	ddr3_Bank1_d41	L30
ddr3_Bank0_d42	AV13	ddr3_Bank1_d42	R31
ddr3_Bank0_d43	AN13	ddr3_Bank1_d43	K30
ddr3_Bank0_d44	AW14	ddr3_Bank1_d44	M30
ddr3_Bank0_d45	AL13	ddr3_Bank1_d45	J30
ddr3_Bank0_d46	AW13	ddr3_Bank1_d46	R30
ddr3_Bank0_d47	AM13	ddr3_Bank1_d47	L31
ddr3_Bank0_d48	AR14	ddr3_Bank1_d48	J28
ddr3_Bank0_d49	AR15	ddr3_Bank1_d49	P29
ddr3_Bank0_d50	AM14	ddr3_Bank1_d50	J29
ddr3_Bank0_d51	AK14	ddr3_Bank1_d51	R29
ddr3_Bank0_d52	AN14	ddr3_Bank1_d52	L28
ddr3_Bank0_d53	AT15	ddr3_Bank1_d53	V29
ddr3_Bank0_d54	AL14	ddr3_Bank1_d54	K28
ddr3_Bank0_d55	AU15	ddr3_Bank1_d55	U29
ddr3_Bank0_d56	AK12	ddr3_Bank1_d56	E28

Table 10: DDR3L SDRAM pin assignments

Bank 0		Bank 1	
FPGA Pin	**Signal**	**FPGA Pin**	**Signal**
ddr3_Bank0_d57	AE11	ddr3_Bank1_d57	C28
ddr3_Bank0_d58	AG12	ddr3_Bank1_d58	D28
ddr3_Bank0_d59	AD12	ddr3_Bank1_d59	A28
ddr3_Bank0_d60	AF11	ddr3_Bank1_d60	F29
ddr3_Bank0_d61	AE10	ddr3_Bank1_d61	B29
ddr3_Bank0_d62	AL12	ddr3_Bank1_d62	B28
ddr3_Bank0_d63	AE12	ddr3_Bank1_d63	A29
ddr3_Bank0_d64	AV11	ddr3_Bank1_d64	G34
ddr3_Bank0_d65	AR11	ddr3_Bank1_d65	E32
ddr3_Bank0_d66	AK11	ddr3_Bank1_d66	H34
ddr3_Bank0_d67	AL11	ddr3_Bank1_d67	F32
ddr3_Bank0_d68	AW11	ddr3_Bank1_d68	K33
ddr3_Bank0_d69	AT11	ddr3_Bank1_d69	J34
ddr3_Bank0_d70	AR12	ddr3_Bank1_d70	J33
ddr3_Bank0_d71	AU11	ddr3_Bank1_d71	K34
ddr3_Bank0_dqs00n	AE15	ddr3_Bank1_dqs00n	E25
ddr3_Bank0_dqs00p	AD15	ddr3_Bank1_dqs00p	E24
ddr3_Bank0_dqs01n	AG18	ddr3_Bank1_dqs01n	R26
ddr3_Bank0_dqs01p	AF19	ddr3_Bank1_dqs01p	R25
ddr3_Bank0_dqs02n	AG10	ddr3_Bank1_dqs02n	F27
ddr3_Bank0_dqs02p	AF10	ddr3_Bank1_dqs02p	G27
ddr3_Bank0_dqs03n	AW10	ddr3_Bank1_dqs03n	T28
ddr3_Bank0_dqs03p	AV10	ddr3_Bank1_dqs03p	U28
ddr3_Bank0_dqs04n	AF14	ddr3_Bank1_dqs04n	C31
ddr3_Bank0_dqs04p	AE14	ddr3_Bank1_dqs04p	D31
ddr3_Bank0_dqs05n	AU14	ddr3_Bank1_dqs05n	N31
ddr3_Bank0_dqs05p	AT14	ddr3_Bank1_dqs05p	P31
ddr3_Bank0_dqs06n	AP15	ddr3_Bank1_dqs06n	T30
ddr3_Bank0_dqs06p	AN15	ddr3_Bank1_dqs06p	U30
ddr3_Bank0_dqs07n	AJ12	ddr3_Bank1_dqs07n	G29
ddr3_Bank0_dqs07p	AH12	ddr3_Bank1_dqs07p	H29
ddr3_Bank0_dqs08n	AU12	ddr3_Bank1_dqs08n	E33
ddr3_Bank0_dqs08p	AT12	ddr3_Bank1_dqs08p	F33
ddr3_Bank0_odt0	AN16	ddr3_Bank1_odt0	A22

Table 10: DDR3L SDRAM pin assignments

Bank 0		Bank 1	
FPGA Pin	**Signal**	**FPGA Pin**	**Signal**
ddr3_Bank0_odt1	AJ7	ddr3_Bank1_odt1	B22
ddr3_Bank0_ras#	AV16	ddr3_Bank1_ras#	C21
ddr3_Bank0_rst#	AU17	ddr3_Bank1_rst#	C20
ddr3_Bank0_tdqs00n	AA15	ddr3_Bank1_tdqs00n	A25
ddr3_Bank0_tdqs00p	AA14	ddr3_Bank1_tdqs00p	B25
ddr3_Bank0_tdqs01n	AD17	ddr3_Bank1_tdqs01n	T25
ddr3_Bank0_tdqs01p	AD18	ddr3_Bank1_tdqs01p	U25
ddr3_Bank0_tdqs02n	AH9	ddr3_Bank1_tdqs02n	A26
ddr3_Bank0_tdqs02p	AG9	ddr3_Bank1_tdqs02p	B26
ddr3_Bank0_tdqs03n	AP10	ddr3_Bank1_tdqs03n	U27
ddr3_Bank0_tdqs03p	AN10	ddr3_Bank1_tdqs03p	U26
ddr3_Bank0_tdqs04n	AG13	ddr3_Bank1_tdqs04n	A31
ddr3_Bank0_tdqs04p	AF13	ddr3_Bank1_tdqs04p	B31
ddr3_Bank0_tdqs05n	AP12	ddr3_Bank1_tdqs05n	J31
ddr3_Bank0_tdqs05p	AN12	ddr3_Bank1_tdqs05p	K31
ddr3_Bank0_tdqs06n	AL15	ddr3_Bank1_tdqs06n	M29
ddr3_Bank0_tdqs06p	AK15	ddr3_Bank1_tdqs06p	N28
ddr3_Bank0_tdqs07n	AC12	ddr3_Bank1_tdqs07n	G28
ddr3_Bank0_tdqs07p	AB12	ddr3_Bank1_tdqs07p	H28
ddr3_Bank0_tdqs08n	AN11	ddr3_Bank1_tdqs08n	G32
ddr3_Bank0_tdqs08p	AM11	ddr3_Bank1_tdqs08p	G33
ddr3_Bank0_we#	AP16	ddr3_Bank1_we#	A20

Table 10: DDR3L SDRAM pin assignments

3.8 Dual QSFP+ Interface

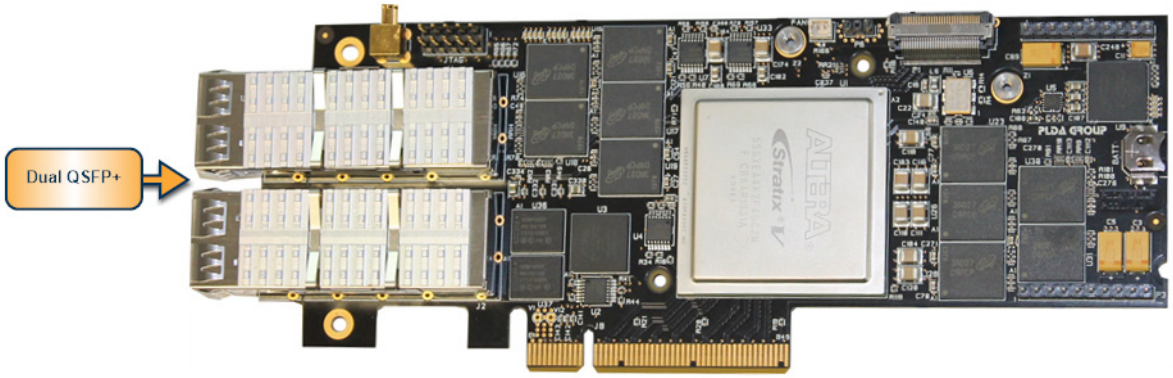


Figure 11: QSFP+ interface

The XpressGX5LP-QE dual QSFP+ interfaces use eight FPGA GXB transceivers to enable either 2 x 40Gbps or up to 8 x 10Gpbs links. Both QSFP+ interfaces are fully independent, although they share a reference clock, as shown on the following diagram:

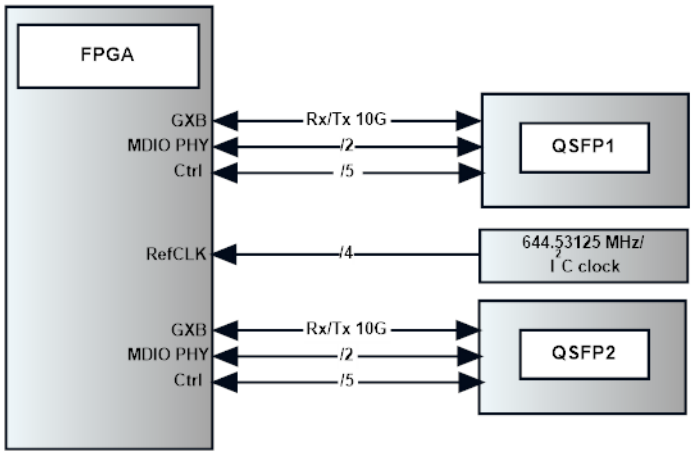


Figure 12: Dual QSFP+ interface connections

The following table shows the QSFP+ 1 pin assignments on the FPGA:

Signal	FPGA Pin	Ctrl/cmd/RefCLK	FPGA Pin
qsfp1_rx0n	AV1	qsfp1_int#	AH27
qsfp1_rx0p	AV2	qsfp1_lpmode	AD26
qsfp1_rx1n	AT1	qsfp1_modprs#	AH25
qsfp1_rx1p	AT2	qsfp1_modsel	AE26
qsfp1_rx2n	AP1	qsfp1_reset#	AF25
qsfp1_rx2p	AP2	qsfp1_scl	AF26
qsfp1_rx3n	AM1	qsfp1_sda	AG25
qsfp1_rx3p	AM2	qsfp1_refclk0_n	AF5
qsfp1_tx0n	AU3	qsfp1_refclk0_p	AF6
qsfp1_tx0p	AU4	qsfp1_refclk1_n	AD6
qsfp1_tx1n	AR3	qsfp1_refclk1_p	AD7
qsfp1_tx1p	AR4	--	--
qsfp1_tx2n	AN3	--	--
qsfp1_tx2p	AN4	--	--
qsfp1_tx3n	AL3	--	--
qsfp1_tx3p	AL4	--	--

Table 11: QSFP+ 1 pin assignments

The following table shows the QSFP+ 2 pin assignments on the FPGA:

Signal	FPGA Pin	Ctrl/cmd/RefCLK	FPGA Pin
qsfp2_rx0n	AF1	qsfp2_int#	AA29
qsfp2_rx0p	AF2	qsfp2_lpmode	AU20
qsfp2_rx1n	AD1	qsfp2_modprs#	AE27
qsfp2_rx1p	AD2	qsfp2_modsel	AV20
qsfp2_rx2n	AB1	qsfp2_reset#	AW20
qsfp2_rx2p	AB2	qsfp2_scl	AD27
qsfp2_rx3n	Y1	qsfp2_sda	AG27
qsfp2_rx3p	Y2	qsfp2_refclk2_n	AB5
qsfp2_tx0n	AE3	qsfp2_refclk2_p	AB6
qsfp2_tx0p	AE4	qsfp2_refclk3_n	Y6
qsfp2_tx1n	AC3	qsfp2_refclk3_p	Y7
qsfp2_tx1p	AC4	--	--

Table 12: QSFP+ 2 pin assignments

Signal	FPGA Pin	Ctrl/cmd/RefCLK	FPGA Pin
qsfp2_tx2n	AA3	--	--
qsfp2_tx2p	AA4	--	--
qsfp2_tx3n	W3	--	--
qsfp2_tx3p	W4	--	--

Table 12: QSFP+ 2 pin assignments

3.9 Time Stamping on Micro BNC

A time stamping feature is available on the XpressGX5LP-QE via a MicroBNC connector (Samtec part#: MCS-P-P-RA-TH1):

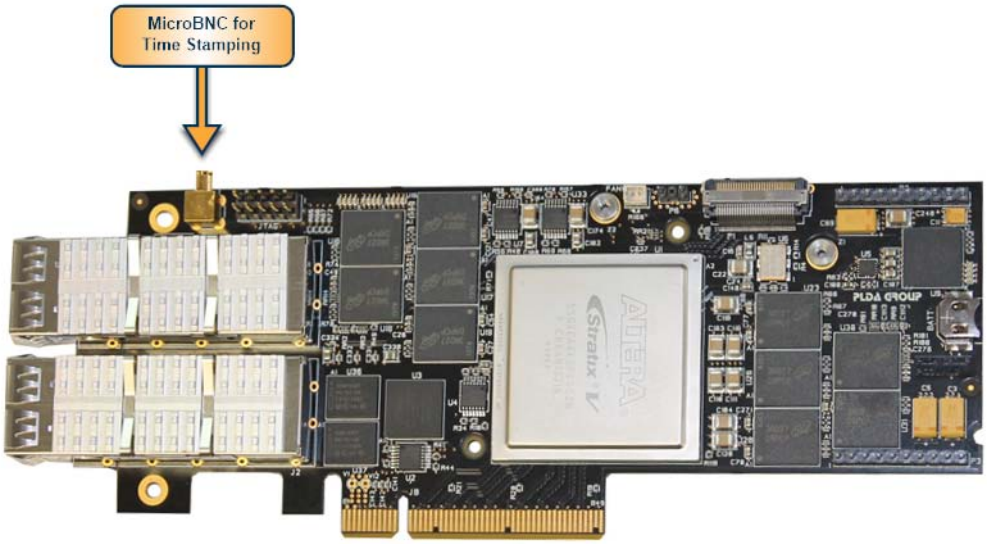
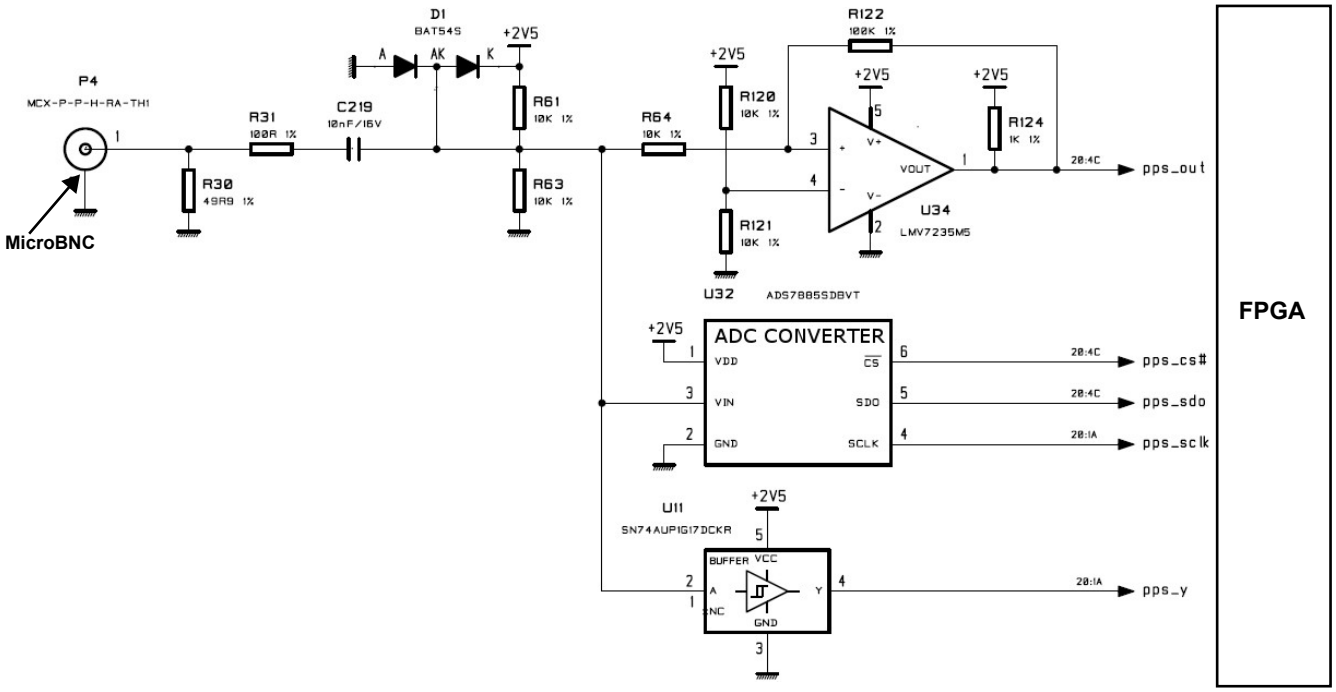


Figure 13: MicroBNC for time stamping

Time stamping signals are available as following on the FPGA:



Signal	FPGA Pin	Comment
pps_out	T10	Comparator pps clock input
pps_cs#	U9	ADC SPI chip select
pps_sdo	U10	ADC SPI data signal
Pps_sclk	U11	ADC SPI clock signal
pps_y	T12	Schmitt triggered pps clock input

Table 13: Time stamping signals

3.10 Extension Interface

An Extension interface is available on the XpressGX5LP-QE. This interface features eight high-speed links, directly connected to eight FPGA GXB transceivers. It also features 10 LVCMOS25 signals.

The connector part number is Samtec LSHM-130-01-F-DH-A-S-K and mates with Samtec HLCD cables or LSHM connectors.

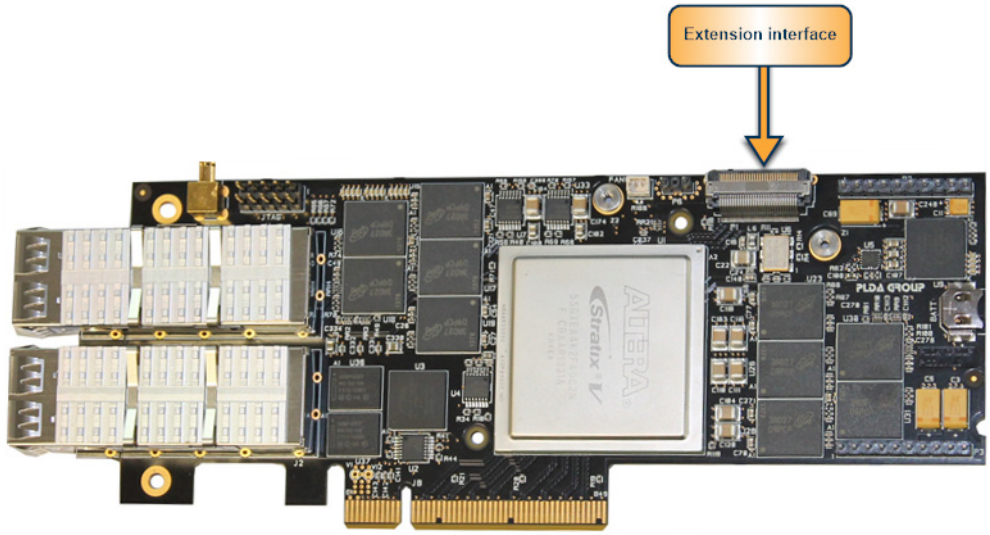


Figure 14: Extension interface

Signal	FPGA Pin	Connector Pin	Signal	FPGA Pin	Connector Pin
Ext_link_tx0n	N3	4	Ext_link_rx0n	P1	3
Ext_link_tx0p	N4	6	Ext_link_rx0p	P2	5
Ext_link_tx1n	L3	10	Ext_link_rx1n	M1	9
Ext_link_tx1p	L4	12	Ext_link_rx1p	M2	11
Ext_link_tx2n	J3	16	Ext_link_rx2n	K1	15
Ext_link_tx2p	J4	18	Ext_link_rx2p	K2	17
Ext_link_tx3n	G3	22	Ext_link_rx3n	H1	21
Ext_link_tx3p	G4	24	Ext_link_rx3p	H2	23

Table 14: Extension interface pin assignment

Signal	FPGA Pin	Connector Pin	Signal	FPGA Pin	Connector Pin
Ext_link_tx4n	N37	28	Ext_link_rx4n	P39	27
Ext_link_tx4p	N36	30	Ext_link_rx4p	P38	29
Ext_link_tx5n	L37	34	Ext_link_rx5n	M39	33
Ext_link_tx5p	L36	36	Ext_link_rx5p	M38	35
Ext_link_tx6n	J37	40	Ext_link_rx6n	K39	39
Ext_link_tx6p	J36	42	Ext_link_rx6p	K38	41
Ext_link_tx7n	G37	46	Ext_link_rx7n	H39	45
Ext_link_tx7p	G36	48	Ext_link_rx7p	H38	47
Ext_link_d1	E6	52	Ext_link_d0	A8	51
Ext_link_d3	D6	54	Ext_link_d2	E7	53
Ext_link_d5	C8	56	Ext_link_d4	B8	55
Ext_link_d7	D9	58	Ext_link_d6	F8	57
Ext_link_d9	E8	60	Ext_link_d8	C9	59

Table 14: Extension interface pin assignment

The Reference clock for the eight GxB links of the Extension interface can be chosen from the following four clocks (644.53125MHz or I²C clock, see Section 3.5 for more information).

Signal	FPGA Pin	Signal	FPGA Pin
Herma_refclk4_n	V5	Herma_refclk6_n	V35
Herma_refclk4_p	V6	Herma_refclk6_p	V34
Herma_refclk5_n	T6	Herma_refclk7_n	T34
Herma_refclk5_p	T7	Herma_refclk7_p	T33

Table 15: Extension interface clocks

3.11 LEDs

Eight user LEDs are available on the board:

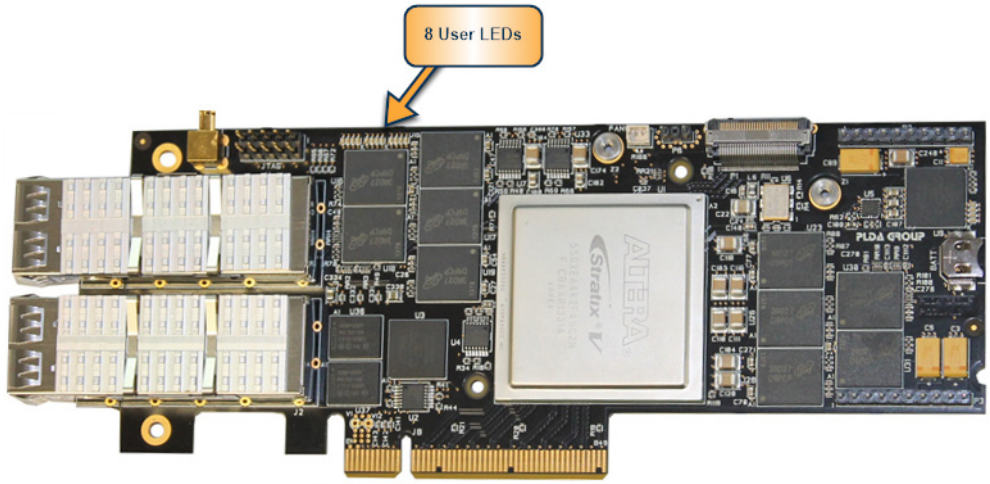


Figure 15: User LEDs

The following table describes pin assignments for the LEDs:

Signal	FPGA Pin	LED Name	LED Color
user_led0	AJ20	DS2	Yellow
user_led1	AK21	DS3	Yellow
user_led2	AL20	DS4	Green
user_led3	AL21	DS5	Green
user_led4	AM20	DS6	Orange
user_led5	AN21	DS7	Orange
user_led6	AN20	DS8	Red
user_led7	AR20	DS9	Red

Table 16: Pin assignments for the board LEDs

3.12 Local Reset

One active low reset push button (BPI) is available on the solder side of the board to enable register initialization:

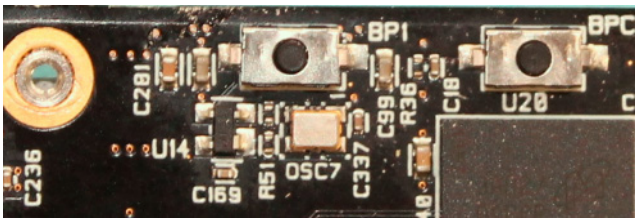


Figure 16: Reset button

Signal	FPGA Pin
user_resetn	N14

Table 17: Pin assignments for the reset button

3.13 Mechanical Switches

Three user switches are available on the solder side of the XpressGX5LP-QE on SW1. These enable three IOs to be set to a logical ’0’ or a logical ’1’. A fourth switch (SW1-4) enables you to select the configuration bit stream to load on the FPGA during configuration. This switch is not connected to the FPGA.

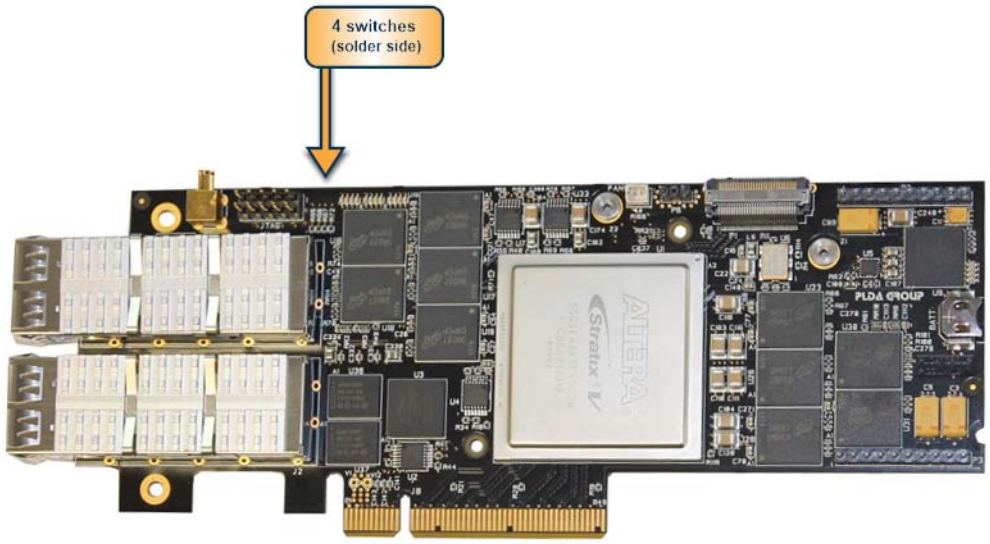


Figure 17: Mechanical switches

Signal Name	FPGA Pin or Function	Module
user_sw_a	U13	SW1-1
user_sw_b	U12	SW1-2
user_sw_c	T13	SW1-3
max_sw0	Configuration boot selection/ config MAX pin_A10	SW1-4

Table 18: Pin assignments for the mechanical switches

3.14 EEPROMs

Two 256k-bit Serial FlashPROMs (M24256BSMN6T) are available on the solder side of the XpressGX5LP for data storage via two I²C links.

The following table shows pin assignments for the EEPROMs:

EEPROM 0 Signal	FPGA Pin	EEPROM 1Signal	FPGA Pin
eeprom0_scl	P14	eeprom1_scl	T13
eeprom0_sda	N15	eeprom1_sda	R15
eeprom0_wr	R14	eeprom1_wr	U14

Table 19: Pin assignments for the EEPROMs

3.15 PIC

A PIC is available on the board for IP protection purposes. It is reserved for future use. The following table shows the PIC pin assignment on the FPGA:

Signal	FPGA Pin
pic_gpio0	AG26
pic_gpio1	AJ26
pic_gpio2	AJ24
pic_gpio3	AG24

Table 20: Pin assignments for the PIC

3.16 Power Supply

The XpressGX5LP-QE board is supplied by both the 12 V and 3.3 V of the PCI Express slot. These voltages are available on the mezzanine power supply daughter card, which is mounted on the XpressGX5LP-QE by default.

The PCI Express 12 V generates 1.5 V, 1.8 V, 2.5 V, and 0.9 V voltages, while the 3.3 V generates 3.0 V voltages, as shown below.

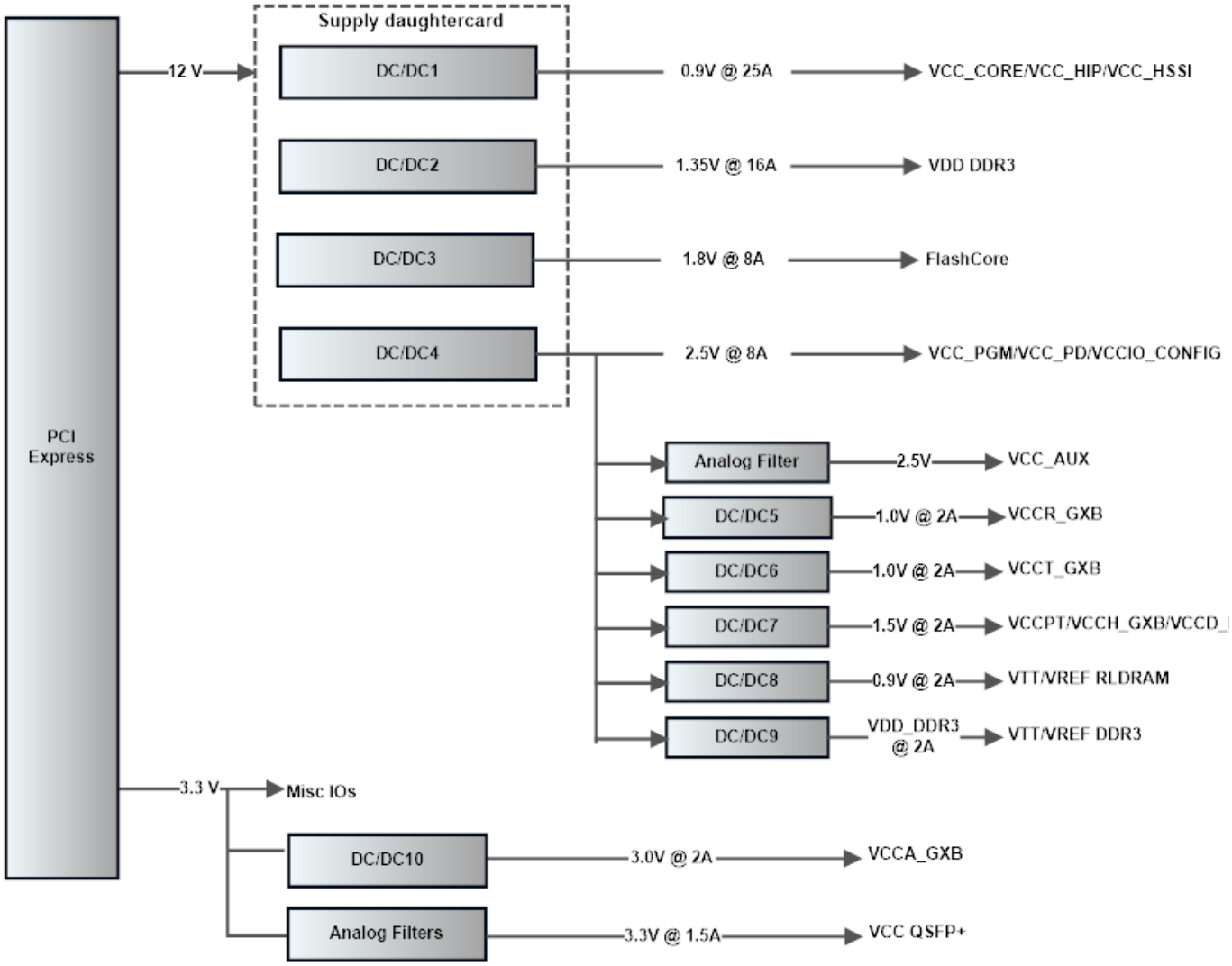


Figure 18: Power Distribution for the XpressGX5LP-QE

Note: The figures above are provided for illustrative purposes only.

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