To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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2SK3000

Silicon N Channel MOS FET
Low Frequency Power Switching

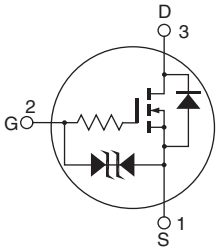
REJ03G0379-0300Z
(Previous ADE-208-585A (Z))
Rev.3.00
Jun.15.2004

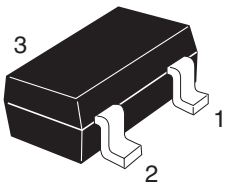
Features

- Low on-resistance
  $R_{DS(on)}$ = 0.16 Ω typ. (V_{GS} = 10 V, I_D = 450 mA)
- 4 V gate drive devices.
- Small package (MPAK)
- Expansive drain to source surge power capability

Outline

MPAK





1. Source
2. Gate
3. Drain

Note: Marking is “ZY–”.

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	40	V
Gate to source voltage	V_{GSS}	±10	V
Drain current	I_D	1.0	A
Drain peak current	$I_{D(pulse)}$ Note1	4.0	A
Reverse drain current	I_{DR}	1.0	A
Channel dissipation	Pch Note2	400	mW
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Notes: 1. PW ≤ 10 µs, duty cycle ≤ 1 %
2. When using the glass epoxy board (10 mm x 10 mm x 1 mm^t)

Electrical Characteristics

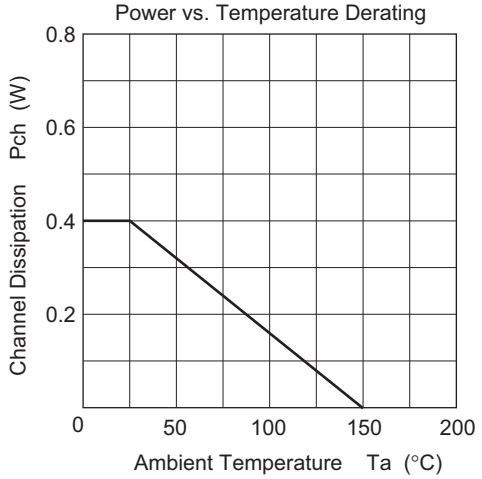
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	40	—	60	V	I_D = 100 µA, V_{GS} = 0
Drain to source voltage	$V_{DS(SUS)}$	40	—	—	V	L = 100 µH, I_D = 3 A
Gate to source breakdown voltage	$V_{(BR)GSS}$	±10	—	—	V	I_G = ±100 µA, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	1.0	µA	V_{DS} = 40 V, V_{GS} = 0
Gate to source leak current	I_{GSS}	—	—	±5	µA	V_{GS} = ±6.5V, V_{DS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.1	—	2.1	V	I_D = 10 µA, V_{DS} = 5 V
Forward transfer admittance	$\|y_{fs}\|$	0.5	1.2	—	S	I_D = 450 mA, V_{DS} = 10 V Note3
Static drain to source on state resistance	$R_{DS(on)}$	—	0.24	0.5	Ω	I_D = 450 mA, V_{GS} = 4V Note3
	$R_{DS(on)}$	—	0.16	0.3	Ω	I_D = 450 mA, V_{GS} = 10 V Note3
Input capacitance	Ciss	—	14.0	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	68	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	3.0	—	pF	f = 1 MHz
Turn-on delay time	$t_{d(on)}$	—	0.12	—	µs	V_{GS} = 4 V, I_D = 450 mA
Rise time	t_r	—	0.6	—	µs	R_L = 22 Ω
Turn-off delay time	$t_{d(off)}$	—	1.7	—	µs	
Fall time	t_f	—	1.4	—	µs	

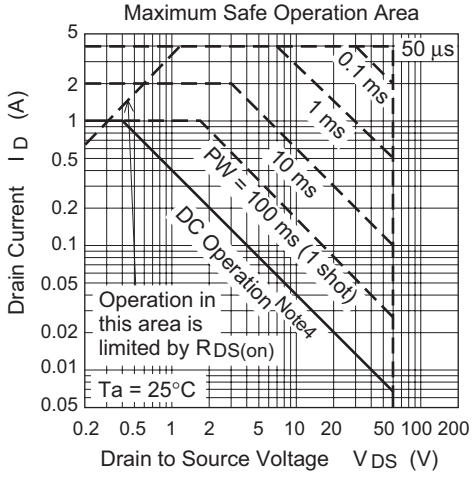
Notes: 3. Pulse test

Main Characteristics

Power vs. Temperature Derating

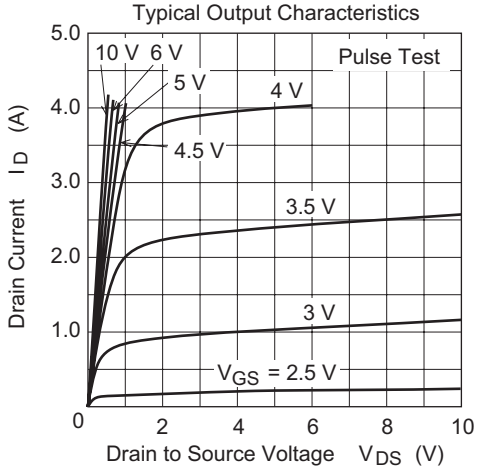


Maximum Safe Operation Area

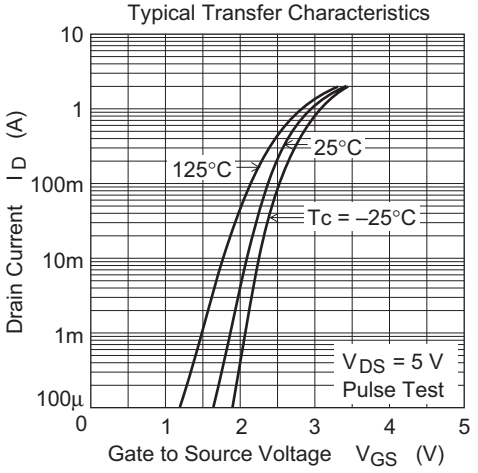


Note4 : When using the glass epoxy board (10mm x 10mm x 1mmt)

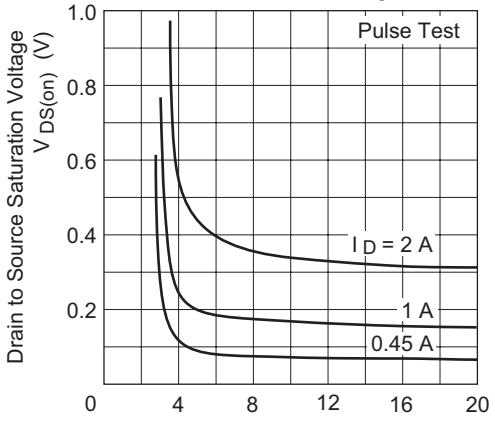
Typical Output Characteristics



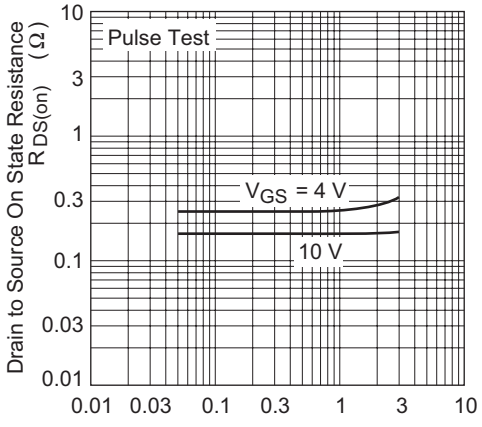
Typical Transfer Characteristics



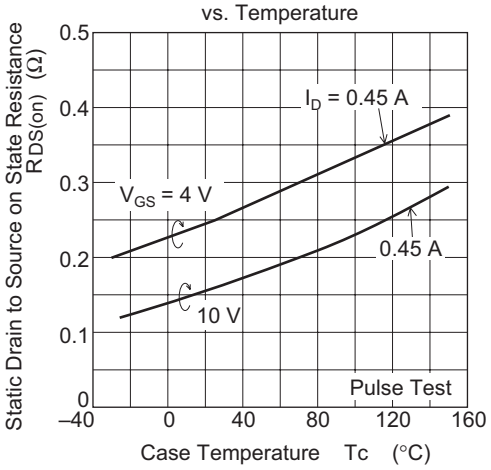
Drain to Source Saturation Voltage vs. Gate to Source Voltage



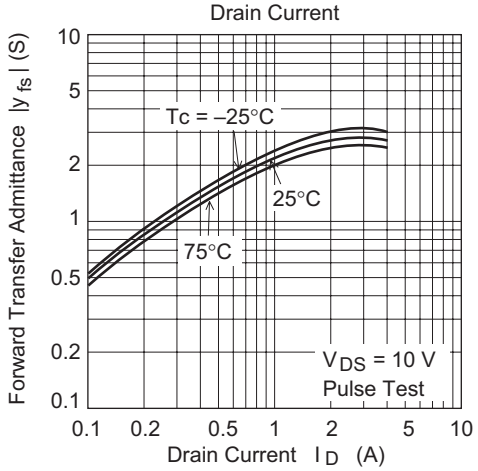
Static Drain to Source on State Resistance vs. Drain Current



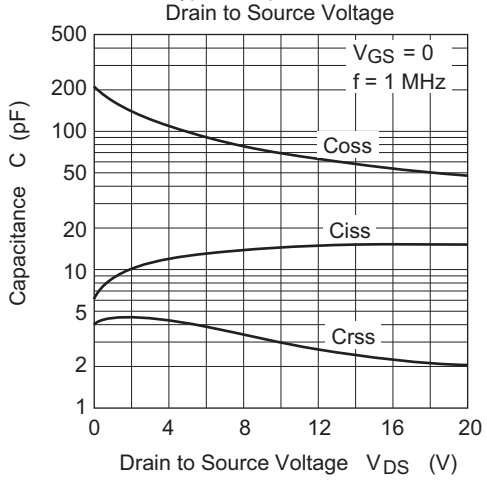
Static Drain to Source on State Resistance vs. Temperature



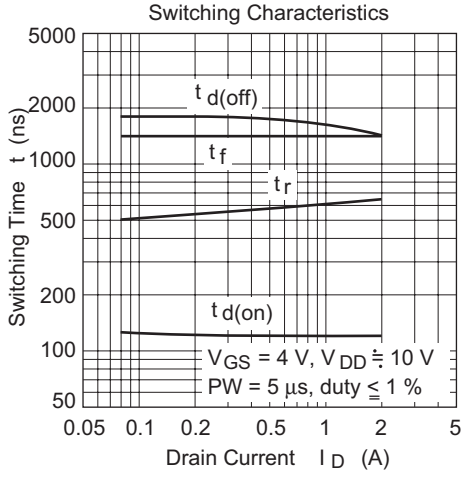
Forward Transfer Admittance vs. Drain Current



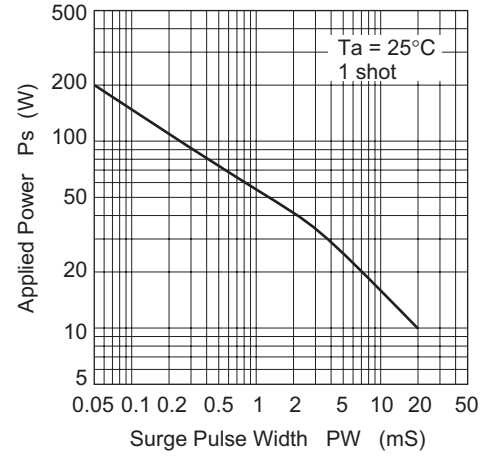
Typical Capacitance vs. Drain to Source Voltage



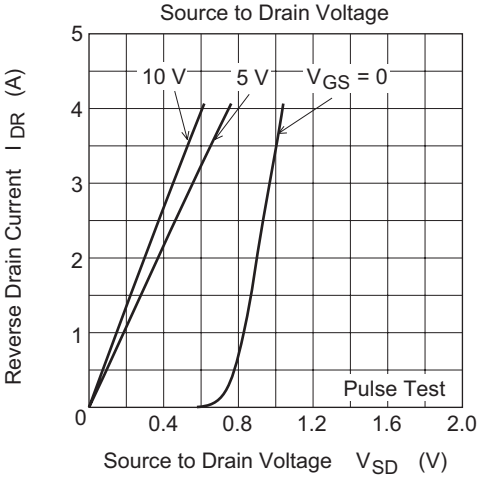
Switching Characteristics



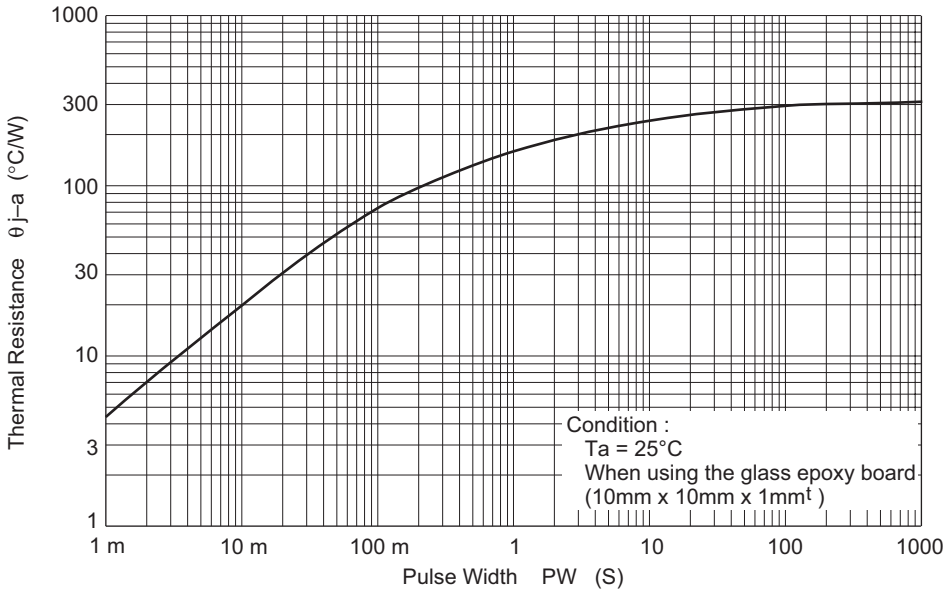
Drain to Source DiodeReverse Surge Destruction Characteristics



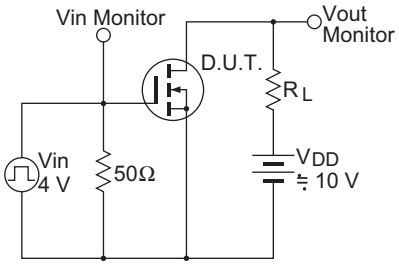
Reverse Drain Current vs. Source to Drain Voltage



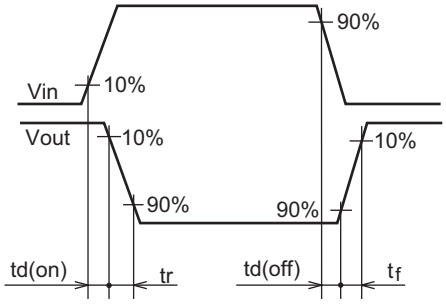
Transient Thermal Resistance



Switching Time Test Circuit



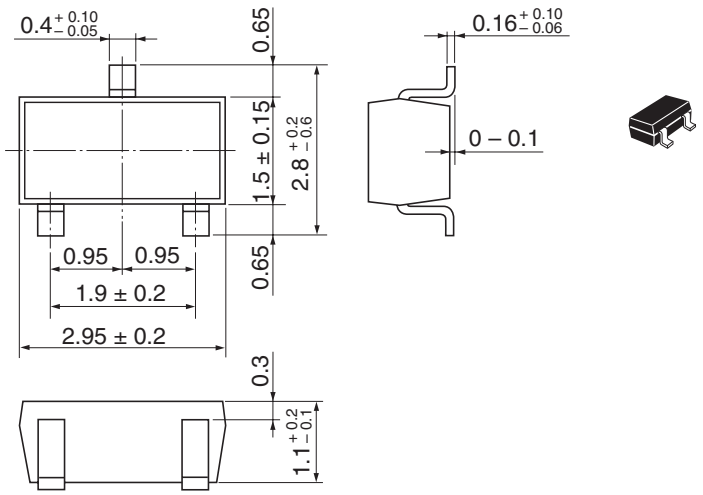
Switching Time Waveforms



Package Dimensions

As of January, 2003

Unit: mm



Package Code	MPAK(T)
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.011 g

Ordering Information

Part Name	Quantity	Shipping Container
2SK3000	3000 pcs	ϕ178 mm Reel Taping (TL)

Note: For some grades, production may be terminated. Please contact the Renesas sales office to check the state of production before ordering the product.

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