2.5V CMOS DUAL 1-TO-5 CLOCK DRIVER

IDT49FCT20805

FEATURES:

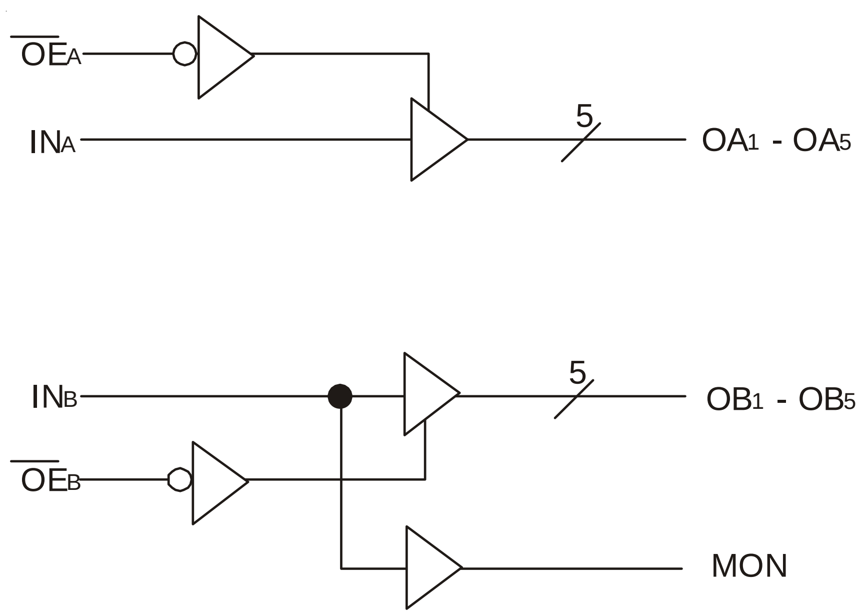
- Advanced CMOS Technology
- Guaranteed low skew < 200ps (max.)
- Very low propagation delay < 2.5ns (max)
- Very low duty cycle distortion < 270ps (max)
- Very low CMOS power levels
- Operating frequency up to 166MHz
- TTL compatible inputs and outputs
- Two independent output banks with 3-state control
- 1:5 fanout per bank
- "Heartbeat" monitor output
- V_{CC} = 2.5V ± 0.2V
- Available in SSOP and QSOP packages

DESCRIPTION:

The FCT20805 is a 2.5 volt clock driver built using advanced CMOS technology. The device consists of two banks of drivers, each with a 1:5 fanout and its own output enable control. The device has a "heartbeat" monitor for diagnostics and PLL driving. The MON output is identical to all other outputs and complies with the output specifications in this document. The FCT20805 offers low capacitance inputs.

The FCT20805 is designed for high speed clock distribution where signal quality and skew are critical. The FCT20805 also allows single point-to-point transmission line driving in applications such as address distribution, where one signal must be distributed to multiple recievers with low skew and high signal quality.

FUNCTIONAL BLOCK DIAGRAM



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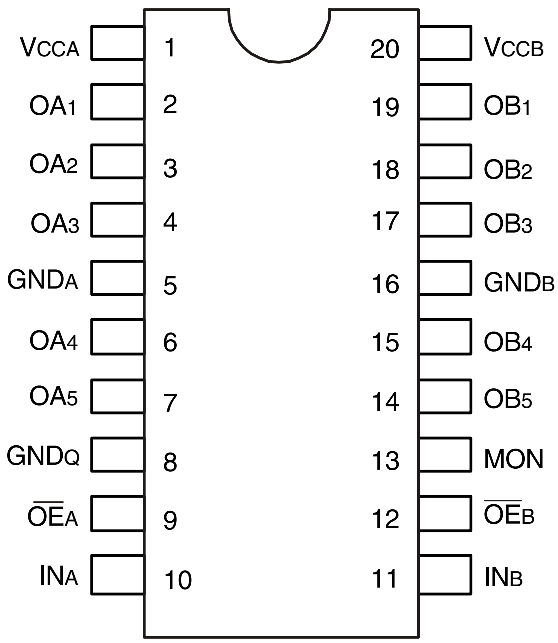
PIN CONFIGURATIONS



SSOP/ QSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
V_{CC}	Input Power Supply Voltage	–0.5 to +4.6	V
V_I	Input Voltage	–0.5 to +5.5	V
V_O	Output Voltage	–0.5 to V_{CC}+0.5	V
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	–65 to +165	°C

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3	4	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	—	6	pF

NOTE:
1. This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
OE_A, OE_B	3-State Output Enable Inputs (Active LOW)
IN_A, IN_B	Clock Inputs
OAn, OBn	Clock Outputs
MON	Monitor Output

FUNCTION TABLE (1)

Inputs		Outputs	
OE_A, OE_B	IN_A, IN_B	OAn, OBn	MON
L	L	L	L
L	H	H	H
H	L	Z	L
H	H	Z	H

NOTE:
1. H = HIGH
   L = LOW
   Z = High-Impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified
Industrial: T_A = -40°C to +85°C, V_{CC} = 2.5V ± 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level			1.7	—	5.5	V
V_{IL}	Input LOW Level			–0.5	—	0.7	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = 5.5V	—	—	±1	µA
I_{IL}	Input LOW Current	V_{CC} = Max.	V_I = GND	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	±1	
I_{OZL}	(3-State Outputs Pins)		V_O = GND	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{ODH}	Output HIGH Current	V_{CC} = 2.5V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.25V[3,4]		–15	–35	–90	mA
I_{ODL}	Output LOW Current	V_{CC} = 2.5V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.25V[3,4]		25	55	100	mA
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3,4]		–30	–50	–120	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –8mA	1.7[5]	—	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –100µA	V_{CC} - 0.2	—	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 8mA	—	0.2	0.4	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 100µA	—	—	0.2	

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 2.5V, 25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. V_{OH} = Vcc -0.6V at rated current.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.1	20	µA
ΔI_{CC}	Power Supply Current per Input HIGH	V_{CC} = Max. V_{IN} = V_{CC} –0.6V		—	35	250	µA
I_{CCD}	Dynamic Power Supply Current per Output[3]	V_{CC} = Max. C_L = 15pF All Outputs Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	65	100	µA/MHz
I_C	Total Power Supply Current[4]	V_{CC} = Max. C_L = 15pF All Outputs Toggling fi = 133MHz	V_{IN} = V_{CC} V_{IN} = GND	—	100	125	mA
			V_{IN} = V_{CC} –0.6V V_{IN} = GND	—	100	125	
		V_{CC} = Max. C_L = 15pF All Outputs Toggling fi = 166MHz	V_{IN} = V_{CC} V_{IN} = GND	—	115	150	
			V_{IN} = V_{CC} –0.6V V_{IN} = GND	—	115	150	

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 2.5V, +25°C ambient.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}\ (f_O N_O)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = V_{CC} -0.6V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_O = Output Frequency
   N_O = Number of Outputs at f_O

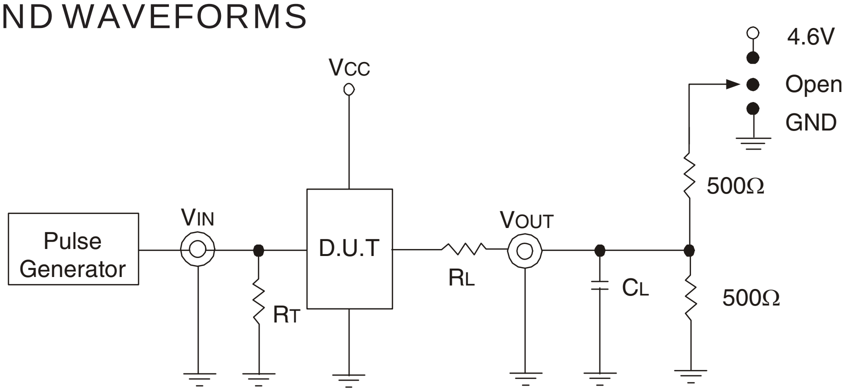
SWITCHING CHARACTERISTICS OVER OPERATING RANGE(3,4)

Symbol	Parameter	Conditions(1)	Min.(2)	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay INA to OAn, INB to OBn	C_L = 15pF f ≤ 133MHz	1	3	ns
t_R	Output Rise Time (0.8V to 2V)		—	1.5	ns
t_F	Output Fall Time (2V to 0.8V)		—	1.5	ns
$t_{SK(O)}$	Same device output pin to pin skew(5)		—	270	ps
$t_{SK(P)}$	Pulse skew(6,9)		—	270	ps
$t_{SK(PP)}$	Part to part skew(7)		—	550	ps
t_{PZL} t_{PZH}	Output Enable Time OEA to OAn, OEB to OBn		—	5.2	ns
t_{PLZ} t_{PHZ}	Output Disable Time OEA to OAn, OEB to OBn		—	5.2	ns
f_{MAX}	Input Frequency		—	133	MHz

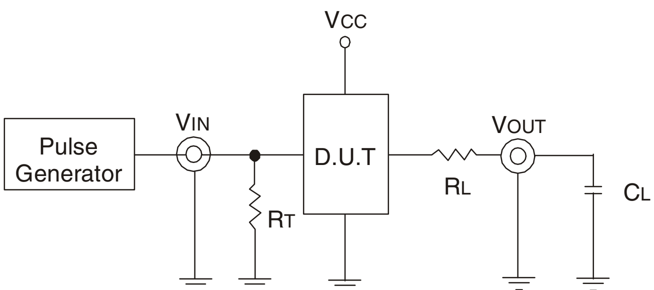
Symbol	Parameter	Conditions(1,8)	Min.(2)	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay INA to OAn, INB to OBn	C_L = 15pF 133MHz ≤ f ≤ 166MHz	0.5	2.5	ns
t_R	Output Rise Time (0.7V to 1.7V)		—	1.25	ns
t_F	Output Fall Time (1.7V to 0.7V)		—	1.25	ns
$t_{SK(O)}$	Same device output pin to pin skew(5)		—	200	ps
$t_{SK(P)}$	Pulse skew(6,9)		—	270	ps
$t_{SK(PP)}$	Part to part skew(7)		—	550	ps
t_{PZL} t_{PZH}	Output Enable Time OEA to OAn, OEB to OBn		—	5.2	ns
t_{PLZ} t_{PHZ}	Output Disable Time OEA to OAn, OEB to OBn		—	5.2	ns
f_{MAX}	Input Frequency		—	166	MHz

NOTES:
1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. t_{PLH} and t_{PHL} are production tested. All other parameters guaranteed but not production tested.
4. Propagation delay range indicated by Min. and Max. limit is due to V_{CC}, operating temperature and process parameters. These propagation delay limits do not imply skew.
5. Skew measured between all outputs under identical transitions and load conditions.
6. Skew measured is difference between propagation delay times t_{PHL} and t_{PLH} of same outputs under identical load conditions.
7. Part to part skew for all outputs given identical transitions and load conditions at identical V_{CC} levels and temperature.
8. Airflow of 1m/s is recommended for frequencies above 133MHz.
9. This parameter is measured using f = 1MHz.

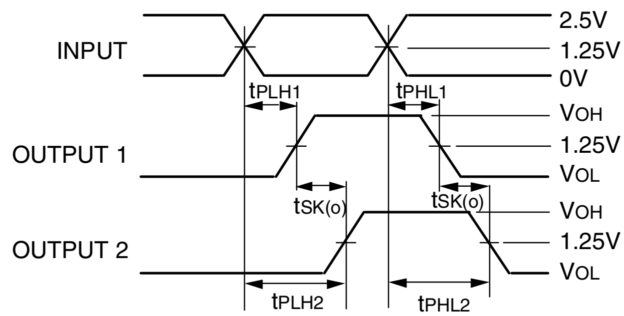
TEST CIRCUITS AND WAVEFORMS



Enable and Disable Time Circuit



C_L = 15pF Test Circuit



$t_{SK(o)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

Output Skew - $t_{SK(O)}$

SWITCH POSITION

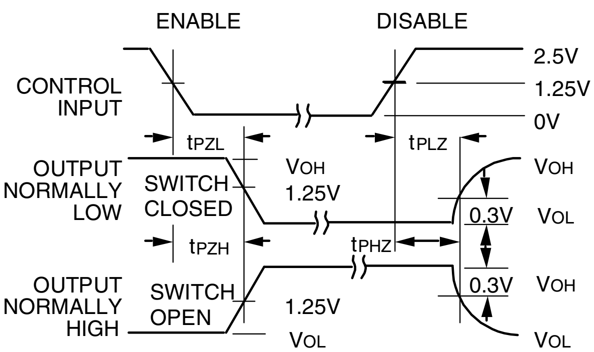
Test	Switch
Disable Low Enable Low	4.6V
Disable High Enable High	GND

TEST CONDITIONS

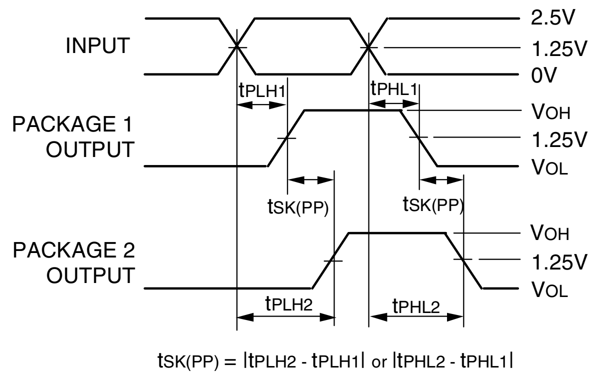
Symbol	V_{CC} = 2.5V ±0.2V	Unit
C_L	15	pF
R_T	Z_{OUT} of pulse generator	Ω
R_L	33	Ω
t_R / t_F	1 (0V to 2.5V or 2.5V to 0V)	ns

DEFINITIONS:
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.
t_R / t_F = Rise/Fall time of the input stimulus from the Pulse Generator.

TEST CIRCUITS AND WAVEFORMS



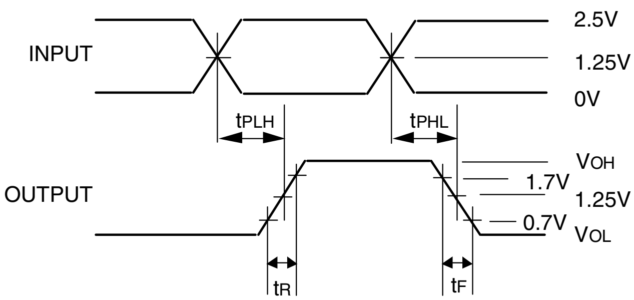
Enable and Disable Times



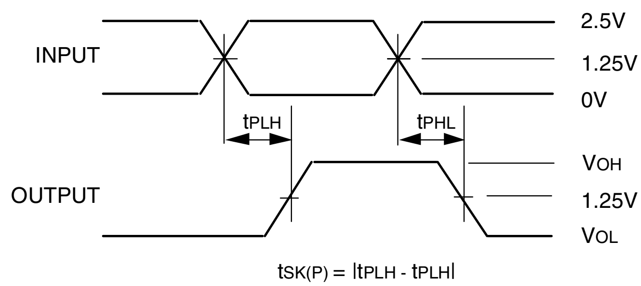
Part-to-Part Skew - tSK(PP)

NOTE:
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH

Part-to-Part Skew is for the same package and speed grade.



Propagation Delay



Pulse Skew

ORDERING INFORMATION

IDT49FCT XXXX X X

Process	I	-40°C to +85°C (Industrial)
Package	PYG	SSOP - Green
Package	QG	QSOP - Green
Device Type	20805	2.5V CMOS Dual 1-to-5 Clock Driver

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