Description

The 5PB1104 is a high-performance LVCMOS clock buffer. It has an additive phase jitter of 50fs RMS.

The 5PB1104 also supports a synchronous glitch-free output enable (OE) function to eliminate any potential intermediate incorrect output clock cycles when enabling or disabling outputs. It can operate from a 1.8V to 3.3V supply.

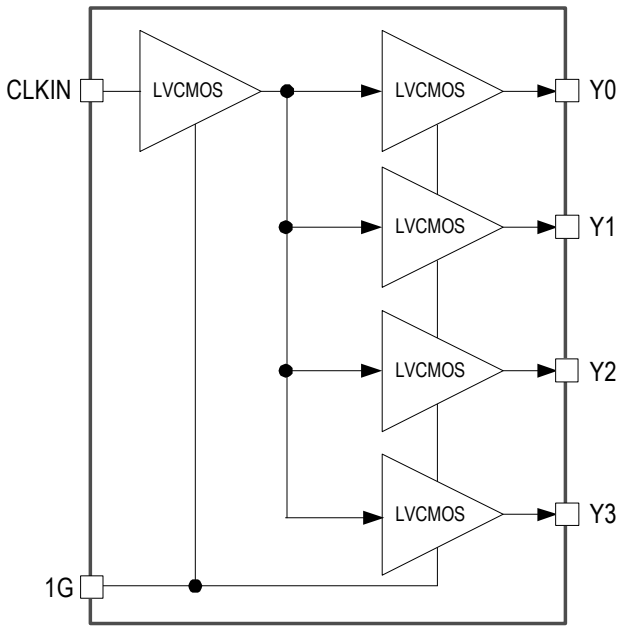
Typical Applications

- Automotive applications

Features

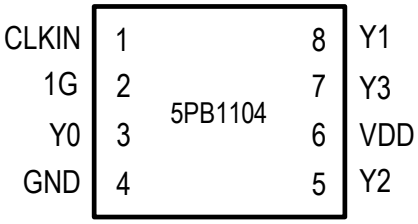
- High-performance 1:4 LVCMOS clock buffer
- Very low pin-to-pin skew: < 50ps
- Very low additive jitter: < 50fs
- Supply voltage: 1.8V to 3.3V
- 3.3V tolerant input clock
- f_{MAX} = 200MHz
- Integrated serial termination for 50Ω channel
- 2.0 × 2.0 mm 8-VFQFN package
- AEC-Q100 Grade 1 (-40°C to +125°C) and Grade 2 (-40°C to +105°C)

Block Diagram



Pin Assignments

Figure 1. Pin Assignments for 2.0 × 2.0 mm 8-VFQFN Package – Top View



Pin Descriptions

Table 1. Pin Descriptions

Number	Name	Type	Description
1	CLKIN	Input	LVCMOS clock input.
2	1G	Input	Clock output enable.
3	Y0	Output	LVCMOS clock output.
4	GND	Power	Connect to ground.
5	Y2	Output	LVCMOS clock output.
6	V_{DD}	Power	1.8V to 3.3V power supply.
7	Y3	Output	LVCMOS clock output.
8	Y1	Output	LVCMOS clock output.

Output Logic Table

Inputs		Output
CLKIN	1G	Yn
X	L	L
L	H	L
H	H	H

After at least three cycles of input clock toggling. Output Enable function is asynchronous to eliminate any intermediate incorrect output clock cycles during transition which may cause frequency peaking to the downstream device.

Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the 5PB1104 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 2. Absolute Maximum Ratings

Item	Rating
Supply Voltage, V_{DD}	3.8V
Output Enable and All Outputs	-0.4 V to V_{DD} + 0.5 V
Input Voltage, CLKIN	-0.4 V to 3.465V
Ambient Operating Temperature (Grade 1)	-40 to +125°C
Ambient Operating Temperature (Grade 2)	-40 to +105°C
Storage Temperature	-65 to +150°C
Junction Temperature	125°C
Soldering Temperature	260°C

Thermal Characteristics

Table 3. Thermal Characteristics

Symbol	Parameter	Value	Units
θ_{JA}	Still air.	120.2	°C/W
θ_{JB}	Still air.	63.3	°C/W
θ_{JC}	Still air.	99.4	°C/W

Recommended Operating Conditions

Table 4. Recommended Operating Conditions

Parameter	Minimum	Typical	Maximum	Units
Ambient Operating Temperature (Grade 1)	-40		+125	°C
Ambient Operating Temperature (Grade 2)	-40		+105	°C
Power Supply Voltage (measured in respect to GND)	+1.71		+3.465	V

DC Electrical Characteristics

V_{DD} = 1.8V, 2.5V, or 3.3V (see tables below). T_A = -40°C to 125°C unless stated otherwise.

Table 5. DC Electrical Characteristics – V_{DD} = 1.8V ±5%

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Operating Voltage		1.71	1.8	1.89	V
V_{IH}	Input High Voltage, CLKIN [1]		0.7 × V_{DD}			V
V_{IL}	Input Low Voltage, CLKIN [1]				0.3 × V_{DD}	V
V_{IH}	Input High Voltage, 1G		1.6		V_{DD}	V
V_{IL}	Input Low Voltage, 1G				0.6	V
V_{OH}	Output High Voltage	I_{OH} = -5mA.	1.2			V
V_{OL}	Output Low Voltage	I_{OL} = 5mA.			0.45	V
Z_O	Nominal Output Impedance			50		Ω
C_{IN}	Input Capacitance	CLKIN, 1G pin.		5		pF
I_{DD}	Operating Supply Current	0.001MHz, C_L = 5pF.		0.7	1	mA
		0.008MHz, C_L = 5pF.		0.7	1	mA
		40MHz, C_L = 5pF.		11	13	mA
		100MHz, C_L = 5pF.		25	30	mA
		156.25MHz, C_L = 5pF.		37	47	mA
		200MHz, C_L = 5pF.		39	57	mA

[1] Nominal switching threshold is V_{DD}/2.

Table 6. DC Electrical Characteristics – V_{DD} = 2.5V ±5%

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Operating Voltage		2.375	2.5	2.625	V
V_{IH}	Input High Voltage, CLKIN [1]		0.7 × V_{DD}			V
V_{IL}	Input Low Voltage, CLKIN [1]				0.3 × V_{DD}	V
V_{IH}	Input High Voltage, 1G		1.8		V_{DD}	V
V_{IL}	Input Low Voltage, 1G				0.7	V
V_{OH}	Output High Voltage	I_{OH} = -8mA.	1.6			V
V_{OL}	Output Low Voltage	I_{OL} = 8mA.			0.625	V
Z_O	Nominal Output Impedance			50		Ω
C_{IN}	Input Capacitance	CLKIN, 1G pin.		5		pF

Table 6. DC Electrical Characteristics – V_{DD} = 2.5V ±5% (Cont.)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
I_{DD}	Operating Supply Current	0.001MHz, C_L = 5pF.		0.9	1.3	mA
		0.008MHz, C_L = 5pF.		0.9	1.3	mA
		40MHz, C_L = 5pF.		15	17	mA
		100MHz, C_L = 5pF.		35	42	mA
		156.25MHz, C_L = 5pF.		52	67	mA
		200MHz, C_L = 5pF.		56	80	mA

[1] Nominal switching threshold is $V_{DD}/2$.

Table 7. DC Electrical Characteristics – V_{DD} = 3.3V ±5%

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Operating Voltage		3.135	3.3	3.465	V
V_{IH}	Input High Voltage, CLKIN [1]		0.7 × V_{DD}			V
V_{IL}	Input Low Voltage, CLKIN [1]				0.3 × V_{DD}	V
V_{IH}	Input High Voltage, 1G		2		V_{DD}	V
V_{IL}	Input Low Voltage, 1G				0.8	V
V_{OH}	Output High Voltage	I_{OH} = -12mA.	2.1			V
V_{OL}	Output Low Voltage	I_{OL} = 12mA.			0.825	V
Z_O	Nominal Output Impedance			50		Ω
C_{IN}	Input Capacitance	CLKIN, 1G pin.		5		pF
I_{DD}	Operating Supply Current	0.001MHz, C_L = 5pF.		1.2	1.7	mA
		0.008MHz, C_L = 5pF.		1.2	1.7	mA
		40MHz, C_L = 5pF.		19	22	mA
		100MHz, C_L = 5pF.		45	54	mA
		156.25MHz, C_L = 5pF.		67	87	mA
		200MHz, C_L = 5pF.		75	107	mA

[1] Nominal switching threshold is $V_{DD}/2$.

AC Electrical Characteristics

V_{DD} = 1.8V, 2.5V, or 3.3V (see tables below). T_A = -40°C to 125°C unless stated otherwise.

Table 8. AC Electrical Characteristics – V_{DD} = 1.8V ±5%

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
	Input Frequency		0		200	MHz
t_{OR}	Output Rise Time (5pF load)	0.36V to 1.44V, C_L = 5pF.		0.65	1.2	ns
t_{OF}	Output Fall Time (5pF load)	1.44V to 0.36V, C_L = 5pF.		0.65	1.2	ns
$t_{START-UP}$	Start-up Time	Part start-up time for valid outputs after V_{DD} ramp-up.			3	ms
	Propagation Delay [1]		1.6	2.3	3.4	ns
	Buffer Additive Phase Jitter, RMS	156.25MHz, Integration Range: 12kHz–20MHz.			0.06	ps
	Output to Output Skew	Rising edges at V_{DD}/2 [2]		35	50	ps
	Device to Device Skew	Rising edges at V_{DD}/2.			200	ps
t_{EN}	Output Enable Time	$C_L \leq$ 5pF.			3	cycles
t_{DIS}	Output Disable Time	$C_L \leq$ 5pF.			3	cycles
t_{DC}	Duty Cycle [3]			50		%

Table 9. AC Electrical Characteristics – V_{DD} = 2.5V ±5%

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
	Input Frequency		0		200	MHz
t_{OR}	Output Rise Time (5pF load)	0.5V to 2.0V, C_L = 5pF.		0.63	1.2	ns
t_{OF}	Output Fall Time (5pF load)	2.0V to 0.5V, C_L = 5pF.		0.63	1.2	ns
$t_{START-UP}$	Start-up Time	Part start-up time for valid outputs after V_{DD} ramp-up.			3	ms
	Propagation Delay [1]		2.0	2.9	4.5	ns
	Buffer Additive Phase Jitter, RMS	156.25MHz, Integration Range: 12kHz–20MHz.			0.06	ps
	Output to Output Skew	Rising edges at V_{DD}/2 [2]		35	50	ps
	Device to Device Skew	Rising edges at V_{DD}/2.			200	ps
t_{EN}	Output Enable Time	$C_L \leq$ 5pF.			3	cycles
t_{DIS}	Output Disable Time	$C_L \leq$ 5pF.			3	cycles
t_{DC}	Duty Cycle [3]			50		%

Table 10. AC Electrical Characteristics – V_{DD} = 3.3V ±5%

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
	Input Frequency		0		200	MHz
t_{OR}	Output Rise Time (5pF load)	0.66V to 2.64V, C_L = 5pF.		0.61	1.2	ns
t_{OF}	Output Fall Time (5pF load)	2.64V to 0.66V, C_L = 5pF.		0.61	1.2	ns
$t_{START-UP}$	Start-up Time	Part start-up time for valid outputs after V_{DD} ramp-up.			3	ms
	Propagation Delay [1]		1.7	2.3	3.4	ns
	Buffer Additive Phase Jitter, RMS	156.25MHz, Integration Range: 12kHz–20MHz.			0.05	ps
	Output to Output Skew	Rising edges at $V_{DD}/2$ [2]		35	50	ps
	Device to Device Skew	Rising edges at $V_{DD}/2$.			200	ps
t_{EN}	Output Enable Time	$C_L \leq$ 5pF.			3	cycles
t_{DIS}	Output Disable Time	$C_L \leq$ 5pF.			3	cycles
t_{DC}	Duty Cycle [3]			50		%

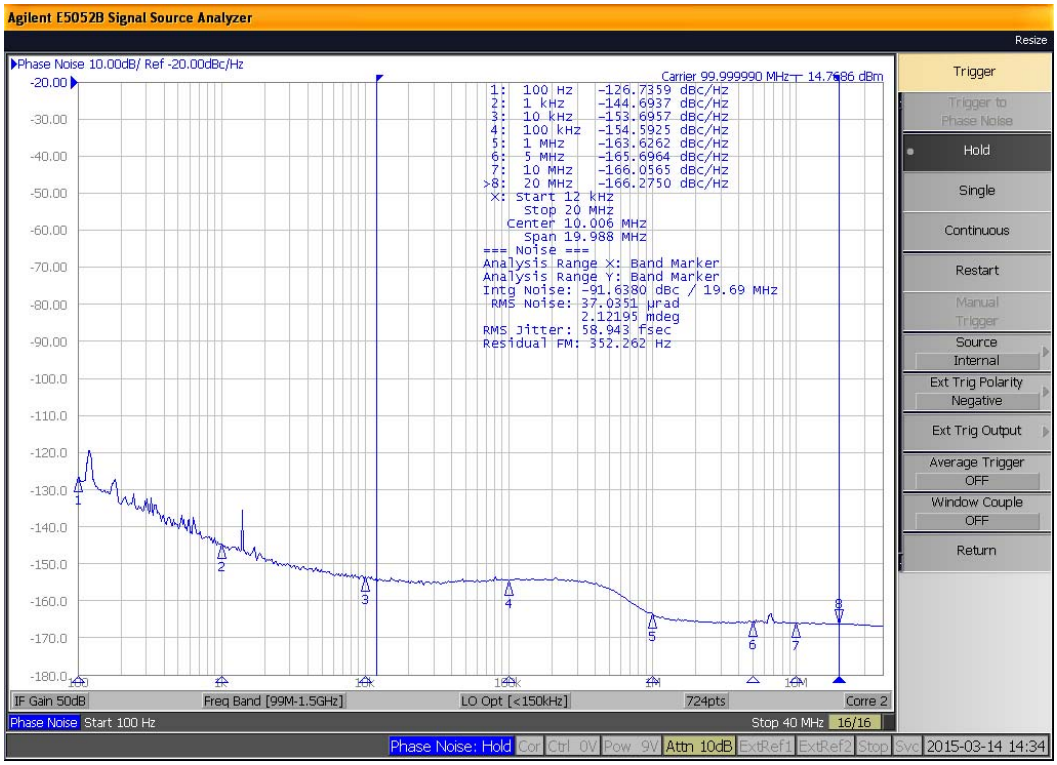
[1] With rail-to-rail input clock.

[2] Between any 2 outputs with equal loading.

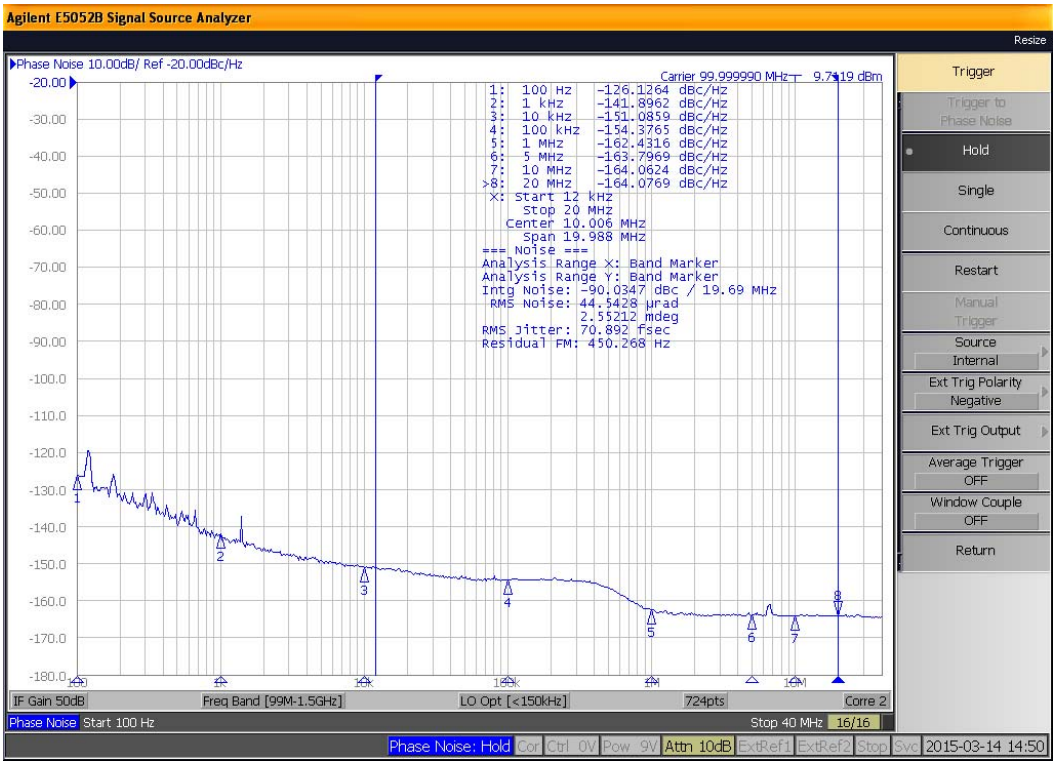
[3] Duty cycle on outputs will match incoming clock duty cycle when V_{IH} on CLKIN pin equals V_{DD} power supply voltage. Consult IDT for tight duty cycle clock generators.

Phase Noise Plots

The phase noise plots show the low additive jitter of the 5PB1104 high-performance buffer. With an integration range of 12kHz to 20MHz, the reference input has about 58.9fs of RMS phase jitter while the output of 5PB1104 has about 70.9fs of RMS phase jitter. This results in a low additive phase jitter of only 39fs.

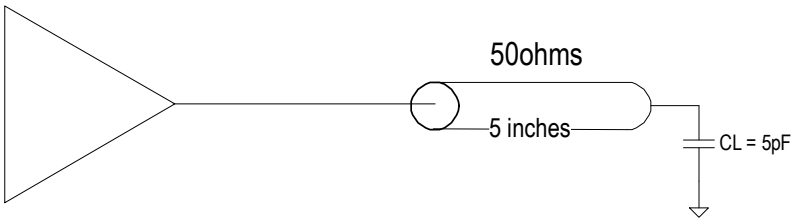


Reference Phase Noise 58.9fs (12kHz to 20MHz)



Output Phase Noise 70.9fs (12kHz to 20MHz)

Test Load and Circuit

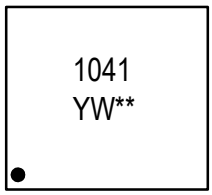


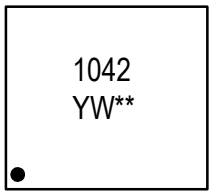
Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

www.idt.com/document/psc/cmg8-package-outline-drawing-20-x-20-x-05-mm-body-05mm-pitch-dfn

Marking Diagrams





- Line 1: truncated part number; last number is the temperature grade: 1 = Grade 1; 2 = Grade 2.
- "YW" is the last digit of the year and work week that the part was assembled.
- "**" denotes the lot sequence number.

Ordering Information

Orderable Part Number	Package	Carrier Type	Temperature
5PB1104CMG1	2.0 × 2.0 mm, 0.5mm pitch 8-VFQFN	Tubes	-40° to +125°C
5PB1104CMG18	2.0 × 2.0 mm, 0.5mm pitch 8-VFQFN	Reel	-40° to +125°C
5PB1104CMG2	2.0 × 2.0 mm, 0.5mm pitch 8-VFQFN	Tubes	-40° to +105°C
5PB1104CMG28	2.0 × 2.0 mm, 0.5mm pitch 8-VFQFN	Reel	-40° to +105°C

Revision History

Revision Date	Description of Change
October 15, 2018	Initial release.

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