PRODUCT DISCONTINUATION NOTICE - LAST TIME BUY EXPIRES SEPEMBER 7, 2016 DATA SHEET

General Description

The IDT5T9302I 2.5V differential clock buffer is a user-selectable differential input to two LVDS outputs. The fanout from a differential input to two LVDS outputs reduces loading on the preceding driver and provides an efficient clock distribution network. The IDT5T9302I can act as a translator from a differential HSTL, eHSTL, LVEPECL (2.5V), LVPECL (3.3V), CML, or LVDS input to LVDS outputs. A single-ended 3.3V / 2.5V LVTTL input can also be used to translate to LVDS outputs. The redundant input capability allows for an asynchronous change-over from a primary clock source to a secondary clock source. Selectable reference inputs are controlled by SEL.

The IDT5T9302I outputs can be asynchronously enabled/ disabled. When disabled, the outputs will drive to the value selected by the GL pin. Multiple power and grounds reduce noise.

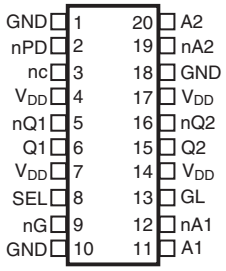
Applications

- Clock distribution

Features

- Guaranteed low skew: 50ps (maximum)
- Very low duty cycle distortion: 125ps (maximum)
- High speed propagation delay: 1.5ns (maximum)
- Up to 450MHz operation
- Selectable inputs
- Hot insertable and over-voltage tolerant inputs
- 3.3V/2.5V LVTTL, HSTL eHSTL, LVEPECL (2.5V), LVPECL (3.3V), CML or LVDS input interface
- Selectable differential inputs to two LVDS outputs
- Power-down mode
- 2.5V V_{DD}
- -40°C to 85°C ambient operating temperature
- Available in Lead-free (RoHS 6) package
- **Not Recommended For New Designs**
- **For functional replacement part use 8SLVP1102**

Pin Assignment



IDT5T9302I

20-Lead TSSOP, E-Pad 4.4mm x 6.5mm x 0.925mm package body G Package Top View

Block Diagram

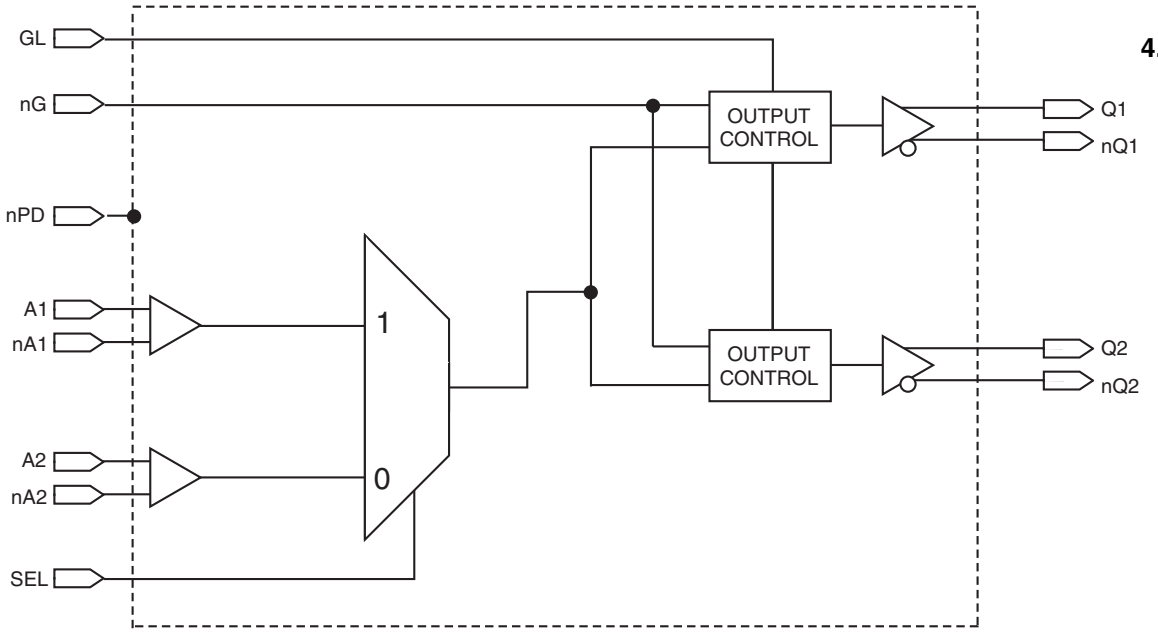


Table 1. Pin Descriptions

Name	Type		Description
A[1:2]	Input	Adjustable (1, 4)	Clock input. A[1:2] is the "true" side of the differential clock input.
nA[1:2]	Input	Adjustable (1, 4)	Complementary clock inputs. nA[1:2] is the complementary side of A[1:2]. For LVTTL single-ended operation, nA[1:2]should be set to the desired toggle voltage for A[1:2]: 3.3V LVTTL V_{REF} = 1650mV 2.5V LVTTL V_{REF} = 1250mV
nG	Input	LVTTL	Gate control for differential outputs Q1, nQ1 and Q2, nQ2. When nG is LOW, the differential outputs are active. When nG is HIGH, the differential outputs are asynchronously driven to the level designated by GL(2). See Table 3A.
GL	Input	LVTTL	Specifies output disable level. If HIGH, "true" outputs disable HIGH and "complementary" outputs disable LOW. If LOW, "true" outputs disable LOW and "complementary" outputs disable HIGH. See Table 3A.
Q[1:2]	Output	LVDS	Clock outputs.
nQ[1:2]	Output	LVDS	Complementary clock outputs.
SEL	Input	LVTTL	Reference clock select. When LOW, selects A2 and nA2. When HIGH, selects A1 and nA1. See Table 3B.
nPD	Input	LVTTL	Power-down control. Shuts off entire chip. If LOW, the device goes into low power mode. Inputs and outputs are disabled. Both "true" and “complementary” outputs will pull to V_{DD}. Set HIGH for normal operation.(3)
V_{DD}		Power	Power supply for the device core and inputs.
GND		Power	Power supply return for all power.
nc	Unused		No connect; recommended to connect to GND.

NOTES:
1. Inputs are capable of translating the following interface standards:
   Single-ended 3.3V and 2.5V LVTTL levels
   Differential HSTL and eHSTL levels
   Differential LVEPECL (2.5V) and LVPECL (3.3V) levels
   Differential LVDS levels
   Differential CML levels
2. Because the gate controls are asynchronous, runt pulses are possible. It is the user's responsibility to either time the gate control signals to minimize the possibility of runt pulses or be able to tolerate them in down stream circuitry.
3. It is recommended that the outputs be disabled before entering power-down mode. It is also recommended that the outputs remain disabled until the device completes power-up after asserting nPD.
4. The user must take precautions with any differential input interface standard being used in order to prevent instability when there is no input signal.

Table 2. Pin Characteristics (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			3		pF

NOTE: This parameter is measured at characterization but not tested.

Function Tables

Table 3A. Gate Control Output Table

Control Output		Outputs	
GL	**nG**	**Q[1:2]**	**nQ[1:2]**
0	0	Toggling	Toggling
0	1	LOW	HIGH
1	0	Toggling	Toggling
1	1	HIGH	LOW

Table 3B. Input Selection Table

Selection SEL pin	Inputs
0	A2, nA2
1	A1, nA1

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Power Supply Voltage, V_{DD}	-0.5V to +3.6V
Input Voltage, V_I	-0.5V to +3.6V
Output Voltage, V_O Not to exceed 3.6V	-0.5 to V_{DD} +0.5V
Storage Temperature, T_{STG}	-65°C to 150°C
Junction Temperature, T_J	150°C

Recommended Operating Range

Symbol	Description	Minimum	Typical	Maximum	Units
T_A	Ambient Operating Temperature	-40	+25	+85	°C
V_{DD}	Internal Power Supply Voltage	2.3	2.5	2.7	V

DC Electrical Characteristics

Table 4A. LVDS Power Supply DC Characteristics(1), T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical(2)	Maximum	Units
I_{DDQ}	Quiescent V_{DD} Power Supply Current	V_{DD} = Max., All Input Clocks = LOW(2); Outputs enabled			240	mA
I_{TOT}	Total Power V_{DD} Supply Current	V_{DD} = 2.7V; $F_{REFERENCE}$ Clock = 450MHz			250	mA
I_{nPD}	Total Power Down Supply Current	nPD = LOW			5	mA

NOTE 1: These power consumption characteristics are for all the valid input interfaces and cover the worst case conditions.
NOTE 2: The true input is held LOW and the complementary input is held HIGH.

Table 4B. LVCMOS/LVTTL DC Characteristics(1), T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical(2)	Maximum	Units
I_{IH}	Input High Current	V_{DD} = = 2.7V			±5	µA
I_{IL}	Input Low Current	V_{DD} = = 2.7V			±5	µA
V_{IK}	Clamp Diode Voltage	V_{DD} = 2.3V, I_{IN} = -18mA		-0.7	-1.2	V
V_{IN}	DC Input Voltage		-0.3		3.6	V
V_{IH}	DC Input High Voltage		1.7			V
V_{IL}	DC Input Low Voltage				0.7	V
V_{THI}	DC Input Threshold Crossing Voltage			V_{DD}/2		V
V_{REF}	Single-Ended Reference Voltage (3)	3.3V LVTTL		1.65		V
		2.5V LVTTL		1.25		V

NOTE 1: See *Recommended Operating Range* table.
NOTE 2: Typical values are at V_{DD} = 2.5V, +25°C ambient.
NOTE 3: For A[1:2] single-ended operation, nA[1:2] is tied to a DC reference voltage.

Table 4C. Differential DC Characteristics(1), T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical(2)	Maximum	Units
I_{IH}	Input High Current	V_{DD} = 2.7V			±5	µA
I_{IL}	Input Low Current	V_{DD} = 2.7V			±5	µA
V_{IK}	Clamp Diode Voltage	V_{DD} = 2.3V, I_{IN} = -18mA		-0.7	-1.2	V
V_{IN}	DC Input Voltage		-0.3		3.6	V
V_{DIF}	DC Differential Voltage(3)		0.1			V
V_{CM}	DC Common Mode Input Voltage		0.05		V_{DD}	V

NOTE 1: See *Recommended Operating Range* table.
NOTE 2: Typical values are at V_{DD} = 2.5V, +25°C ambient.
NOTE 3: V_{DIF} specifies the minimum input differential voltage (V_{TR} - V_{CP}) required for switching where V_{TR} is the "true" input level and V_{CP} is the "complement" input level. The DC differential voltage must be maintained to guarantee retaining the existing HIGH or LOW input. The AC differential voltage must be achieved to guarantee switching to a new state.
NOTE 4: V_{CM} specifies the maximum allowable range of (V_{TR} + V_{CP}) /2.

Table 4D. LVDS DC Characteristics[1], T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical[2]	Maximum	Units
$V_{OT(+)}$	Differential Output Voltage for the True Binary State		247		454	mV
$V_{OT(-)}$	Differential Output Voltage for the False Binary State		247		454	mV
ΔV_{OT}	Change in V_{OT} Between Complementary Output States				50	mV
V_{OS}	Output Common Mode Voltage (Offset Voltage)		1.125	1.2	1.375	V
ΔV_{OS}	Change in V_{OS} Between Complementary Output States				50	mV
I_{OS}	Outputs Short Circuit Current	V_{OUT+} and V_{OUT-} = 0V		12	24	mA
I_{OSD}	Differential Outputs Short Circuit Current	$V_{OUT+} = V_{OUT-}$		6	12	mA

NOTE 1: See *Recommended Operating Range* table.
NOTE 2: Typical values are at V_{DD} = 2.5V, +25°C ambient.

AC Electrical Characteristics

Table 5A. HSTL Differential Input AC Characteristics, T_A = -40°C to 85°C

Symbol	Parameter	Value	Units
V_{DIF}	Input Signal Swing[1]	1	V
V_X	Differential Input Signal Crossing Point[2]	750	mV
D_H	Duty Cycle	50	%
V_{THI}	Input Timing Measurement Reference Level[3]	Crossing Point	V
t_R / t_F	Input Signal Edge Rate[4]	2	V/ns

NOTE 1: The 1V peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the VDIF (AC) specification under actual use conditions.
NOTE 2: A 750mV crossing point level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the VX specification under actual use conditions.
NOTE 3: In all cases, input waveform timing is marked at the differential cross-point of the input signals.
NOTE 4: The input signal edge rate of 2V/ns or greater is to be maintained in the 20% to 80% range of the input waveform.

Table 5B. eHSTL AC Differential Input Characteristics, T_A = -40°C to 85°C

Symbol	Parameter	Value	Units
V_{DIF}	Input Signal Swing[1]	1	V
V_X	Differential Input Signal Crossing Point[2]	900	mV
D_H	Duty Cycle	50	%
V_{THI}	Input Timing Measurement Reference Level[3]	Crossing Point	V
t_R / t_F	Input Signal Edge Rate[4]	2	V/ns

NOTE 1: The 1V peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the VDIF (AC) specification under actual use conditions.
NOTE 2: A 900mV crossing point level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the Vx specification under actual use conditions.
NOTE 3: In all cases, input waveform timing is marked at the differential cross-point of the input signals.
NOTE 4: The input signal edge rate of 2V/ns or greater is to be maintained in the 20% to 80% range of the input waveform.

Table 5C. LVEPECL (2.5V) and LVPECL (3.3V) Differential Input AC Characteristics, T_A = -40°C to 85°C

Symbol	Parameter		Maximum	Units
V_{DIF}	Input Signal Swing[1]		732	mV
V_X	Differential Input Cross Point Voltage[2]	LVEPECL	1082	mV
		LVPECL	1880	mV
D_H	Duty Cycle		50	%
V_{THI}	Input Timing Measurement Reference Level[3]		Crossing Point	V
t_R / t_F	Input Signal Edge Rate[4]		2	V/ns

NOTE 1: The 732mV peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the VDIF (AC) specification under actual use conditions.
NOTE 2: A 1082mV LVEPECL (2.5V) and 1880 LVPECL (3.3V) crossing point level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the Vx specification under actual use conditions.
NOTE 3: In all cases, input waveform timing is marked at the differential cross-point of the input signals.
NOTE 4: The input signal edge rate of 2V/ns or greater is to be maintained in the 20% to 80% range of the input waveform.

Table 5D. LVDS Differential Input AC Characteristics, T_A = -40°C to 85°C

Symbol	Parameter	Maximum	Units
V_{DIF}	Input Signal Swing[1]	400	mV
V_X	Differential Input Cross Point Voltage[2]	1.2	V
D_H	Duty Cycle	50	%
V_{THI}	Input Timing Measurement Reference Level[3]	Crossing Point	V
t_R / t_F	Input Signal Edge Rate[4]	2	V/ns

NOTE 1: The 400mV peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the VDIF (AC) specification under actual use conditions.
NOTE 2: A 1.2V crossing point level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the Vx specification under actual use conditions.
NOTE 3: In all cases, input waveform timing is marked at the differential cross-point of the input signals.
NOTE 4: The input signal edge rate of 2V/ns or greater is to be maintained in the 20% to 80% range of the input waveform.

Table 5E. AC Differential Input Characteristics[1], T_A = -40°C to 85°C

Symbol	Parameter	Minimum	Typical	Maximum	Units
V_{DIF}	AC Differential Voltage[2]	0.1		3.6	V
V_X	Differential Input Cross Point Voltage	0.05		V_{DD}	V
V_{CM}	Common Mode Input Voltage Range[3]	0.05		V_{DD}	V
V_{IN}	Input Voltage	-0.3		3.6	V/ns

NOTE 1: The output will not change state until the inputs have crossed and the minimum differential voltage range defined by V_{DIF} has been met or exceeded.
NOTE 2: V_{DIF} specifies the minimum input voltage ($V_{TR} – V_{CP}$) required for switching where V_{TR} is the “true” input level and V_{CP} is the “complement” input level. The AC differential voltage must be achieved to guarantee switching to a new state.
NOTE 3: V_{CM} specifies the maximum allowable range of ($V_{TR} + V_{CP}$) /2.

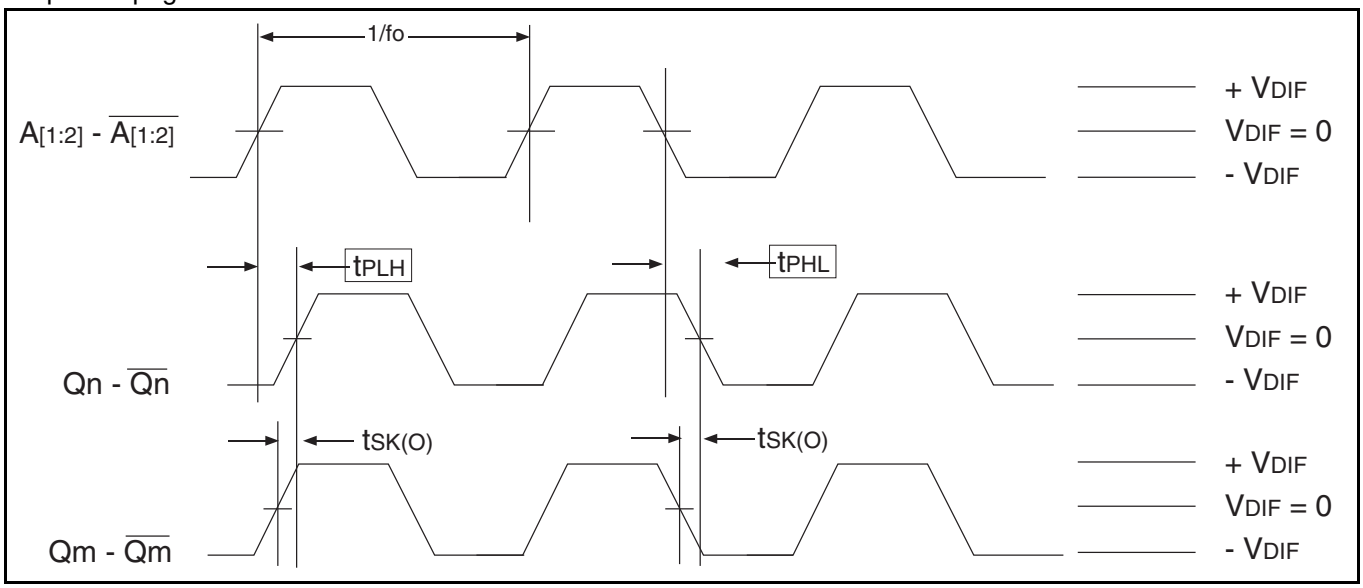
Table 5E. AC Characteristics[1,5], T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
*t*sk(o)	Same Device Output Pin-to-Pin Skew [2]				50	ps
*t*sk(p)	Pulse Skew[3]				125	ps
*t*sk(pp)	Part-to-Part Skew[4]				350	ps
tp_{LH}	Propagation Delay, Low-to-High	A[1:2]/nA[1:2] Crosspoint to Qx/nQx Crosspoint		1.35	1.5	ns
tp_{HL}	Propagation Delay, High-to-Low			1.35	1.5	ns
fo	Output Frequency [6]				450	MHz
t_{PGE}	Output Gate Enable Crossing VTHI-to-Qx/Qx Crosspoint				3.5	ns
t_{PGD}	Output Gate Enable Crossing VTHI-to-Qx/Qx Crosspoint Driven to Designated Level				3.5	ns
t_{PWRDN}	nPD Crossing V_{THI}-to-Qx = V_{DD}, Qx = V_{DD}				100	µS
t_{PWRUP}	Output Gate Disable Crossing V_{THI} to Qx/nQx Driven to Designated Level				100	µS

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: AC propagation measurements should not be taken within the first 100 cycles of startup.
NOTE 2: Skew measured between crosspoints of all differential output pairs under identical input and output interfaces, transitions and load conditions on any one device.
NOTE 3: Skew measured is the difference between propagation delay times tp_{HL} and tp_{LH} of any differential output pair under identical input and output interfaces, transitions and load conditions on any one device.
NOTE 4: Skew measured is the magnitude of the difference in propagation times between any single differential output pair of two devices, given identical transitions and load conditions at identical V_{DD} levels and temperature.
NOTE 5: All parameters are tested with a 50% input duty cycle.
NOTE 6: Guaranteed by design but not production tested.

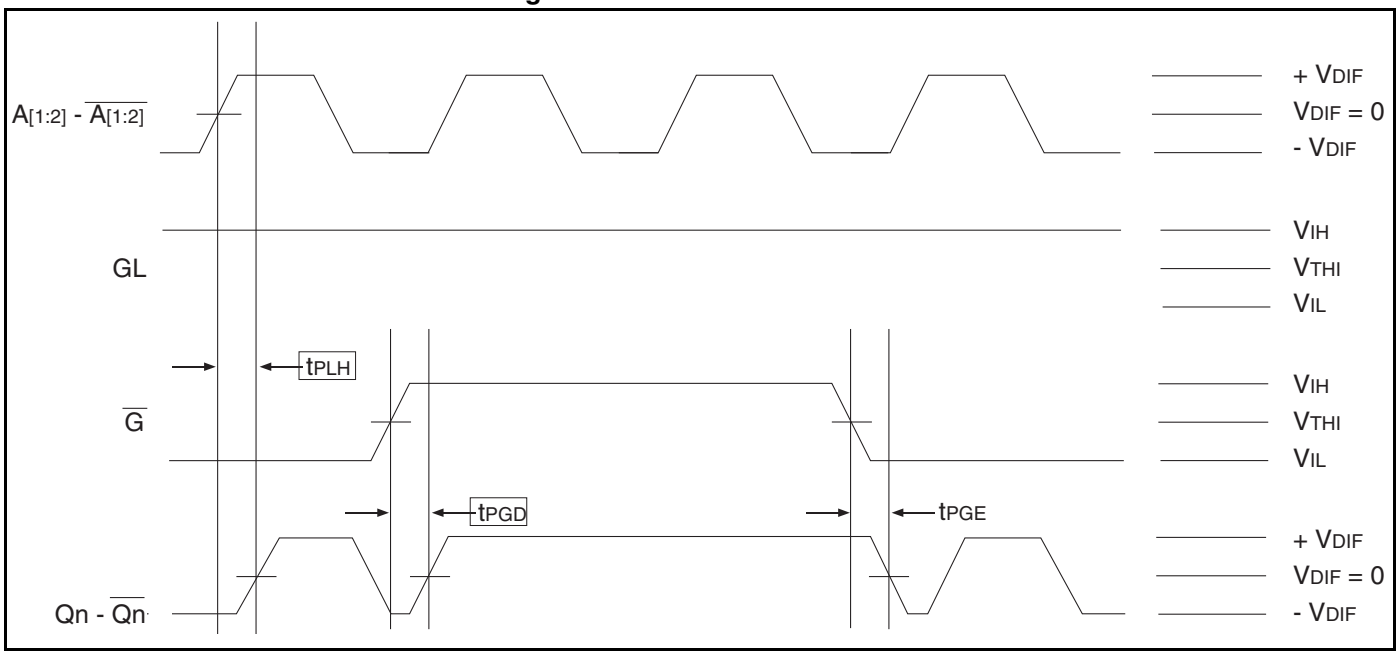
Differential AC Timing Waveforms

Output Propagation and Skew Waveforms



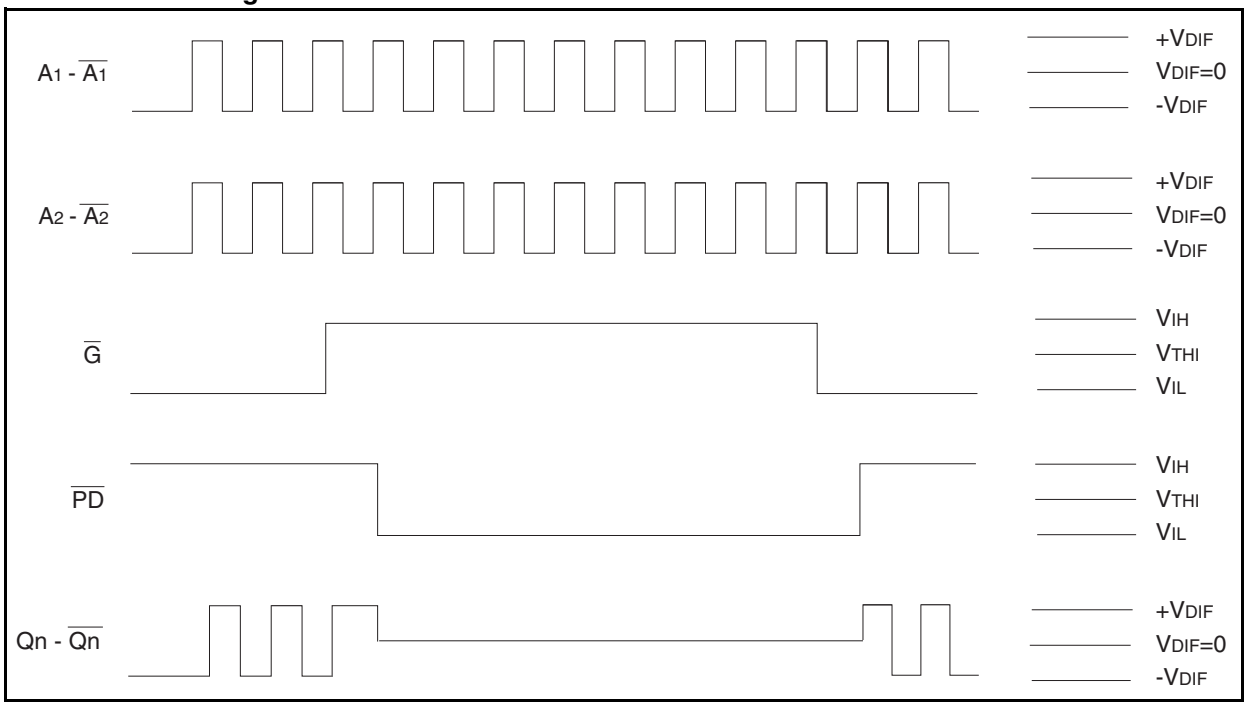
NOTE 1: Pulse skew is calculated using the following expression:
$t_{sk(p)} = |tp_{HL} - tp_{LH}|$
Note that the tp_{HL} and tp_{LH} shown above are not valid measurements for this calculation because they are not taken from the same pulse.
NOTE 2: AC propagation measurements should not be taken within the first 100 cycles of startup.

Differential Gate Disabled/Enable Showing Runt Pulse Generation



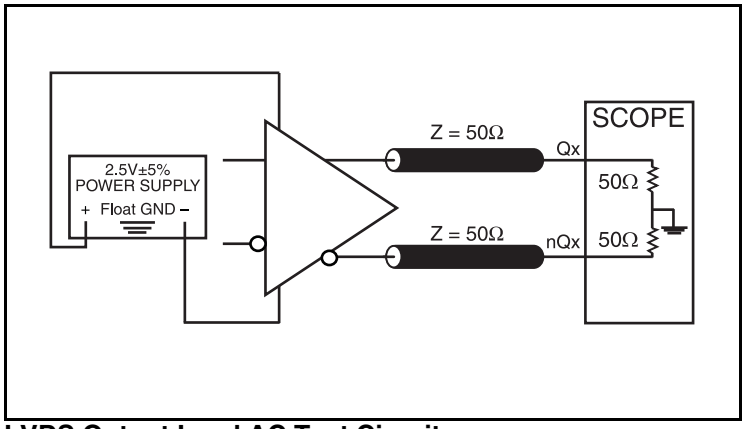
NOTE 1: As shown, it is possible to generate runt pulses on gate disable and enable of the outputs. It is the user's responsibility to time the nG signal to avoid this problem.

Power Down Timing

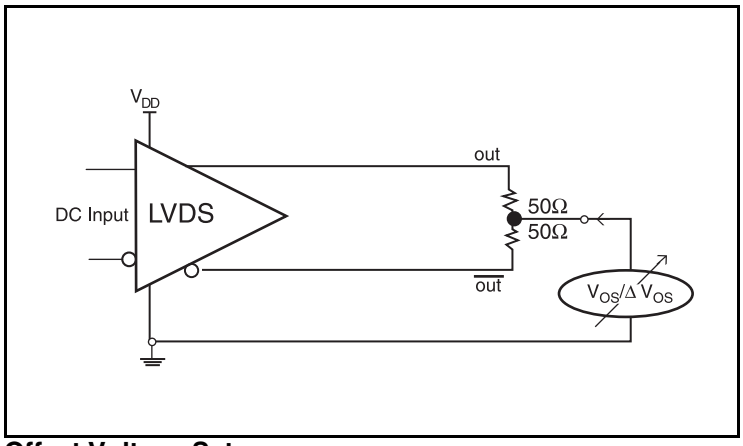


NOTE 1: It is recommended that outputs be disabled before entering power-down mode. It is also recommended that the outputs remain disabled until the device completes power-up after asserting nPD.
NOTE 2: The *Power Down Timing* diagram assumes that GL is HIGH.
NOTE 3: It should be noted that during power-down mode, the outputs are both pulled to V_{DD}. In the *Power Down Timing* diagram this is shown when Qx/nQx goes to $V_{DIF} = 0$.

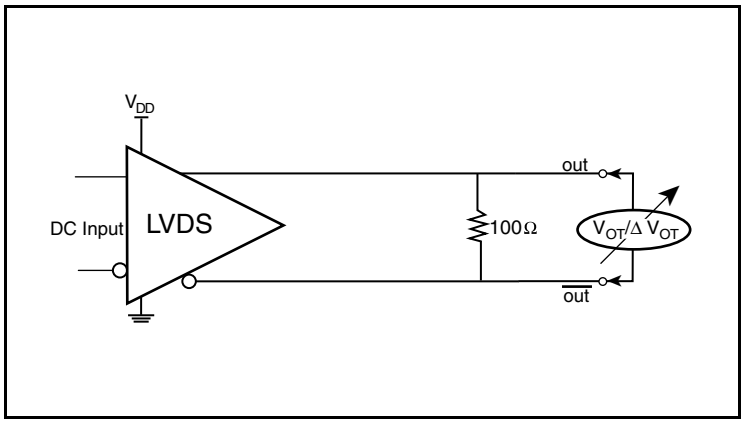
Parameter Measurement Information



LVDS Output Load AC Test Circuit



Offset Voltage Setup



Differential Output Voltage Setup

Applications Information

EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 1.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.

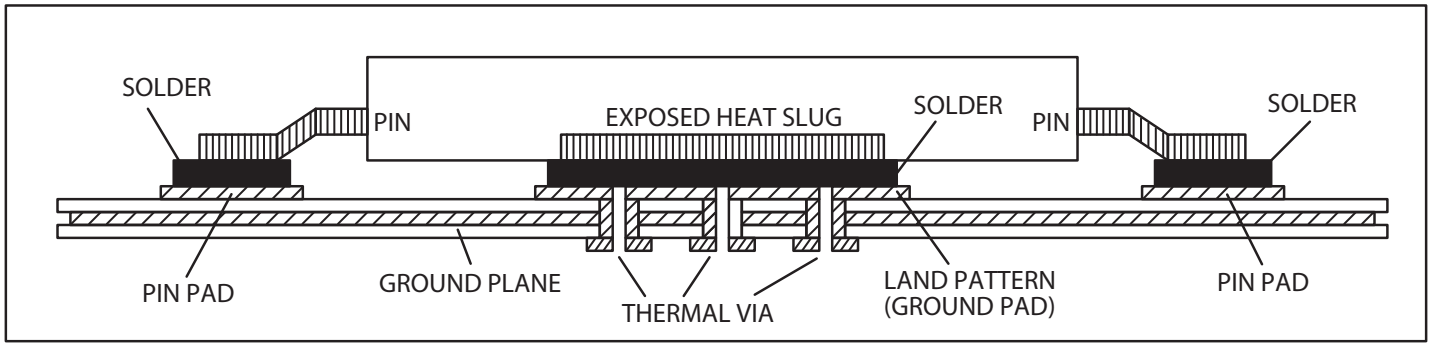


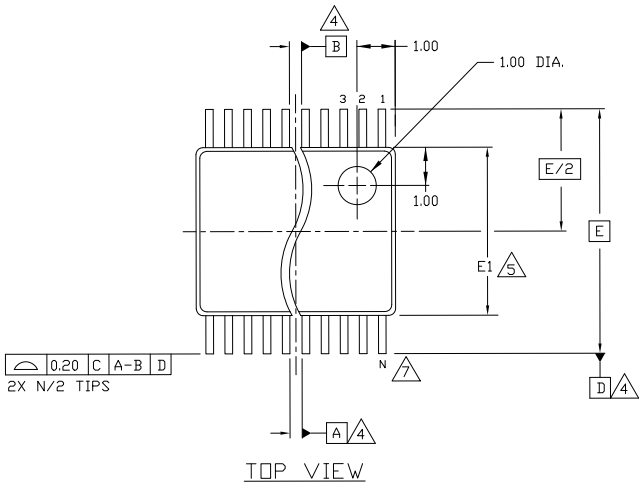
Figure 1. Assembly for Exposed Pad Thermal Release Path - Side View (drawing not to scale)

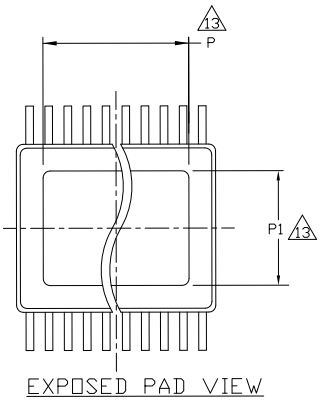
Package Drawing and Dimensions

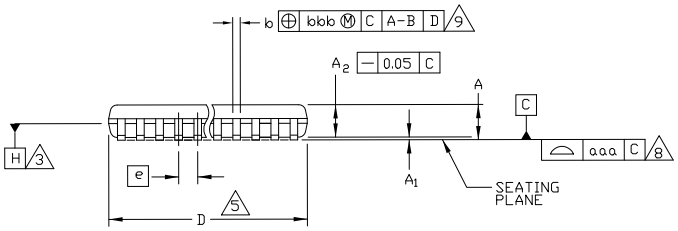
Table 7. Package Dimensions for 20 Lead TSSOP, E-Pad

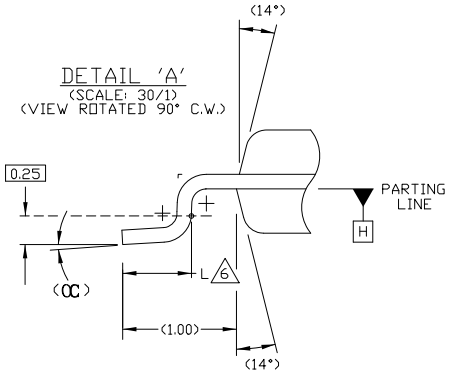
All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		20	
A			1.10
A1	0.5		0.15
A2	0.85	0.90	0.95
aaa		0.076	
b	0.19		0.30
b1	0.19	0.22	0.25
bbb		0.10	
c	0.09		0.20
c1	0.09	0.127	0.16
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
e		0.65 Basic	
E		6.40 Basic	
L	0.50	0.60	0.70
P			4.2
P1			3.0
cc	0°		8°

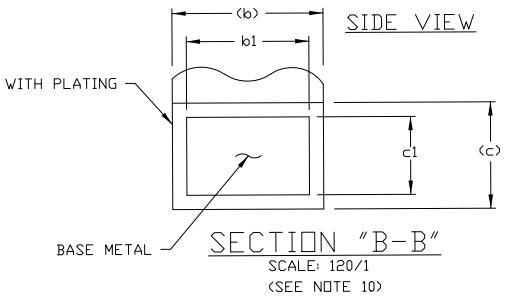
NOTE: Reference Document: IDT PSC-4284

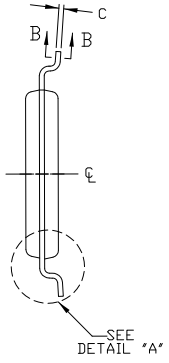


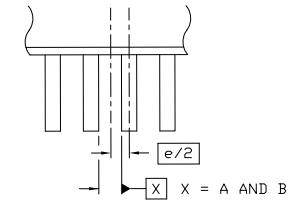


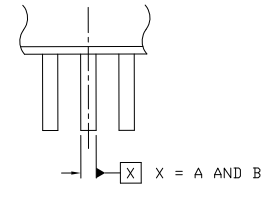












Ordering Information

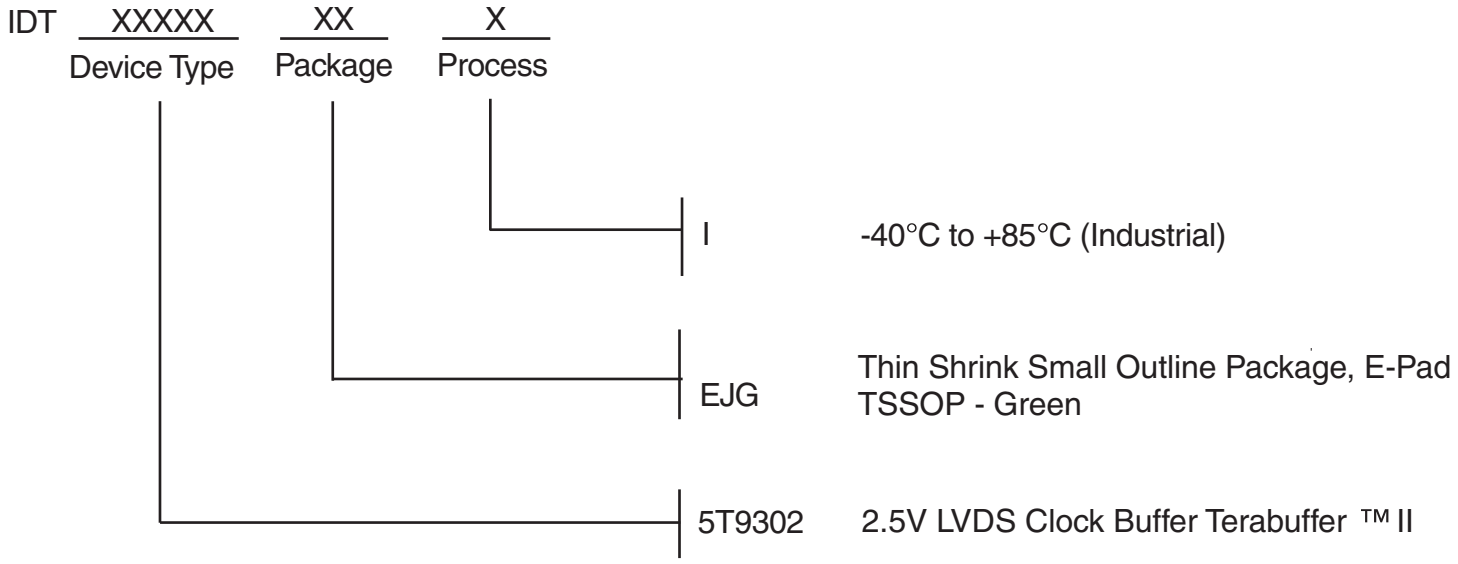


Table 8. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
5T9302EJGI	IDT5T9302EJGI	“Lead-Free” 20 Lead TSSOP, E-Pad	Tube	-40°C to 85°C
5T9302EJGI8	IDT5T9302EJGI	“Lead-Free” 20 Lead TSSOP, E-Pad	Tape & Reel	-40°C to 85°C

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	T8	13	Ordering information - Removed leaded devices	12/16/14
A		1	Product Discontinuation Notice - Last time buy expires September 7, 2016. PDN N-16-02.	3/10/16

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