4-OUTPUT FANOUT BUFFER FOR PCIE GEN1, 2, 3, 4

6V31024

Description

The 6V31024 is a 4-output lower-power differential buffer. Each output has its own OE# pin. It has a maximum operating frequency of 150MHz.

Recommended Application

PCI-Express Gen1, 2, 3 and 4 fanout buffer

Output Features

- 4 - low power differential output pairs
- Individual OE# control of each output pair

Features/Benefits

- Low power differential outputs for PCI-Express
- Power-down mode when all OE# are high
- 4 x 4 mm 20-VFQFPN package

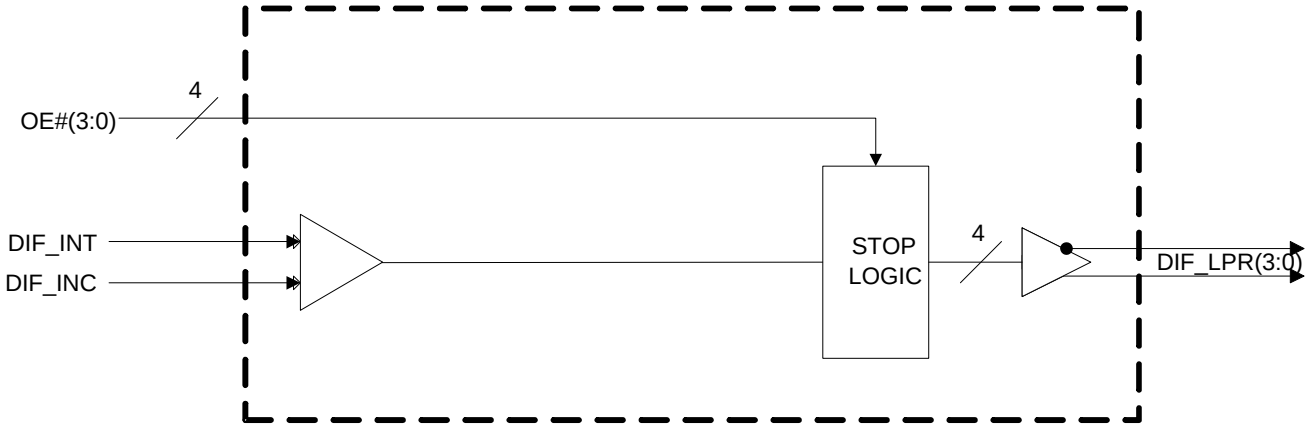
Key Specifications

- Output cycle-cycle jitter < 15ps additive
- Output to Output skew: < 50ps

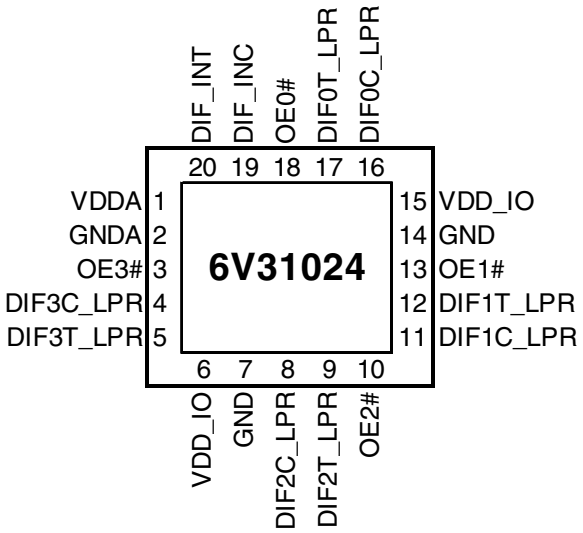
Power Groups

Pin Number		Description
VDD	GND	
6,15	7,14	VDD_IO for DIF(3:0)
1	2	3.3V Analog VDD & GND

Block Diagram

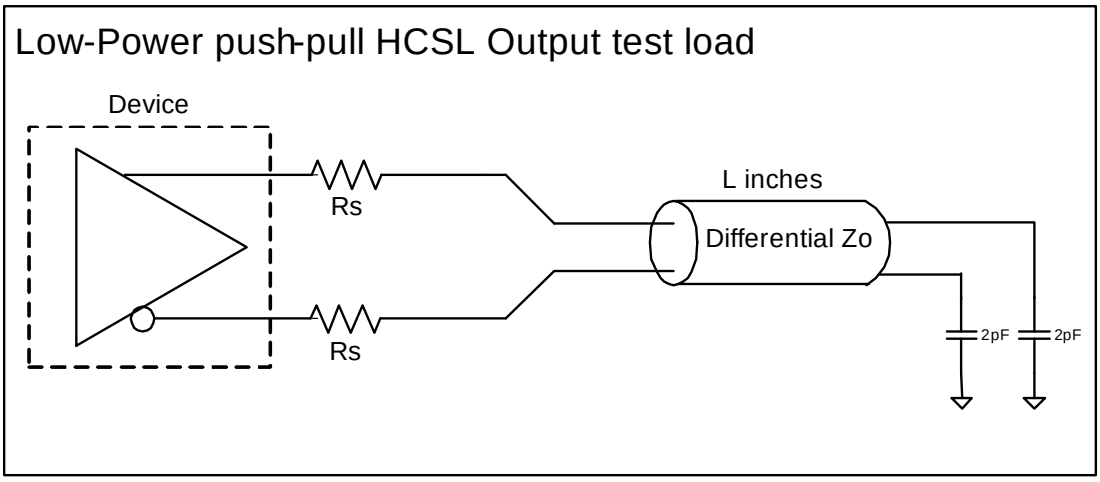


Pin Configuration



20-VFQFPN

Test Loads



Single Ended Impedance (Zo)	Rs 5% tolerance	Rs 2% tolerance	Notes
50	33	33.2	In general, 5% resistors may be used. All values are in ohms.
45	27	27.4	
42.5	24 or 27	24.9	

L = 5 inches

Pin Descriptions

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	VDDA	PWR	3.3V Power for the Analog Core
2	GNDA	GND	Ground for the Analog Core
3	OE3#	IN	Output Enable for DIF3 output. Control is as follows: 0 = enabled, 1 = Low-Low
4	DIF3C_LPR	OUT	Complement clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
5	DIF3T_LPR	OUT	True clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
6	VDD_IO	PWR	Power supply for low power differential outputs, nominal 1.05V to 3.3V
7	GND	GND	Ground pin
8	DIF2C_LPR	OUT	Complement clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
9	DIF2T_LPR	OUT	True clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
10	OE2#	IN	Output Enable for DIF2 output. Control is as follows: 0 = enabled, 1 = Low-Low
11	DIF1C_LPR	OUT	Complement clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
12	DIF1T_LPR	OUT	True clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
13	OE1#	IN	Output Enable for DIF1 output. Control is as follows: 0 = enabled, 1 = Low-Low
14	GND	GND	Ground pin
15	VDD_IO	PWR	Power supply for low power differential outputs, nominal 1.05V to 3.3V
16	DIF0C_LPR	OUT	Complement clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
17	DIF0T_LPR	OUT	True clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
18	OE0#	IN	Output Enable for DIF0 output. Control is as follows: 0 = enabled, 1 = Low-Low
19	DIF_INC	IN	Complement side of differential input clock
20	DIF_INT	IN	True side of differential input clock

Absolute Maximum Ratings

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	Notes
Maximum Supply Voltage	VDDA	Core Supply Voltage		4.6	V	1,7
Maximum Supply Voltage	VDD_IO	Low-Voltage Differential I/O	0.99	3.8	V	1,7
Maximum Input Voltage	V_{IH}	3.3V LVCMOS Inputs		4.6	V	1,7,8
Minimum Input Voltage	V_{IL}	Any Input	Vss - 0.5		V	1,7
Ambient Operating Temp	TambCOM	Commercial Range	0	70	°C	1
Storage Temperature	Ts	-	-65	150	°C	1,7
Input ESD protection	ESD prot	Human Body Model	2000		V	1,7

Electrical Characteristics–Input/Supply/Common Output Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	Notes
Supply Voltage	VDDA	Supply Voltage	3.000	3.600	V	1
Supply Voltage	VDDxxx_IO	Low-Voltage Differential I/O Supply	0.99	3.600	V	1
Input High Voltage	V_{IHSE}	Single-ended inputs	2	V_{DD} + 0.3	V	1
Input Low Voltage	V_{ILSE}	Single-ended inputs	V_{SS} - 0.3	0.8	V	1
Differential Input High Voltage	V_{IHDIF}	Differential inputs (single-ended measurement)	600	1.15	V	1
Differential Input Low Voltage	V_{ILDIF}	Differential inputs (single-ended measurement)	V_{SS} - 0.3	300	V	1
Input Slew Rate - DIF_IN	dv/dt	Measured differentially	0.4	8	V/ns	2
Input Leakage Current	I_{IN}	$V_{IN} = V_{DD}$, V_{IN} = GND	-5	5	uA	1
Operating Supply Current	$I_{DD\_3.3V}$	VDDA supply current		20	mA	1
	$I_{DD\_IO\_133M}$	VDD_IO supply @ fOP = 133MHz		20	mA	1
Power Down Current (All OE# pins High)	$I_{DD\_SB\_3.3V}$	VDDA supply current, Input stopped, OE# pins all high		750	uA	1
	I_{DD_SBIO}	VDD_IO supply, Input stopped, OE# pins all high		150	uA	1
Input Frequency	F_i	V_{DD} = 3.3 V	15	150	MHz	2
Pin Inductance	L_{pin}			7	nH	1
Input Capacitance	C_{IN}	Logic Inputs	1.5	5	pF	1
	C_{OUT}	Output pin capacitance		6	pF	1
OE# latency (at least one OE# is low)	$T_{OE\#LAT}$	Number of clocks to enable or disable output from assertion/deassertion of OE#	1	3	periods	1
Clock stabilization time (from all OE# high to first OE# low).	T_{STAB}	Delay from assertion of first OE# to first clock out (assumes input clock running and device in power down state))		150	ns	1
Tdrive_OE#	$T_{DROE\#}$	Output enable after OE# de-assertion		10	ns	1
Tfall_OE#	T_{FALL}	Fall/rise time of OE# inputs		5	ns	1
Trise_OE#	T_{RISE}			5	ns	1

AC Electrical Characteristics–DIF Low Power Differential Outputs

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	NOTES
Rising Edge Slew Rate	t_{SLR}	Differential Measurement	1.5	4	V/ns	1,2
Falling Edge Slew Rate	t_{FLR}	Differential Measurement	1.5	4	V/ns	1,2
Slew Rate Variation	t_{SLVAR}	Single-ended Measurement		20	%	1
Maximum Output Voltage	V_{HIGH}	Includes overshoot		1150	mV	1
Minimum Output Voltage	V_{LOW}	Includes undershoot	-300		mV	1
Differential Voltage Swing	V_{SWING}	Differential Measurement	1200		mV	1
Crossing Point Voltage	V_{XABS}	Single-ended Measurement	300	550	mV	1,3,4
Crossing Point Variation	$V_{XABSVAR}$	Single-ended Measurement		140	mV	1,3,5
Duty Cycle Distortion	$D_{CYCDIS0}$	Differential Measurement, fIN<=133.33MHz		3	%	1,6
Additive Cycle to Cycle Jitter	$DIFJ_{C2CADD}$	Differential Measurement, **Additive**		15	ps	1
DIF[3:0] Skew	DIF_{SKEW}	Differential Measurement		50	ps	1
Propagation Delay	t_{PD}	Input to output Delay	2.5	3.5	ns	1
Additive Phase Jitter - PCIe Gen1	$t_{phase\_addPCIeG1}$	1.5MHz < 22MHz		6	ps Pk-Pk	1,9
Additive Phase Jitter - PCIe Gen2 High Band	$t_{phase\_addPCIeG2HI}$	High Band is 1.5MHz to Nyquist (50MHz)		0.16	ps rms	1,9
Additive Phase Jitter PCIe Gen2 Low Band	$t_{phase\_addPCIeG2LO}$	Low Band is 10KHz to 1.5MHz		0.07	ps rms	1,9
Additive Phase Jitter PCIe Gen3-4	$t_{phase\_addPCIeG3-4}$	2M-4M, or 2M to 5M		0.1	ps rms	1,9

Notes on Electrical Characteristics (all measurements use 9LRS3187B as clock source and R_S = 33ohms/C_L = 2pF test load):

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Slew rate measured through Vswing centered around differential zero

[3] Vxabs is defined as the voltage where CLK = CLK#

[4] Only applies to the differential rising edge (CLK rising and CLK# falling)

[5] Defined as the total variation of all crossing voltages of CLK rising and CLK# falling. Matching applies to rising edge rate of CLK and falling edge of CLK#. It is measured using a +/-75mV window centered on the average cross point where CLK meets CLK#.

[6] This figure refers to the maximum distortion of the input wave form.

[7] Operation under these conditions is neither implied, nor guaranteed.

[8] Maximum input voltage is not to exceed maximum VDD

[9] The 6V31024 has no PLL, so the part itself contributes very little jitter to the input clock. But this also means that the 6V31024 cannot 'de-jitter' a noisy input clock. Values calculated per PCI SIG and per Intel Clock Jitter tool version 1.6.6for Common Clock Architectures.

Thermal Characteristics

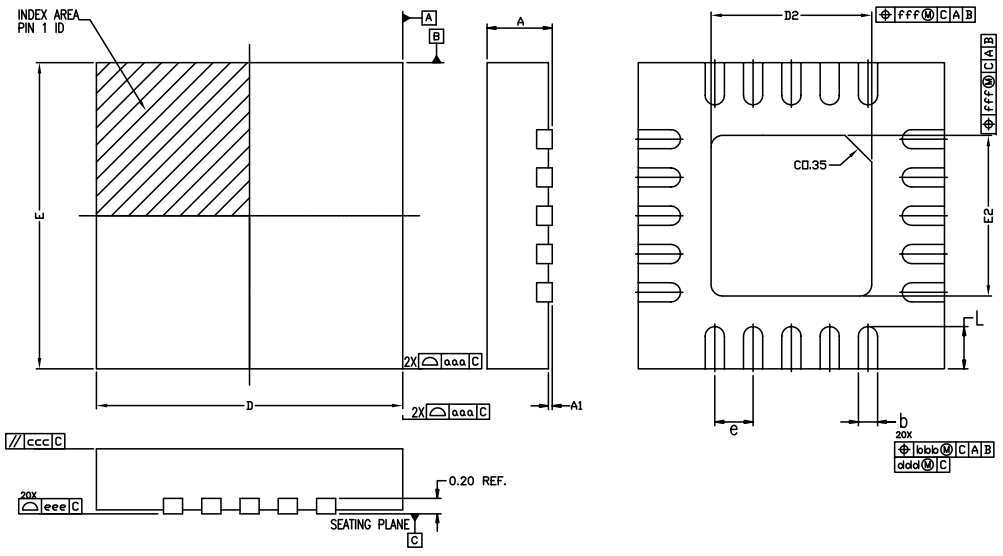
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		39		°C/W
	θ_{JA}	1 m/s air flow		36		°C/W
	θ_{JA}	2.5 m/s air flow		34		°C/W

Marking Diagram

Notes:
1. '$' denotes the mark code.
2. 'G' after the two-letter package code denotes Pb-free, RoHS compliant.
3. 'YYWW' is the date code the part was assembled.
4. Bottom marking: country of origin.

REVISIONS	
REV	DESCRIPTION
00	INITIAL RELEASE

TOP VIEW SIDE VIEW BOTTOM VIEW



SYMBOL	DIMEN	
	MIN	NOM
A	0.80	0.90
A1	0.00	0.02
D	3.90	4.00
E	3.90	4.00
D2	1.95	2.10
E2	1.95	2.10
L	0.45	0.55
e	0.50 B	
N	20	
b	0.20	0.25
aaa	0.15	
bbb	0.10	
ccc	0.10	
ddd	0.05	
eee	0.08	
fff	0.10	

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. ALL DIMENSIONING AND TOLERANCING CONFROM TO ANSI Y14.5M–1982.

TOLERANCES UNLESS SPECIFIED	
DECIMAL	ANGULAR
X±	±1°
XX±	
XXX±	

APPROVALS	DATE
DRAWN RAC	5/13/08
CHECKED	

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TITLE NL/NLG 20 LEADS
4.0 x 4.0 mm B
0.50 mm PITCH

SIZE	DRAWING No.
C	PSC–4

DO NOT SCALE DRAWING

REVISIONS	
REV	DESCRIPTION
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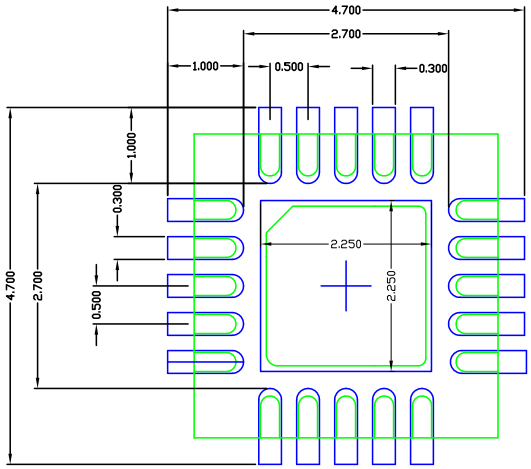

RECOMMENDED LAND PATTERN DIMENSION

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOWS FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

TOLERANCES UNLESS SPECIFIED		IDT™ www.IDT.com
DECIMAL X± XX± XXX±	ANGULAR ±1°	
APPROVALS	DATE	TITLE NL/NLG 20 LEADS 4.0 x 4.0 mm BOD 0.50 mm PITCH VF
DRAWN R&C	5/13/08	
CHECKED		SIZE C / DRAWING No. PSC-4
		DO NOT SCALE DRAWING

Ordering Information

Part / Order Number	Shipping Packaging	Package	Temperature
6V31024NLG	Trays	20-VFQFPN	0 to +70°C
6V31024NLG8	Tape and Reel	20-VFQFPN	0 to +70°C

"G" after the two-letter package code denotes Pb-Free configuration, RoHS compliant.

Revision History

Rev.	Issue Date	Description	Page #
A	5/16/2012	Initial Release.	
B	6/8/2012	Added Thermal char table and marking diagram	6
C	8/15/2017	1. Updated front page text to indicate PCIe Gen1-4, Updated Data sheet Title 2. Renamed "Terminations" to "Test Loads" and updated drawing to latest format. No change to values. 3. Updated "MLF" package references to "VFQFPN" throughout data sheet 4. Updated "DIF Low Power Differential Outputs" Table to include PCIe Gen3 and 4 5. Updated package drawing to latest format. No change to package.	1, 2, 5, 7

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