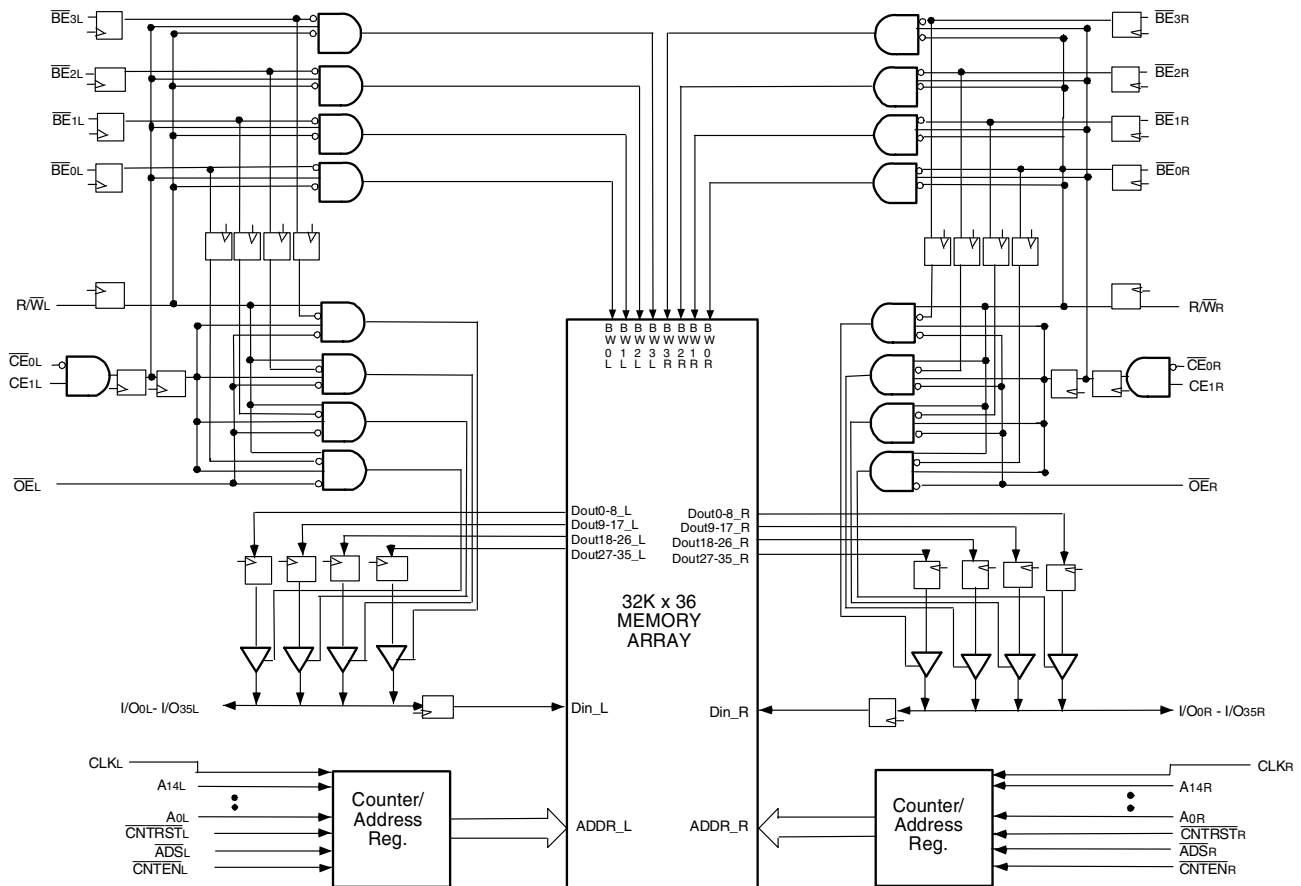


Features:

- ◆ True Dual-Port memory cells which allow simultaneous access of the same memory location
- ◆ High-speed clock to data access
 - Commercial: 4.2/5/6ns (max.)
 - Industrial: 5ns (max)
- ◆ Pipelined output mode
- ◆ Counter enable and reset features
- ◆ Dual chip enables allow for depth expansion without additional logic
- ◆ Full synchronous operation on both ports
 - 7.5ns cycle time, 133MHz operation (9.6 Gbps bandwidth)
 - Fast 4.2ns clock to data out
 - 1.8ns setup to clock and 0.7ns hold on all control, data, and address inputs @ 133MHz
- Data input, address, byte enable and control registers
- Self-timed write allows fast cycle time
- ◆ Separate byte controls for multiplexed bus and bus matching compatibility
- ◆ LVTTTL-compatible, single 3.3V ($\pm 150\text{mV}$) power supply for core
- ◆ LVTTTL compatible, selectable 3.3V ($\pm 150\text{mV}$)/2.5V ($\pm 125\text{mV}$) power supply for I/Os and control signals on each port
- ◆ Industrial temperature range (-40°C to $+85^{\circ}\text{C}$) is available for selected speeds
- ◆ Available in a 208-pin Plastic Quad Flatpack (PQFP) and 208-pin fine pitch Ball Grid Array, and 256-pin Ball Grid Array
- ◆ Green parts available, see ordering information

Functional Block Diagram



4830 tbl 01

Description:

The IDT70V3579 is a high-speed 32K x 36 bit synchronous Dual-Port RAM. The memory array utilizes Dual-Port memory cells to allow simultaneous access of any address from both ports. Registers on control, data, and address inputs provide minimal setup and hold times. The timing latitude provided by this approach allows systems to be designed with very short cycle times. With an input data register, the IDT70V3579 has been optimized for applications having unidirectional or

bidirectional data flow in bursts. An automatic power down feature, controlled by CE0 and CE1, permits the on-chip circuitry of each port to enter a very low standby power mode.

The 70V3579 can support an operating voltage of either 3.3V or 2.5V on one or both ports, controllable by the OPT pins. The power supply for the core of the device (VDD) remains at 3.3V.

Pin Configuration^(1,2,3,4)

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17	
IO19L	IO18L	VSS	NC	NC	NC	A12L	A8L	BE1L	VDD	CLKL	CNTENL	A4L	A0L	OPTL	IO17L	VSS	
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14	B15	B16	B17	
IO20R	VSS	IO18R	VSS	NC	A13L	A9L	BE2L	CE0L	VSS	ADSL	A5L	A1L	VSS	VDDQR	IO16L	IO15R	
C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12	C13	C14	C15	C16	C17	
VDDQL	IO19R	VDDQR	VDD	NC	A14L	A10L	BE3L	CE1L	VSS	R/WL	A6L	A2L	VDD	IO16R	IO15L	VSS	
D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16	D17	
IO22L	VSS	IO21L	IO20L	NC	A11L	A7L	BE0L	VDD	OEL	CNTRSL	A3L	VDD	IO17R	VDDQL	IO14L	IO14R	
E1	E2	E3	E4	<p style="text-align: center;">70V3579 BF208⁽⁵⁾ BFG208⁽⁵⁾ 208-Pin fpBGA Top View⁽⁶⁾</p>										E14	E15	E16	E17
IO23L	IO22R	VDDQR	IO21R											IO12L	IO13R	VSS	IO13L
F1	F2	F3	F4											F14	F15	F16	F17
VDDQL	IO23R	IO24L	VSS											VSS	IO12R	IO11L	VDDQR
G1	G2	G3	G4											G14	G15	G16	G17
IO26L	VSS	IO25L	IO24R											IO9L	VDDQL	IO10L	IO11R
H1	H2	H3	H4											H14	H15	H16	H17
VDD	IO26R	VDDQR	IO25R											VDD	IO9R	VSS	IO10R
J1	J2	J3	J4											J14	J15	J16	J17
VDDQL	VDD	VSS	VSS											VSS	VDD	VSS	VDDQR
K1	K2	K3	K4	K14	K15	K16	K17										
IO28R	VSS	IO27R	VSS	IO7R	VDDQL	IO8R	VSS										
L1	L2	L3	L4	L14	L15	L16	L17										
IO29R	IO28L	VDDQR	IO27L	IO6R	IO7L	VSS	IO8L										
M1	M2	M3	M4	M14	M15	M16	M17										
VDDQL	IO29L	IO30R	VSS	VSS	IO6L	IO5R	VDDQR										
N1	N2	N3	N4	N14	N15	N16	N17										
IO31L	VSS	IO31R	IO30L	IO3R	VDDQL	IO4R	IO5L										
P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	P13	P14	P15	P16	P17	
IO32R	IO32L	VDDQR	IO35R	NC	NC	A12R	A8R	BE1R	VDD	CLKR	CNTENR	A4R	IO2L	IO3L	VSS	IO4L	
R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	R15	R16	R17	
VSS	IO33L	IO34R	NC	NC	A13R	A9R	BE2R	CE0R	VSS	ADSR	A5R	A1R	VSS	VDDQL	IO1R	VDDQR	
T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16	T17	
IO33R	IO34L	VDDQL	VSS	NC	A14R	A10R	BE3R	CE1R	VSS	R/WR	A6R	A2R	VSS	IO0R	VSS	IO2R	
U1	U2	U3	U4	U5	U6	U7	U8	U9	U10	U11	U12	U13	U14	U15	U16	U17	
VSS	IO35L	VDD	NC	NC	A11R	A7R	BE0R	VDD	OER	CNTRSTR	A3R	A0R	VDD	OPTR	IO0L	IO1L	

4830 drw 02c

NOTES:

1. All VDD pins must be connected to 3.3V power supply.
2. All VDDQ pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to VIH (3.3V), and 2.5V if OPT pin for that port is set to VIL (0V).
3. All VSS pins must be connected to ground supply.
4. Package body is approximately 15mm x 15mm x 1.4mm, with 0.8mm ball-pitch.
5. This package code is used to reference the package diagram.
6. This text does not indicate orientation of the actual part-marking.

Pin Configuration^(1,2,3,4) (con't.)

70V3579
BC256⁽⁵⁾
BCG256⁽⁵⁾

256-Pin BGA
Top View⁽⁶⁾

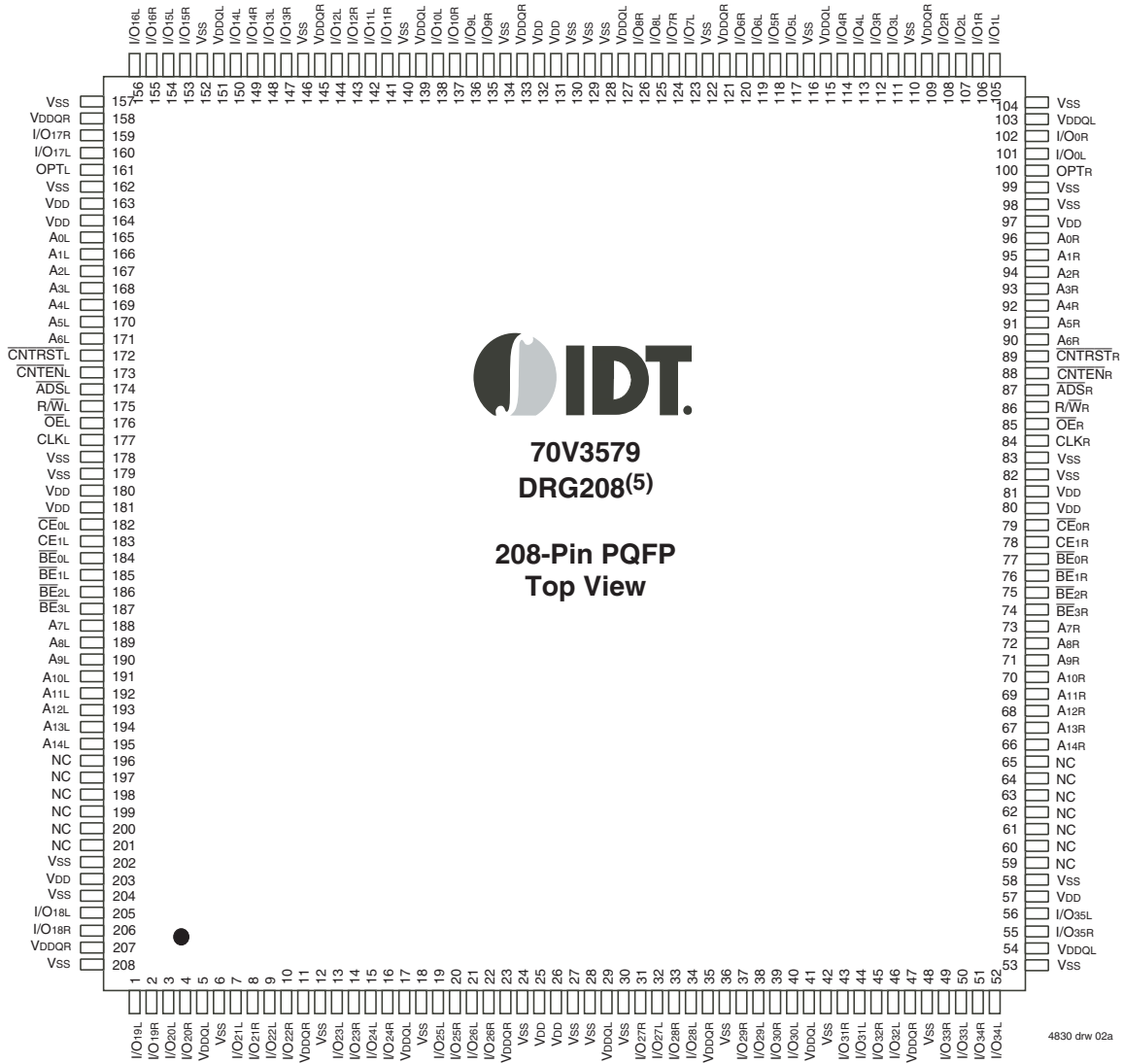
A1 NC	A2 NC	A3 NC	A4 NC	A5 A14L	A6 A11L	A7 A8L	A8 BE ₂ L	A9 CE ₁ L	A10 OE _L	A11 CNTEN _L	A12 A5L	A13 A2L	A14 A0L	A15 NC	A16 NC
B1 I/O ₁₈ L	B2 NC	B3 NC	B4 NC	B5 NC	B6 A12L	B7 A9L	B8 BE ₃ L	B9 CE ₀ L	B10 R/W _L	B11 CNTRST _L	B12 A4L	B13 A1L	B14 VDD	B15 I/O ₁₇ L	B16 NC
C1 I/O ₁₈ R	C2 I/O ₁₉ L	C3 VSS	C4 NC	C5 A13L	C6 A10L	C7 A7L	C8 BE ₁ L	C9 BE ₀ L	C10 CLK _L	C11 ADSL	C12 A6L	C13 A3L	C14 OPT _L	C15 I/O ₁₇ R	C16 I/O ₁₆ L
D1 I/O ₂₀ R	D2 I/O ₁₉ R	D3 I/O ₂₀ L	D4 VDD	D5 VDDQL	D6 VDDQL	D7 VDDQR	D8 VDDQR	D9 VDDQL	D10 VDDQL	D11 VDDQR	D12 VDDQR	D13 VDD	D14 I/O ₁₅ R	D15 I/O ₁₅ L	D16 I/O ₁₆ R
E1 I/O ₂₁ R	E2 I/O ₂₁ L	E3 I/O ₂₂ L	E4 VDDQL	E5 VDD	E6 VDD	E7 VSS	E8 VSS	E9 VSS	E10 VSS	E11 VDD	E12 VDD	E13 VDDQR	E14 I/O ₁₃ L	E15 I/O ₁₄ L	E16 I/O ₁₄ R
F1 I/O ₂₃ L	F2 I/O ₂₂ R	F3 I/O ₂₃ R	F4 VDDQL	F5 VDD	F6 VSS	F7 VSS	F8 VSS	F9 VSS	F10 VSS	F11 VSS	F12 VDD	F13 VDDQR	F14 I/O ₁₂ R	F15 I/O ₁₃ R	F16 I/O ₁₂ L
G1 I/O ₂₄ R	G2 I/O ₂₄ L	G3 I/O ₂₅ L	G4 VDDQR	G5 VSS	G6 VSS	G7 VSS	G8 VSS	G9 VSS	G10 VSS	G11 VSS	G12 VSS	G13 VDDQL	G14 I/O ₁₀ L	G15 I/O ₁₁ L	G16 I/O ₁₁ R
H1 I/O ₂₆ L	H2 I/O ₂₅ R	H3 I/O ₂₆ R	H4 VDDQR	H5 VSS	H6 VSS	H7 VSS	H8 VSS	H9 VSS	H10 VSS	H11 VSS	H12 VSS	H13 VDDQL	H14 I/O ₉ R	H15 I/O ₉ L	H16 I/O ₁₀ R
J1 I/O ₂₇ L	J2 I/O ₂₈ R	J3 I/O ₂₇ R	J4 VDDQL	J5 VSS	J6 VSS	J7 VSS	J8 VSS	J9 VSS	J10 VSS	J11 VSS	J12 VSS	J13 VDDQR	J14 I/O ₈ R	J15 I/O ₇ R	J16 I/O ₈ L
K1 I/O ₂₉ R	K2 I/O ₂₉ L	K3 I/O ₂₈ L	K4 VDDQL	K5 VSS	K6 VSS	K7 VSS	K8 VSS	K9 VSS	K10 VSS	K11 VSS	K12 VSS	K13 VDDQR	K14 I/O ₆ R	K15 I/O ₆ L	K16 I/O ₇ L
L1 I/O ₃₀ L	L2 I/O ₃₁ R	L3 I/O ₃₀ R	L4 VDDQR	L5 VDD	L6 VSS	L7 VSS	L8 VSS	L9 VSS	L10 VSS	L11 VSS	L12 VDD	L13 VDDQL	L14 I/O ₅ L	L15 I/O ₄ R	L16 I/O ₅ R
M1 I/O ₃₂ R	M2 I/O ₃₂ L	M3 I/O ₃₁ L	M4 VDDQR	M5 VDD	M6 VDD	M7 VSS	M8 VSS	M9 VSS	M10 VSS	M11 VDD	M12 VDD	M13 VDDQL	M14 I/O ₃ R	M15 I/O ₃ L	M16 I/O ₄ L
N1 I/O ₃₃ L	N2 I/O ₃₄ R	N3 I/O ₃₃ R	N4 VDD	N5 VDDQR	N6 VDDQR	N7 VDDQL	N8 VDDQL	N9 VDDQR	N10 VDDQR	N11 VDDQL	N12 VDDQL	N13 VDD	N14 I/O ₂ L	N15 I/O ₁ R	N16 I/O ₂ R
P1 I/O ₃₅ R	P2 I/O ₃₄ L	P3 NC	P4 NC	P5 A13R	P6 A10R	P7 A7R	P8 BE ₁ R	P9 BE ₀ R	P10 CLK _R	P11 ADSR	P12 A6R	P13 A3R	P14 I/O ₀ L	P15 I/O ₀ R	P16 I/O ₁ L
R1 I/O ₃₅ L	R2 NC	R3 NC	R4 NC	R5 NC	R6 A12R	R7 A9R	R8 BE ₃ R	R9 CE ₀ R	R10 R/W _R	R11 CNTRST _R	R12 A4R	R13 A1R	R14 OPT _R	R15 NC	R16 NC
T1 NC	T2 NC	T3 NC	T4 NC	T5 A14R	T6 A11R	T7 A8R	T8 BE ₂ R	T9 CE ₁ R	T10 OE _R	T11 CNTEN _R	T12 A5R	T13 A2R	T14 A0R	T15 NC	T16 NC

4830 drw 02d

NOTES:

1. All VDD pins must be connected to 3.3V power supply.
2. All VDDQ pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to VIH (3.3V), and 2.5V if OPT pin for that port is set to VIL (0V).
3. All VSS pins must be connected to ground supply.
4. Package body is approximately 17mm x 17mm x 1.4mm, with 1.0mm ball-pitch.
5. This package code is used to reference the package diagram.
6. This text does not indicate orientation of the actual part-marking.

Pin Configuration^(1,2,3,4) (con't.)



NOTES:

1. All VDD pins must be connected to 3.3V power supply.
2. All VDDQ pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to VIH (3.3V), and 2.5V if OPT pin for that port is set to VIL (0V).
3. All VSS pins must be connected to ground supply.
4. Package body is approximately 28mm x 28mm x 3.5mm.
5. This package code is used to reference the package diagram.

Pin Names

Left Port	Right Port	Names
\overline{CE}_{0L} , CE_{1L}	\overline{CE}_{0R} , CE_{1R}	Chip Enables
R/\overline{WL}	R/\overline{WR}	Read/Write Enable
\overline{OE}_L	\overline{OE}_R	Output Enable
A0L - A14L	A0R - A14R	Address
I/O0L - I/O35L	I/O0R - I/O35R	Data Input/Output
CLKL	CLKR	Clock
\overline{ADS}_L	\overline{ADS}_R	Address Strobe Enable
\overline{CNTEN}_L	\overline{CNTEN}_R	Counter Enable
\overline{CNTRST}_L	\overline{CNTRST}_R	Counter Reset
\overline{BE}_{0L} - \overline{BE}_{3L}	\overline{BE}_{0R} - \overline{BE}_{3R}	Byte Enables (9-bit bytes)
VDD0L	VDD0R	Power (I/O Bus) (3.3V or 2.5V) ⁽¹⁾
OPTL	OPTR	Option for selecting VDD0X ^(1,2)
VDD		Power (3.3V) ⁽¹⁾
VSS		Ground (0V)

4830 tbl 01

NOTES:

- VDD, OPTx, and VDD0x must be set to appropriate operating levels prior to applying inputs on the I/Os and controls for that port.
- OPTx selects the operating voltage levels on that port. If OPTx is set to VIH (3.3V), then that port's I/Os and controls will operate at 3.3V levels and VDD0x must be supplied at 3.3V. If OPTx is set to VIL (0V), then that port's I/Os and controls will operate at 2.5V levels and VDD0x must be supplied at 2.5V. The OPT pins are independent of one another—both ports can operate at 3.3V levels, both can operate at 2.5V levels, or either can operate at 3.3V with the other at 2.5V.

Truth Table I—Read/Write and Enable Control^(1,2,3,4)

\overline{OE}	CLK	\overline{CE}_0	CE_1	\overline{BE}_3	\overline{BE}_2	\overline{BE}_1	\overline{BE}_0	R \overline{W}	Byte 3 I/O27-35	Byte 2 I/O18-26	Byte 1 I/O9-17	Byte 0 I/O0-8	MODE
X	↑	H	X	X	X	X	X	X	High-Z	High-Z	High-Z	High-Z	Deselected-Power Down
X	↑	X	L	X	X	X	X	X	High-Z	High-Z	High-Z	High-Z	Deselected-Power Down
X	↑	L	H	H	H	H	H	X	High-Z	High-Z	High-Z	High-Z	All Bytes Deselected
X	↑	L	H	H	H	H	L	L	High-Z	High-Z	High-Z	DIN	Write to Byte 0 Only
X	↑	L	H	H	H	L	H	L	High-Z	High-Z	DIN	High-Z	Write to Byte 1 Only
X	↑	L	H	H	L	H	H	L	High-Z	DIN	High-Z	High-Z	Write to Byte 2 Only
X	↑	L	H	L	H	H	H	L	DIN	High-Z	High-Z	High-Z	Write to Byte 3 Only
X	↑	L	H	H	H	L	L	L	High-Z	High-Z	DIN	DIN	Write to Lower 2 Bytes Only
X	↑	L	H	L	L	H	H	L	DIN	DIN	High-Z	High-Z	Write to Upper 2 bytes Only
X	↑	L	H	L	L	L	L	L	DIN	DIN	DIN	DIN	Write to All Bytes
L	↑	L	H	H	H	H	L	H	High-Z	High-Z	High-Z	DOUT	Read Byte 0 Only
L	↑	L	H	H	H	L	H	H	High-Z	High-Z	DOUT	High-Z	Read Byte 1 Only
L	↑	L	H	H	L	H	H	H	High-Z	DOUT	High-Z	High-Z	Read Byte 2 Only
L	↑	L	H	L	H	H	H	H	DOUT	High-Z	High-Z	High-Z	Read Byte 3 Only
L	↑	L	H	H	H	L	L	H	High-Z	High-Z	DOUT	DOUT	Read Lower 2 Bytes Only
L	↑	L	H	L	L	H	H	H	DOUT	DOUT	High-Z	High-Z	Read Upper 2 Bytes Only
L	↑	L	H	L	L	L	L	H	DOUT	DOUT	DOUT	DOUT	Read All Bytes
H	↑	L	H	L	L	L	L	X	High-Z	High-Z	High-Z	High-Z	Outputs Disabled

NOTES:

- "H" = VIH, "L" = VIL, "X" = Don't Care.
- \overline{ADS} , \overline{CNTEN} , \overline{CNTRST} = X.
- \overline{OE} is an asynchronous input signal.
- It is possible to read or write any combination of bytes during a given access. A few representative samples have been illustrated here.

4830 tbl 02

Truth Table II—Address Counter Control^(1,2)

Address	Previous Address	Addr Used	CLK ⁽⁶⁾	\overline{ADS}	\overline{CNTEN}	\overline{CNRST}	I/O ⁽⁹⁾	MODE
X	X	0	↑	X	X	L ⁽⁴⁾	D _{IO} (0)	Counter Reset to Address 0
An	X	An	↑	L ⁽⁴⁾	X	H	D _{IO} (n)	External Address Used
An	Ap	Ap	↑	H	H	H	D _{IO} (p)	External Address Blocked—Counter disabled (Ap reused)
X	Ap	Ap + 1	↑	H	L ⁽⁵⁾	H	D _{IO} (p+1)	Counter Enabled—Internal Address generation

NOTES:

- "H" = V_{IH}, "L" = V_{IL}, "X" = Don't Care.
- Read and write operations are controlled by the appropriate setting of R \overline{W} , $\overline{CE0}$, CE₁, \overline{BEn} and \overline{OE} .
- Outputs are in Pipelined mode: the data out will be delayed by one cycle.
- \overline{ADS} and \overline{CNRST} are independent of all other memory control signals including $\overline{CE0}$, CE₁ and \overline{BEn}
- The address counter advances if \overline{CNTEN} = V_{IL} on the rising edge of CLK, regardless of all other memory control signals including $\overline{CE0}$, CE₁, \overline{BEn} .

4830 tbl 03

Recommended Operating Temperature and Supply Voltage⁽¹⁾

Grade	Ambient Temperature	GND	V _{DD}
Commercial	0°C to +70°C	0V	3.3V ± 150mV
Industrial	-40°C to +85°C	0V	3.3V ± 150mV

NOTE:

- Industrial temperature: for specific speeds, packages and powers contact your sales office.

4830 tbl 04

Recommended DC Operating Conditions with V_{DDQ} at 2.5V

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{DD}	Core Supply Voltage	3.15	3.3	3.45	V
V _{DDQ}	I/O Supply Voltage ⁽³⁾	2.375	2.5	2.625	V
V _{SS}	Ground	0	0	0	V
V _{IH}	Input High Voltage ⁽³⁾ (Address & Control Inputs)	1.7	—	V _{DDQ} + 125mV ⁽²⁾	V
V _{IH}	Input High Voltage - I/O ⁽³⁾	1.7	—	V _{DDQ} + 125mV ⁽²⁾	V
V _{IL}	Input Low Voltage	-0.3 ⁽¹⁾	—	0.7	V

NOTES:

- V_{IL} ≥ -1.5V for pulse width less than 10 ns.
- V_{TERM} must not exceed V_{DDQ} + 125mV.
- To select operation at 2.5V levels on the I/Os and controls of a given port, the OPT pin for that port must be set to V_{IL} (0V), and V_{DDQX} for that port must be supplied as indicated above.

4830 tbl 05a

Absolute Maximum Ratings⁽¹⁾

Symbol	Rating	Commercial & Industrial	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
T _{BIAS}	Temperature Under Bias	-55 to +125	°C
T _{STG}	Storage Temperature	-65 to +150	°C
I _{OUT}	DC Output Current	50	mA

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{TERM} must not exceed V_{DD} + 150mV for more than 25% of the cycle time or 4ns maximum, and is limited to ≤ 20mA for the period of V_{TERM} ≥ V_{DD} + 150mV.

4830 tbl 06

Recommended DC Operating Conditions with V_{DDQ} at 3.3V

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{DD}	Core Supply Voltage	3.15	3.3	3.45	V
V _{DDQ}	I/O Supply Voltage ⁽³⁾	3.15	3.3	3.45	V
V _{SS}	Ground	0	0	0	V
V _{IH}	Input High Voltage (Address & Control Inputs) ⁽³⁾	2.0	—	V _{DDQ} + 150mV ⁽²⁾	V
V _{IH}	Input High Voltage - I/O ⁽³⁾	2.0	—	V _{DDQ} + 150mV ⁽²⁾	V
V _{IL}	Input Low Voltage	-0.3 ⁽¹⁾	—	0.8	V

NOTES:

- V_{IL} ≥ -1.5V for pulse width less than 10 ns.
- V_{TERM} must not exceed V_{DDQ} + 150mV.
- To select operation at 3.3V levels on the I/Os and controls of a given port, the OPT pin for that port must be set to V_{IH} (3.3V), and V_{DDQX} for that port must be supplied as indicated above.

4830 tbl 05b

Capacitance⁽¹⁾

($T_A = +25^\circ\text{C}$, $F = 1.0\text{MHz}$) PQFP ONLY

Symbol	Parameter	Conditions ⁽²⁾	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 3\text{dV}$	8	pF
$C_{OUT}^{(3)}$	Output Capacitance	$V_{OUT} = 3\text{dV}$	10.5	pF

4830 tbl 07

NOTES:

- These parameters are determined by device characterization, but are not production tested.
- 3dV references the interpolated capacitance when the input and output switch from 0V to 3V or from 3V to 0V.
- C_{OUT} also references C_{IO} .

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range ($V_{DD} = 3.3\text{V} \pm 150\text{mV}$)

Symbol	Parameter	Test Conditions	70V3579S		Unit
			Min.	Max.	
$ I_{LI} $	Input Leakage Current ⁽¹⁾	$V_{DDQ} = \text{Max.}, V_{IN} = 0\text{V to } V_{DDQ}$	—	10	μA
$ I_{LO} $	Output Leakage Current	$\overline{CE_0} = V_{IH}$ or $CE_1 = V_{IL}, V_{OUT} = 0\text{V to } V_{DDQ}$	—	10	μA
$V_{OL} (3.3\text{V})$	Output Low Voltage ⁽²⁾	$I_{OL} = +4\text{mA}, V_{DDQ} = \text{Min.}$	—	0.4	V
$V_{OH} (3.3\text{V})$	Output High Voltage ⁽²⁾	$I_{OH} = -4\text{mA}, V_{DDQ} = \text{Min.}$	2.4	—	V
$V_{OL} (2.5\text{V})$	Output Low Voltage ⁽²⁾	$I_{OL} = +2\text{mA}, V_{DDQ} = \text{Min.}$	—	0.4	V
$V_{OH} (2.5\text{V})$	Output High Voltage ⁽²⁾	$I_{OH} = -2\text{mA}, V_{DDQ} = \text{Min.}$	2.0	—	V

4830 tbl 08

NOTES:

- At $V_{DD} \leq -2.0\text{V}$ input leakages are undefined.
- V_{DDQ} is selectable (3.3V/2.5V) via OPT pins. Refer to p.4 for details.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range⁽³⁾ ($V_{DD} = 3.3V \pm 150mV$)

Symbol	Parameter	Test Condition	Version	70V3579S4 Com'l Only		70V3579S5 Com'l & Ind		70V3579S6 Com'l Only		Unit
				Typ. ⁽⁴⁾	Max.	Typ. ⁽⁴⁾	Max.	Typ. ⁽⁴⁾	Max.	
IDD	Dynamic Operating Current (Both Ports Active)	\overline{CE}_L and $\overline{CE}_R = V_{IL}$, Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L S	375	460	285	360	245	310	mA
			IND S	—	—	285	415	245	360	
ISB1	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L = \overline{CE}_R = V_{IH}$ $f = f_{MAX}^{(1)}$	COM'L S	145	190	105	145	95	125	mA
			IND S	—	—	105	175	95	150	
ISB2	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}^*A^* = V_{IL}$ and $\overline{CE}^*B^* = V_{IH}^{(5)}$ Active Port Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L S	265	325	190	260	175	225	mA
			IND S	—	—	190	300	175	260	
ISB3	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports \overline{CE}_L and $\overline{CE}_R \geq V_{DDQ} - 0.2V$, $V_{IN} \geq V_{DDQ} - 0.2V$ or $V_{IN} \leq 0.2V$, $f = 0^{(2)}$	COM'L S	6	15	6	15	6	15	mA
			IND S	—	—	6	30	6	30	
ISB4	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}^*A^* \leq 0.2V$ and $\overline{CE}^*B^* \geq V_{DDQ} - 0.2V^{(5)}$ $V_{IN} \geq V_{DDQ} - 0.2V$ or $V_{IN} \leq 0.2V$, Active Port, Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L S	265	325	180	260	170	225	mA
			IND S	—	—	180	300	170	260	

4830 tbl 09

NOTES:

- At $f = f_{MAX}$, address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of 1/tcyc, using "AC TEST CONDITIONS" at input levels of GND to 3V.
- $f = 0$ means no address, clock, or control lines change. Applies only to input at CMOS level standby.
- Port "A" may be either left or right port. Port "B" is the opposite from port "A".
- $V_{DD} = 3.3V$, $T_A = 25^\circ C$ for Typ, and are not production tested. $I_{DD} dc(f=0) = 120mA$ (Typ).
- $\overline{CE}_X = V_{IL}$ means $\overline{CE}_{0X} = V_{IL}$ and $CE_{1X} = V_{IH}$
 $\overline{CE}_X = V_{IH}$ means $\overline{CE}_{0X} = V_{IH}$ or $CE_{1X} = V_{IL}$
 $\overline{CE}_X \leq 0.2V$ means $\overline{CE}_{0X} \leq 0.2V$ and $CE_{1X} \geq V_{DDQ} - 0.2V$
 $\overline{CE}_X \geq V_{DDQ} - 0.2V$ means $\overline{CE}_{0X} \geq V_{DDQ} - 0.2V$ or $CE_{1X} \leq 0.2V$
 "X" represents "L" for left port or "R" for right port.

AC Test Conditions (V_{DDQ} - 3.3V/2.5V)

Input Pulse Levels (Address & Controls)	GND to 3.0V/GND to 2.35V
Input Pulse Levels (I/Os)	GND to 3.0V/GND to 2.35V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V/1.25V
Output Reference Levels	1.5V/1.25V
Output Load	Figures 1, 2, and 3

4830 tbl 10

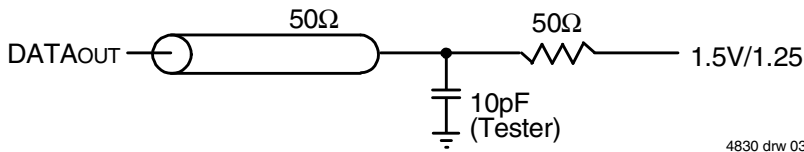


Figure 1. AC Output Test load.

4830 drw 03

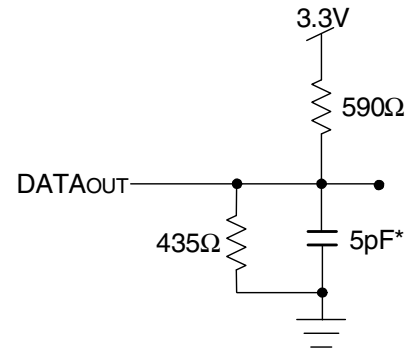
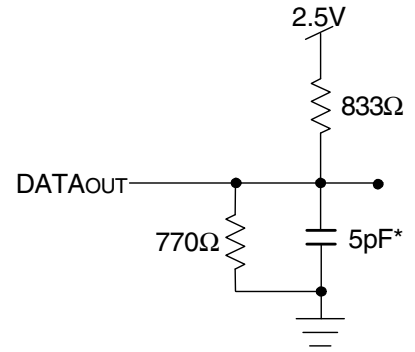
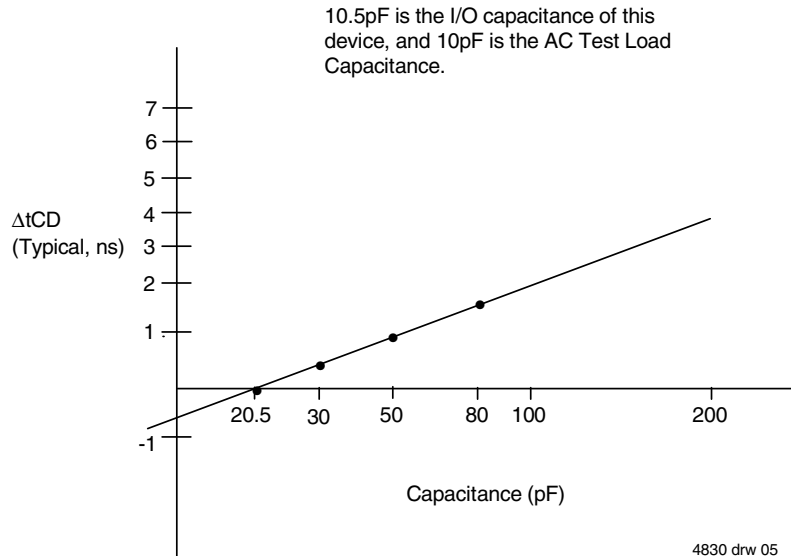


Figure 2. Output Test Load
(For t_{ckLZ}, t_{ckHZ}, t_{oLZ}, and t_{oHZ}).
*Including scope and jig.

4830 drw 04



4830 drw 05

Figure 3. Typical Output Derating (Lumped Capacitive Load).

AC Electrical Characteristics Over the Operating Temperature Range (Read and Write Cycle Timing)^(1,2)
(VDD = 3.3V ± 150mV, TA = 0°C to +70°C)

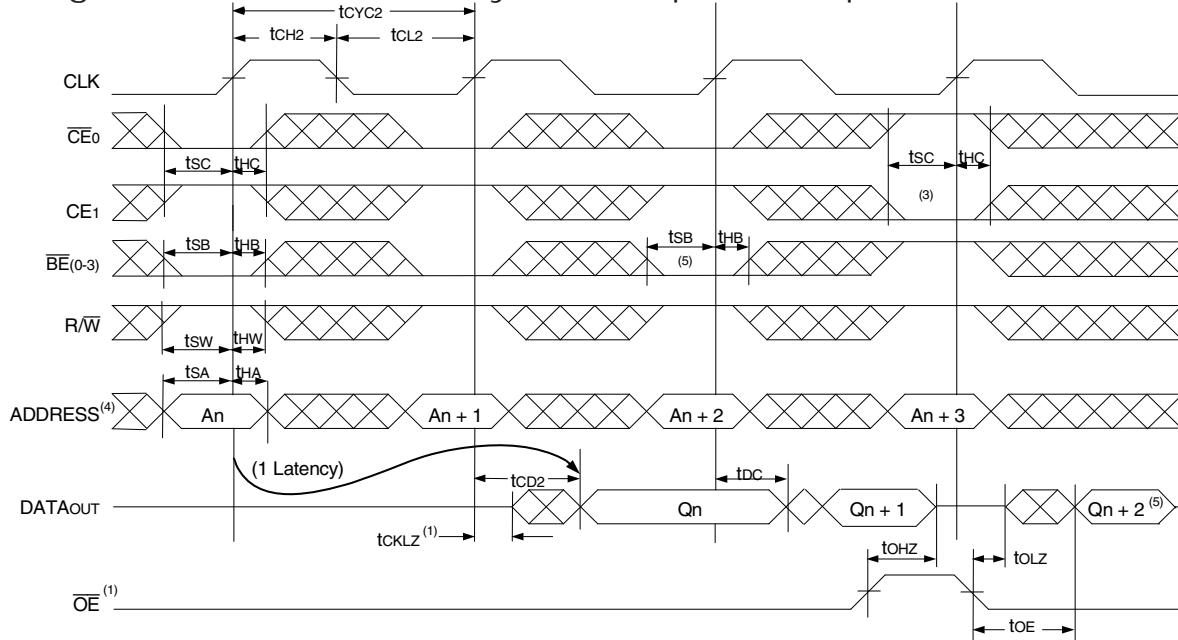
Symbol	Parameter	70V3579S4 Com'l Only		70V3579S5 Com'l & Ind		70V3579S6 Com'l Only		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
tCYC2	Clock Cycle Time (Pipelined)	7.5	—	10	—	12	—	ns
tCH2	Clock High Time (Pipelined)	3	—	4	—	5	—	ns
tCL2	Clock Low Time (Pipelined)	3	—	4	—	5	—	ns
tR	Clock Rise Time	—	3	—	3	—	3	ns
tF	Clock Fall Time	—	3	—	3	—	3	ns
tSA	Address Setup Time	1.8	—	2.0	—	2.0	—	ns
tHA	Address Hold Time	0.7	—	0.7	—	1.0	—	ns
tSC	Chip Enable Setup Time	1.8	—	2.0	—	2.0	—	ns
tHC	Chip Enable Hold Time	0.7	—	0.7	—	1.0	—	ns
tSB	Byte Enable Setup Time	1.8	—	2.0	—	2.0	—	ns
tHB	Byte Enable Hold Time	0.7	—	0.7	—	1.0	—	ns
tSW	R/W Setup Time	1.8	—	2.0	—	2.0	—	ns
tHW	R/W Hold Time	0.7	—	0.7	—	1.0	—	ns
tSD	Input Data Setup Time	1.8	—	2.0	—	2.0	—	ns
tHD	Input Data Hold Time	0.7	—	0.7	—	1.0	—	ns
tSAD	\overline{ADS} Setup Time	1.8	—	2.0	—	2.0	—	ns
tHAD	\overline{ADS} Hold Time	0.7	—	0.7	—	1.0	—	ns
tSCN	\overline{CNTEN} Setup Time	1.8	—	2.0	—	2.0	—	ns
tHCN	\overline{CNTEN} Hold Time	0.7	—	0.7	—	1.0	—	ns
tSRST	\overline{CNTRST} Setup Time	1.8	—	2.0	—	2.0	—	ns
tHRST	\overline{CNTRST} Hold Time	0.7	—	0.7	—	1.0	—	ns
tOE ⁽¹⁾	Output Enable to Data Valid	—	4	—	5	—	6	ns
tOLZ	Output Enable to Output Low-Z	0	—	0	—	0	—	ns
tOHZ	Output Enable to Output High-Z	1	4	1	4.5	1	5	ns
tCD2	Clock to Data Valid (Pipelined)	—	4.2	—	5	—	6	ns
tDC	Data Output Hold After Clock High	1	—	1	—	1	—	ns
tCKHZ	Clock High to Output High-Z	1	3	1	4.5	1.5	6	ns
tCKLZ	Clock High to Output Low-Z	1	—	1	—	1	—	ns
Port-to-Port Delay								
tCO	Clock-to-Clock Offset	6	—	8	—	10	—	ns

NOTES:

1. All input signals are synchronous with respect to the clock except for the asynchronous Output Enable (\overline{OE}).
2. These values are valid for either level of VDD0 (3.3V/2.5V). See page 4 for details on selecting the desired I/O voltage levels for each port.

4830 tbl 11

Timing Waveform of Read Cycle for Pipelined Operation⁽²⁾

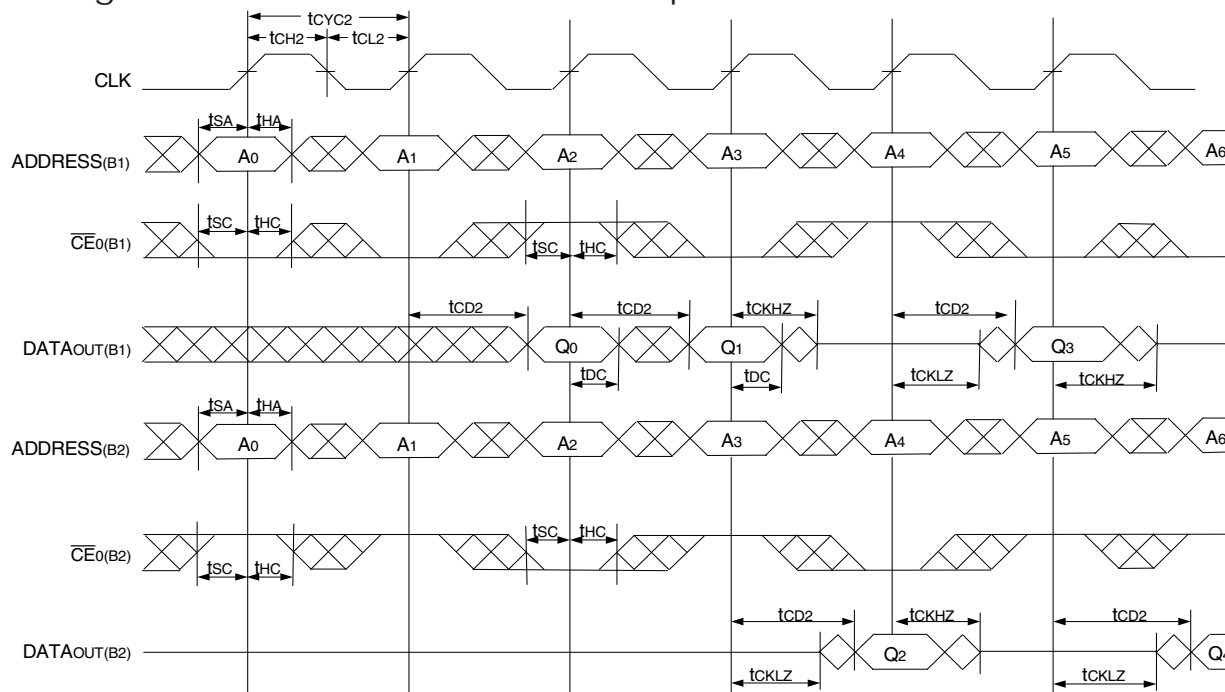


NOTES:

1. \overline{OE} is asynchronously controlled; all other inputs are synchronous to the rising clock edge.
2. $\overline{ADS} = V_{IL}$, \overline{CNTEN} and $\overline{CNTRST} = V_{IH}$.
3. The output is disabled (High-Impedance state) by $\overline{CE}_0 = V_{IH}$, $CE_1 = V_{IL}$, $\overline{BE}_n = V_{IH}$ following the next rising edge of the clock. Refer to Truth Table 1.
4. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. If \overline{BE}_n was HIGH, then the appropriate Byte of DATAout for $Q_n + 2$ would be disabled (High-Impedance state).

4830 drw 06

Timing Waveform of a Multi-Device Pipelined Read^(1,2)

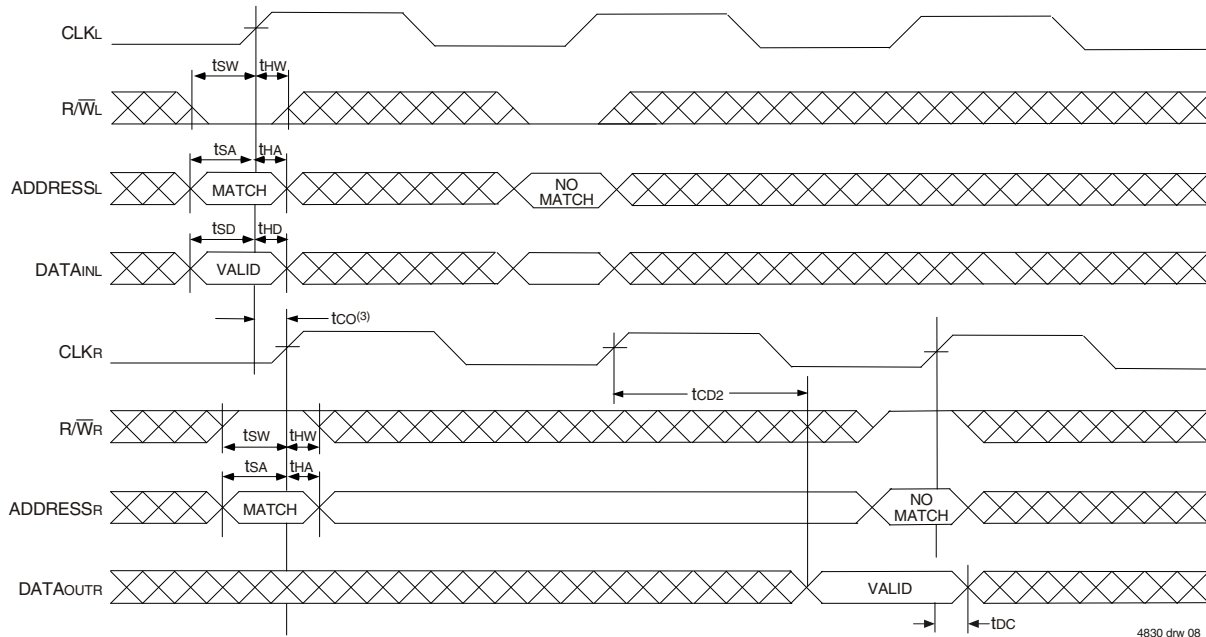


NOTES:

1. B1 Represents Device #1; B2 Represents Device #2. Each Device consists of one IDT70V3579 for this waveform, and are setup for depth expansion in this example. $ADDRESS_{(B1)} = ADDRESS_{(B2)}$ in this situation.
2. \overline{BE}_n , \overline{OE} , and $\overline{ADS} = V_{IL}$; $CE_1(B1)$, $CE_1(B2)$, R/\overline{W} , \overline{CNTEN} , and $\overline{CNTRST} = V_{IH}$.

4830 drw 07

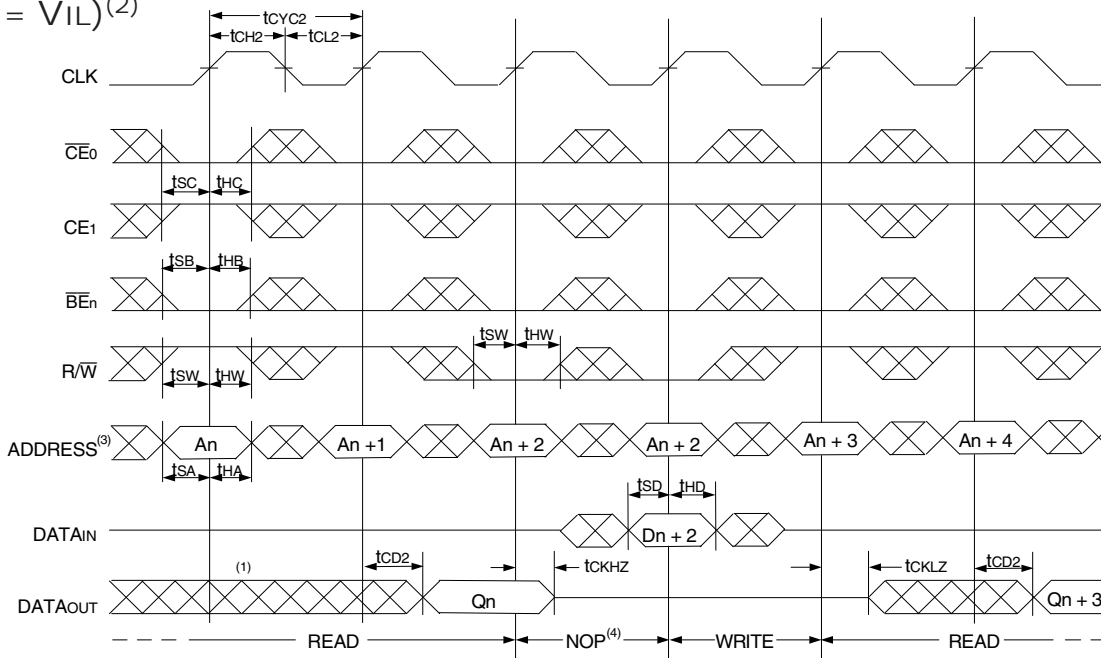
Timing Waveform of Left Port Write to Pipelined Right Port Read^(1,2)



NOTES:

1. \overline{CE}_0 , \overline{BE}_n , and $\overline{ADS} = V_{IL}$; CE_1 , $CNTEN$, and $CNTRST = V_{IH}$.
2. $\overline{OE} = V_{IL}$ for the Right Port, which is being read from. $\overline{OE} = V_{IH}$ for the Left Port, which is being written to.
3. If $t_{CO} \leq$ minimum specified, then data from right port read is not valid until following right port clock cycle (ie, time from write to valid read on opposite port will be $t_{CO} + 2 t_{CYC2} + t_{CD2}$). If $t_{CO} >$ minimum, then data from right port read is available on first right port clock cycle (ie, time from write to valid read on opposite port will be $t_{CO} + t_{CYC2} + t_{CD2}$).

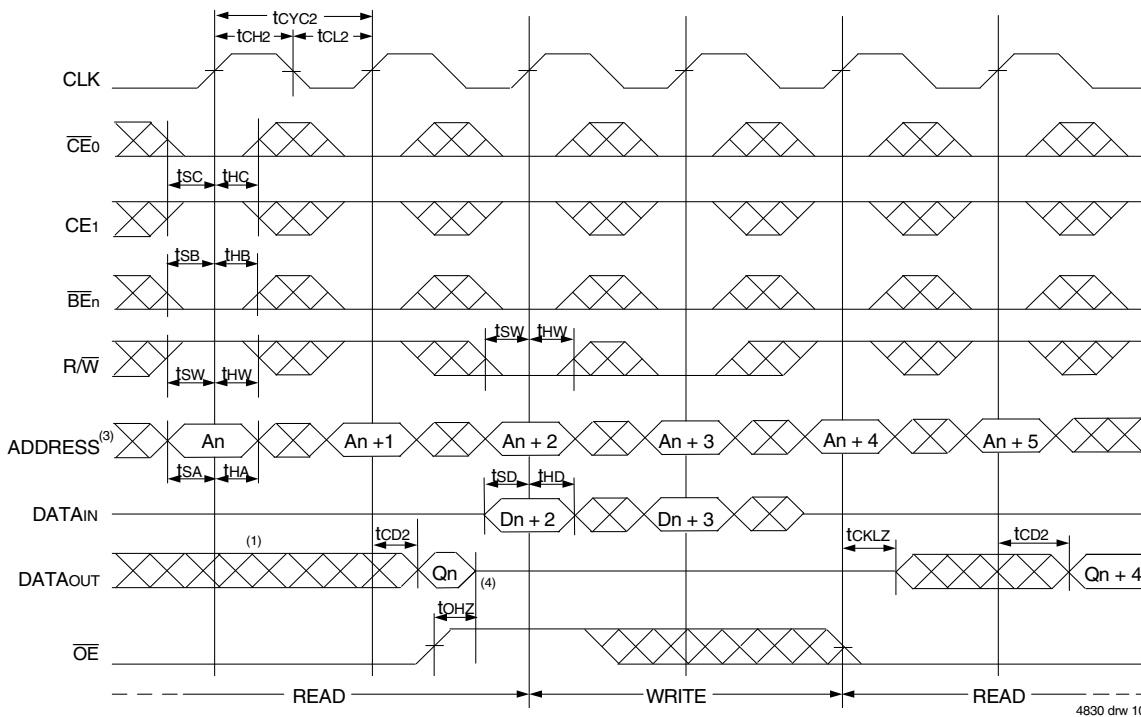
Timing Waveform of Pipelined Read-to-Write-to-Read ($\overline{OE} = V_{IL}$)⁽²⁾



NOTES:

1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2. \overline{CE}_0 , \overline{BE}_n , and $\overline{ADS} = V_{IL}$; CE_1 , $CNTEN$, and $CNTRST = V_{IH}$. "NOP" is "No Operation".
3. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be rewritten to guarantee data integrity.

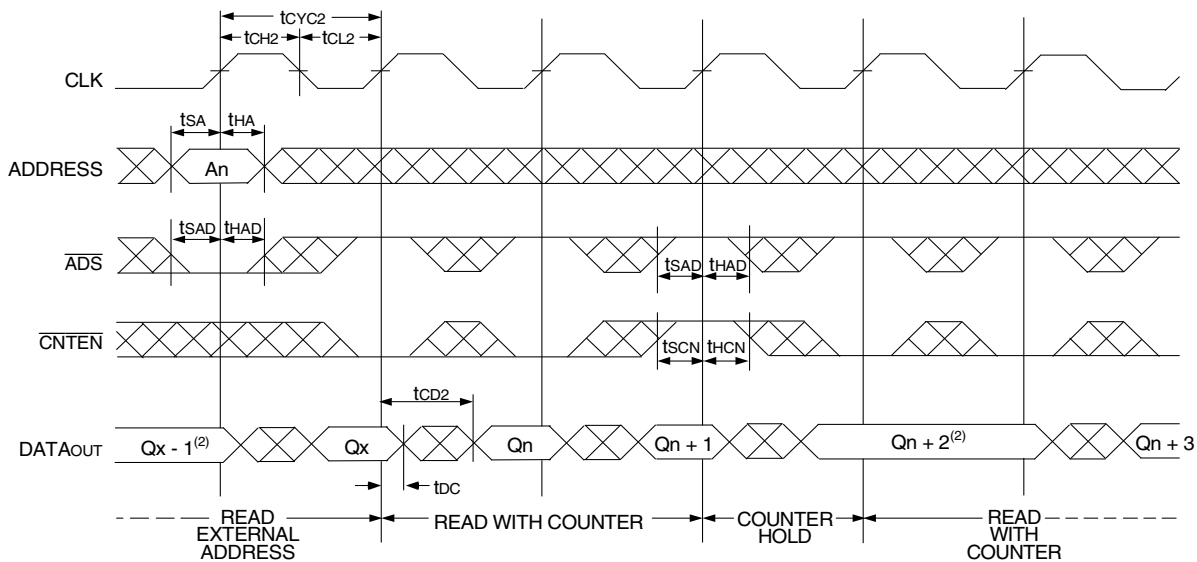
Timing Waveform of Pipelined Read-to-Write-to-Read (\overline{OE} Controlled)⁽²⁾



NOTES:

1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2. \overline{CE}_0 , \overline{BE}_n , and $\overline{ADS} = V_{IL}$; \overline{CE}_1 , \overline{CNTEN} , and $\overline{CNTRST} = V_{IH}$.
3. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. This timing does not meet requirements for fastest speed grade. This waveform indicates how logically it could be done if timing so allows.

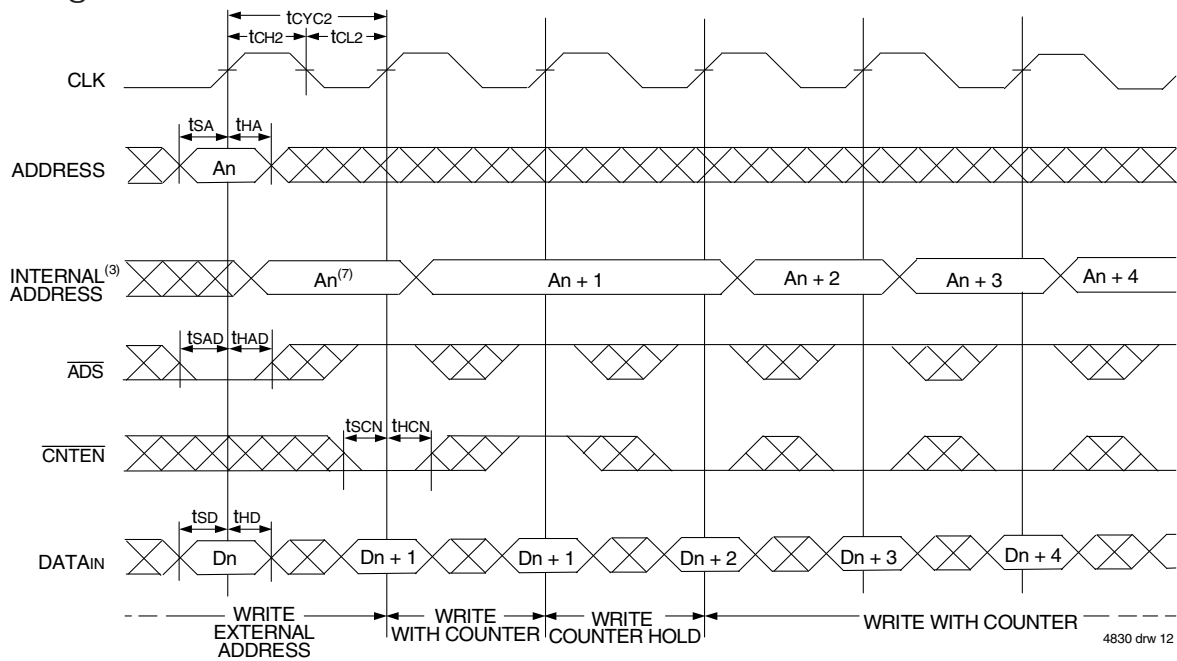
Timing Waveform of Pipelined Read with Address Counter Advance⁽¹⁾



NOTES:

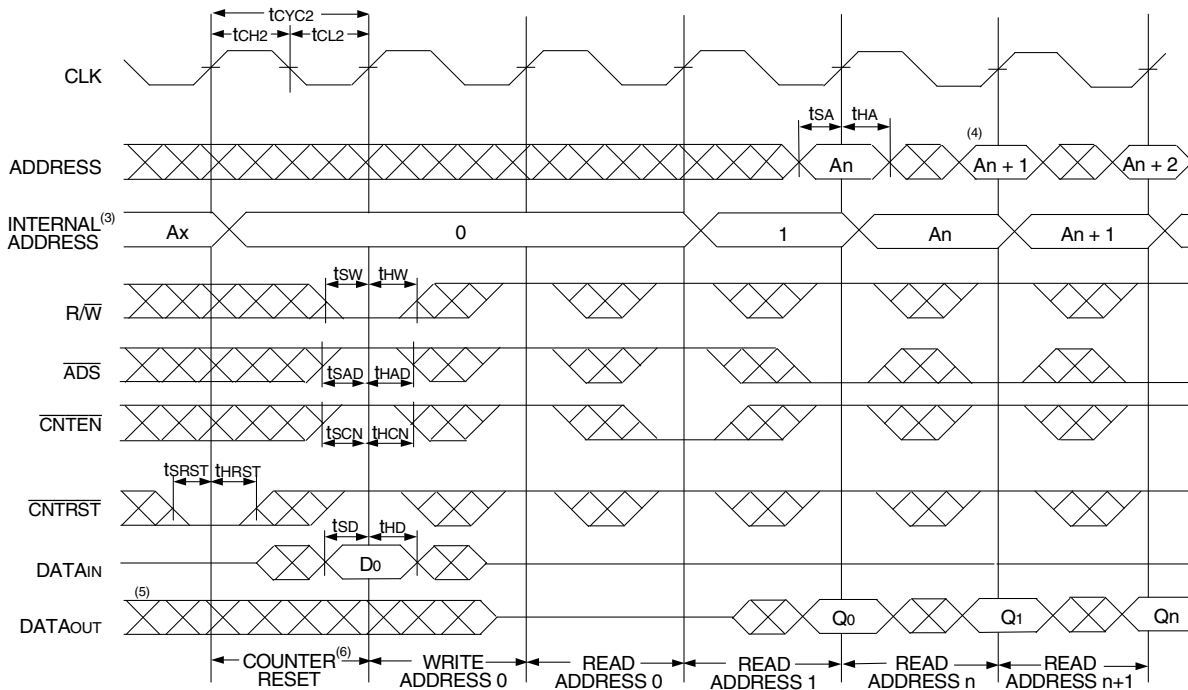
1. \overline{CE}_0 , \overline{OE} , $\overline{BE}_n = V_{IL}$; \overline{CE}_1 , $\overline{R/W}$, and $\overline{CNTRST} = V_{IH}$.
2. If there is no address change via $\overline{ADS} = V_{IL}$ (loading a new address) or $\overline{CNTEN} = V_{IL}$ (advancing the address), i.e. $\overline{ADS} = V_{IH}$ and $\overline{CNTEN} = V_{IH}$, then the data output remains constant for subsequent clocks.

Timing Waveform of Write with Address Counter Advance⁽¹⁾



4830 drw 12

Timing Waveform of Counter Reset⁽²⁾



4830 drw 13

NOTES:

1. \overline{CE}_0 , \overline{BE}_n , and $R/\overline{W} = V_{IL}$; CE_1 and $\overline{CNTRST} = V_{IH}$.
2. \overline{CE}_0 , $\overline{BE}_n = V_{IL}$; $CE_1 = V_{IH}$.
3. The "Internal Address" is equal to the "External Address" when $\overline{ADS} = V_{IL}$ and equals the counter output when $\overline{ADS} = V_{IH}$.
4. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
6. No dead cycle exists during counter reset. A READ or WRITE cycle may be coincidental with the counter reset cycle: Addr 0 will be accessed. Extra cycles are shown here simply for clarification.
7. $\overline{CNTEN} = V_{IL}$ advances Internal Address from 'An' to 'An +1'. The transition shown indicates the time required for the counter to advance. The 'An +1' Address is written to during this cycle.

Functional Description

The IDT70V3579 provides a true synchronous Dual-Port Static RAM interface. Registered inputs provide minimal set-up and hold times on address, data, and all critical control inputs. All internal registers are clocked on the rising edge of the clock signal, however, the self-timed internal write pulse is independent of the LOW to HIGH transition of the clock signal.

An asynchronous output enable is provided to ease asynchronous bus interfacing. Counter enable inputs are also provided to stall the operation of the address counters for fast interleaved memory applications.

A HIGH on $\overline{CE_0}$ or a LOW on CE_1 for one clock cycle will power down the internal circuitry to reduce static power consumption. Multiple chip enables allow easier banking of multiple IDT70V3579s for depth expansion configurations. Two cycles are required with $\overline{CE_0}$ LOW and CE_1 HIGH to reactivate the outputs.

Depth and Width Expansion

The IDT70V3579 features dual chip enables (refer to Truth Table I) in order to facilitate rapid and simple depth expansion with no requirements for external logic. Figure 4 illustrates how to control the various chip enables in order to expand two devices in depth.

The IDT70V3579 can also be used in applications requiring expanded width, as indicated in Figure 4. Through combining the control signals, the devices can be grouped as necessary to accommodate applications needing 72-bits or wider.

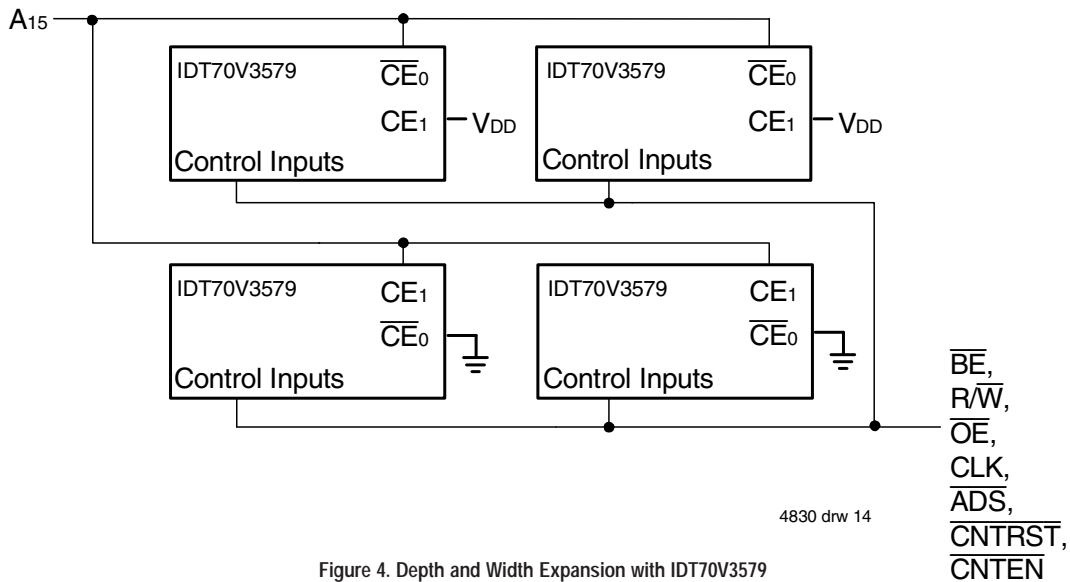
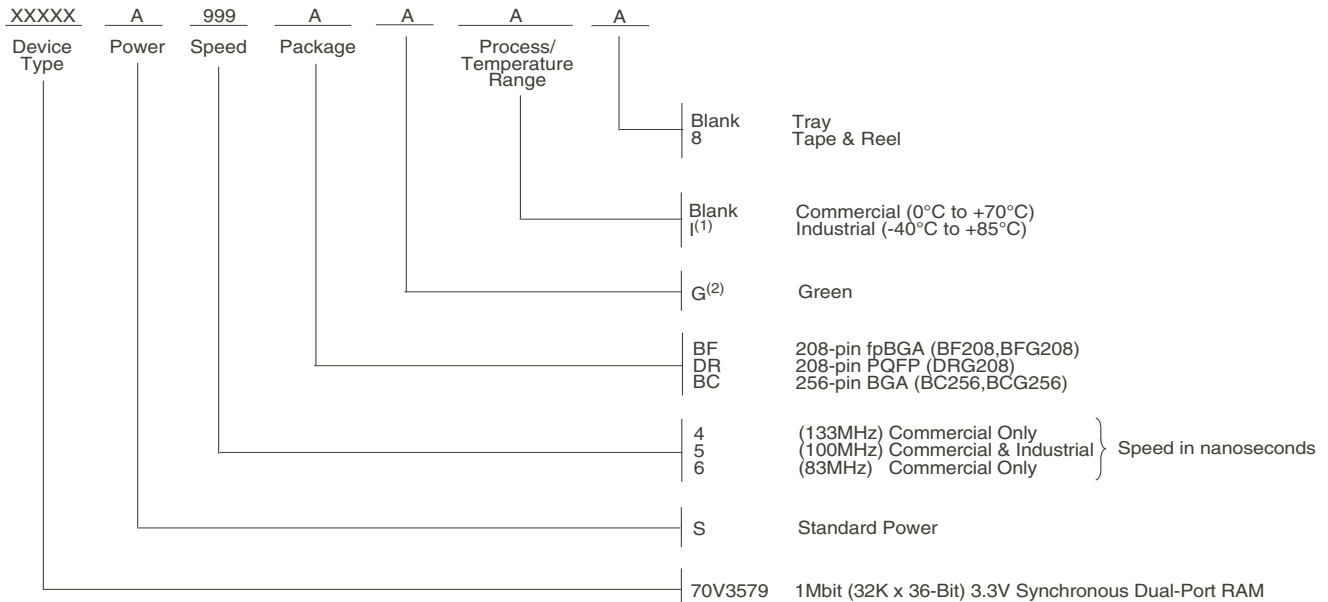


Figure 4. Depth and Width Expansion with IDT70V3579

Ordering Information



NOTES:

4830 drw 15

- Contact your local sales office for additional industrial temp range speeds, packages and powers.
- Green parts available. For specific speeds, packages and powers contact your local sales office.
LEAD FINISH (SnPb) parts are Obsolete excluding BGA and fpBGA. Product Discontinuation Notice - PDN# SP-17-02
 Note that information regarding recently obsoleted parts are included in this datasheet for customer convenience.

Orderable Part Information

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
4	70V3579S4BC	BC256	CABGA	C
	70V3579S4BC8	BC256	CABGA	C
	70V3579S4BCG	BCG256	CABGA	C
	70V3579S4BF	BF208	CABGA	C
	70V3579S4BF8	BF208	CABGA	C
	70V3579S4BFG	BFG208	CABGA	C
	70V3579S4DRG	DRG208	PQFP	C
5	70V3579S5BC	BC256	CABGA	C
	70V3579S5BC8	BC256	CABGA	C
	70V3579S5BCGI	BCG256	CABGA	I
	70V3579S5BCI	BC256	CABGA	I
	70V3579S5BCI8	BC256	CABGA	I
	70V3579S5BF	BF208	CABGA	C
	70V3579S5BF8	BF208	CABGA	C
	70V3579S5BFI	BF208	CABGA	I
	70V3579S5BFI8	BF208	CABGA	I
6	70V3579S6BC	BC256	CABGA	C
	70V3579S6BC8	BC256	CABGA	C
	70V3579S6BCI	BC256	CABGA	I
	70V3579S6BCI8	BC256	CABGA	I
	70V3579S6BF	BF208	CABGA	C
	70V3579S6BF8	BF208	CABGA	C

Datasheet Document History

12/09/98:	Initial Public Release
03/12/99:	Added fpBGA package
04/28/99:	Fixed typo on page 10
06/08/99:	Changed drawing format
	Page 2 Changed package body dimensions
06/15/99:	Page 5 Deleted note 6 for Table II
08/04/99:	Page 6 Improved power numbers
10/04/99:	Upgraded speed to 133MHz, added 2.5V I/O capability
10/19/99:	Page 4 Corrected I/O numbers in Truth Table I
11/12/99:	Replaced IDT logo
04/10/00:	Added new BGA package, added full 2.5V interface capability
01/12/01:	Page 6 Updated Truth Table II
	Increased storage temperature parameter
	Clarified TA Parameter
	Page 8 DC Electrical parameters--changed wording from "open" to "disabled"
	Removed note 7 on DC Electrical Characteristics table
	Removed Preliminary status
04/10/01:	Added Industrial Temperature Ranges and removed related notes
07/19/01:	Page 3 Replaced incorrect BGA package drawing
12/12/01:	Page 2, 3 & 4 Added date revision to pin configurations
	Page 6 Removed industrial temp footnote from table 04
	Page 8 & 10 Removed industrial temp for 6ns from DC & AC Electrical Characteristics
	Page 16 Removed industrial temp from 6ns in ordering information
	Added industrial temp footnote
	Page 1 & 17 Replaced TM logo with ® logo
02/07/06:	Page 1 Added green availability to features
	Page 5 Changed footnote 2 for Truth Table I from $\overline{\text{ADS}}, \overline{\text{CNTEN}}, \overline{\text{CNTRST}} = \text{V}_{\text{IH}}$ to $\overline{\text{ADS}}, \overline{\text{CNTEN}}, \overline{\text{CNTRST}} = \text{X}$
	Page 16 Added green indicator to ordering information
07/25/08:	Page 8 Corrected a typo in the DC Chars table
10/23/08:	Page 16 Removed "IDT" from orderable part number
10/10/14:	Page 15 Added Tape and Reel to the Ordering Information
02/16/18:	Product Discontinuation Notice - PDN# SP-17-02
	Last time buy expires June 15, 2018
08/02/19:	Page 2, 3 & 4 Updated package codes BF-208 to BF208, BFG208, DR-208 to DRG208 & BC-256 to BC256 BCG256
	Page 16 Added Orderable Part Information table

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[IS64WV3216BLL-15CTLA3](#) [IS66WVE4M16ECLL-70BLI](#) [PCF8570P](#) [K6F2008V2E-LF70000](#) [K6T4008C1B-GB70](#) [CY7C1353S-100AXC](#)
[AS6C8016-55BIN](#) [AS7C164A-15PCN](#) [515712X](#) [IDT71V67603S133BG](#) [IS62WV51216EBLL-45BLI](#) [IS63WV1288DBLL-10HLI](#)
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[133AXI](#) [8602501XA](#) [5962-3829425MUA](#) [5962-3829430MUA](#) [5962-8866201YA](#) [5962-8866204TA](#) [5962-9062007MXA](#) [5962-](#)
[9161705MXA](#) [GS882Z18CD-150I](#) [8413202RA](#) [5962-8866208YA](#) [5962-8866203YA](#) [IS61WV102416DBLL-10BLI](#) [IS66WVC2M16ECLL-](#)
[7010BLI](#) [CY7C1380KV33-250AXC](#) [AS6C8016-55BINTR](#) [GS81284Z18B-250I](#) [AS7C34096B-10TIN](#) [GS84018CB-200I](#)
[IS62WV25616EALL-55TLI](#) [IS61WV204816BLL-10TLI](#) [GS8128418B-167IV](#) [CY7C1460KV25-200BZXI](#) [CY7C1315KV18-333BZXC](#)
[CY62157G30-45ZSXI](#) [71V016SA12YG](#) [RMLV0416EGBG-4S2#AC0](#) [CY62126EV18LL-70BVXI](#)