SPREAD SPECTRUM CLOCK GENERATOR
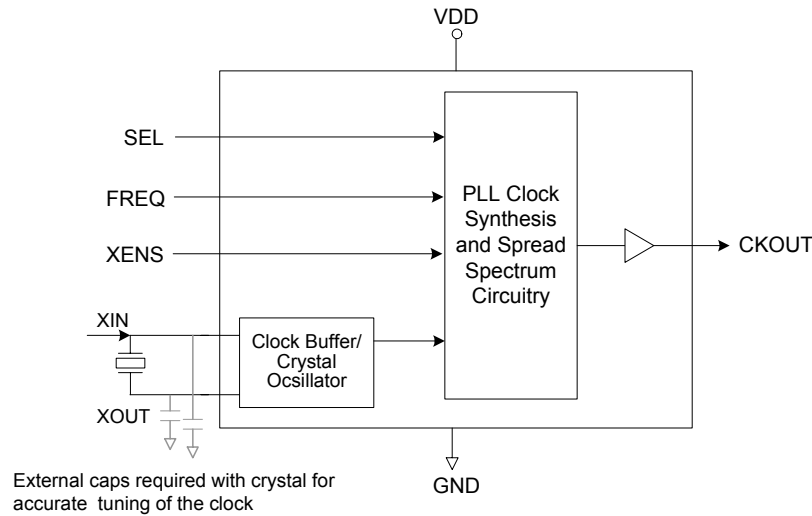
ICS7152A

Description

The ICS7152A-02 and -11 are clock generators for EMI (Electromagnetic Interference) reduction (see below for frequency ranges and multiplier ratios). Spectral peaks are attenuated by modulating the system clock frequency. Down or center spread profiles are selectable. Down spread will not exceed the maximum frequency of an unspread clock, and center spread does not change the average operating frequency of the system

IDT offers many other clocks for computers and computer peripherals. Consult IDT when you need to remove crystals and oscillators from your board.

Features

- Operating voltage of 3.3 V ±0.3 V
- Packaged in 8-pin SOIC
- Input frequency range of 16.6 to 134.0 MHz
- Output frequency range of 16.6 to 134.0 MHz
- Provides a spread spectrum clock output (±0.5%, ±1.5% center spread; -1.0%, -3.0% down spread)
- Low cycle-to-cycle jitter - less than 100 ps
- Advanced, low-power CMOS process
- Industrial and commercial temperature ranges
- Pb (lead) free package, RoHS compliant
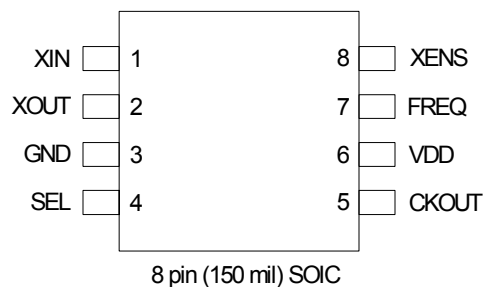- Pin compatible with Fujitsu MB88152-102 and -111

Block Diagram

External caps required with crystal for accurate tuning of the clock

Product Lineup

Product	Input Frequency Range	Modulation Type	Modulation Enable Pin
ICS7152AM-02, ICS7152AMI-02	40.0 MHz to 134.0 MHz	Down spread	Yes
ICS7152AM-11, ICS7152AMI-11	16.6 MHz to 67.0 MHz	Center spread	

Pin Assignment

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         ┌─────────────┐
 XIN  ─┤ 1         8 ├─ XENS
 XOUT ─┤ 2         7 ├─ FREQ
 GND  ─┤ 3         6 ├─ VDD
 SEL  ─┤ 4         5 ├─ CKOUT
         └─────────────┘
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8 pin (150 mil) SOIC

Modulation Enable Select Table

XENS Pin 8	Modulation
0	Modulation
1	No modulation

Spread Direction and Percentage Select Table

SEL Pin 4	Spread Direction	Spread Percentage (%)	Part Number
0	Center	±0.5	ICS7152AM-11
	Down	-1.0	ICS7152AM-02
1	Center	±1.5	ICS7152AM-11
	Down	-3.0	ICS7152AM-02

Frequency Select Table

FREQ Pin 7	Frequency	
0	16.6 to 40 MHz	ICS7152AM-11
	40 to 80 MHz	ICS7152AM-02
1	33 to 67 MHz	ICS7152AM-11
	66 to 134 MHz	ICS7152AM-02

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	XIN	Input	Crystal/clock input pin.
2	XOUT	Output	Crystal.
3	GND	Power	Connect to ground.
4	SEL	Input	Spread modulation select.
5	CKOUT	Output	Clock output.
6	VDD	Power	Connect to +3.3 V.
7	FREQ	Input	Frequency select.
8	XENS	Input	Modulation enable select.

External Components

The ICS7152A requires a minimum number of external components for proper operation.

Decoupling Capacitor

A decoupling capacitor of 0.01µF must be connected between GND and VDD on pins 3 and 6, as close to these pins as possible. For optimum device performance, the decoupling capacitor should be mounted on the component side of the PCB. Avoid the use of vias in the decoupling circuit.

Series Termination Resistor

Series termination should be used on the clock output. To series terminate a 50Ω trace (a commonly used trace impedance) place a 27Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 25Ω

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1) The 0.01µF decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between the decoupling capacitor and VDD pin. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via.

2) To minimize EMI, the 27Ω series termination resistor (if needed) should be placed close to the clock output.

3) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers. Other signal traces should be routed away from the ICS7152A. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

Crystal Information

The crystal used should be a fundamental mode, parallel resonant. Crystal capacitors should be connected from pins X1 to ground and X2 to ground to optimize the initial accuracy. The value of these capacitors is given by the following equation:

$$\text{Crystal caps (pF)} = (C_L - 6) \times 2$$

In the equation, C_L is the crystal load capacitance. So, for a crystal with a 16 pF load capacitance, two 20 pF [(16-6) x 2] capacitors should be used.

Spread Spectrum Profile

The ICS7152A low EMI clock generator uses a triangular frequency modulation profile for optimal down stream tracking of zero delay buffers and other PLL devices. The frequency modulation amplitude is constant with variations of the input frequency.
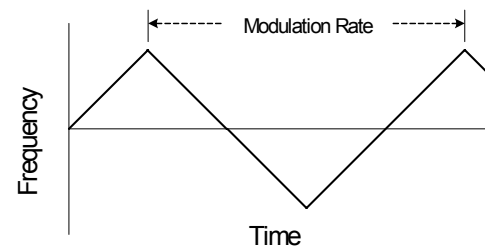
Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS7152A. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	-0.5 to 4.0 V
All Inputs and Outputs (referenced to GND)	-0.5 V to VDD+0.5 V
Ambient Operating Temperature	-40 to +85° C
Storage Temperature	-55 to +125° C
Junction Temperature	-40 to +125° C
Soldering Temperature	260° C
Overshoot (V_{IOVER})	VDD + 1.0 V ($t_{OVER} \leq$ 50 ns) max
Undershoot (V_{IUNDER})	GND - 1.0 V ($t_{UNDER} \leq$ 50 ns) min

Overshoot/Undershoot
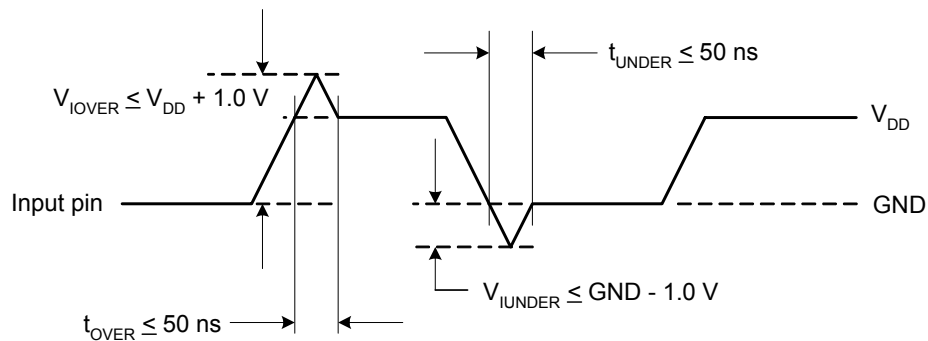
Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	-40		+85	° C
Power Supply Voltage (measured in respect to GND)	+3.0	3.3	3.6	V

DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±0.3 V**, Ambient Temperature -40 to +85°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.0	3.3	3.6	V
Supply Current	IDD	No load, at 3.3 V, output = 24 MHz		10	14	mA
Input High Voltage	V_{IH}	SEL, FREQ, XENS	VDD x 0.8		VDD + 0.3	V
		XIN, Input slew rate 3 V/ns, 16.6 to 100 MHz	VDD x 0.8		VDD + 0.3	V
		XIN, Input slew rate 3 V/ns, 100 to 134 MHz	VDD x 0.9		VDD + 0.3	V
Input Low Voltage	V_{IL}	SEL, FREQ, XENS	GND		VDD x 0.20	V
		XIN, Input slew rate 3 V/ns, 16.6 to 100 MHz	GND		VDD x 0.20	V
		XIN, Input slew rate 3 V/ns, 100 to 134 MHz	GND		VDD x 0.10	V
Output High Voltage	V_{OH}	CKOUT, I_{OH} = -4 mA	VDD - 0.5		VDD	V
Output Low Voltage	V_{OL}	CKOUT, I_{OL} = 4 mA	GND		0.4	V
Input Capacitance	C_{IN}	XIN, SEL, XENS			16	pF
Load Capacitance	C_L	CKOUT, 16.6 to 67 MHz			15	pF
		CKOUT, 67 to 100 MHz			10	pF
		CKOUT, 100 to 134 MHz			7	pF
Output Impedance	Z_O	CKOUT, 16.6 to 134 MHz		25		Ω

AC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±0.3 V**, Ambient Temperature -40 to +85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Oscillation Frequency	f_X	XIN, XOUT, Fundamental oscillation	16.6		40	MHz
		XIN, XOUT, 3rd over tone, note 1	40		48	MHz
Input Frequency	f_{IN}	XIN, ICS7152A-11	16.6		67	MHz
		XIN, ICS7152A-02	40		134	MHz
Output Frequency	f_{OUT}	CKOUT, ICS7152A-11	16.6		67	MHz
		CKOUT, ICS7152A-02	40		134	MHz
Input Clock Duty Cycle	t_{DCI}	XIN, 16.6 to 100 MHz	40	50	60	%
		XIN, 100 to 134 MHz	45	50	55	%
Output Clock Duty Cycle	t_{DCC}	CKOUT, 1.5 V	40		60	%
Output Slew Rate		CKOUT, 0.4 to 2.4 V, load capacitance 15 pF	0.5	TBD	3.0	V/ns
Cycle to Cycle Jitter	t_{JC}	No load, standard deviation		TBD	100	ps
Lock Time	t_{LK}	CKOUT		2	5	ms
Modulation Frequency	f_{MOD}	CKOUT=TBD		33		kHz

Note 1: Contact ICS Applications for more information.

Input Frequency ($f_{IN} = 1/t_{IN}$)
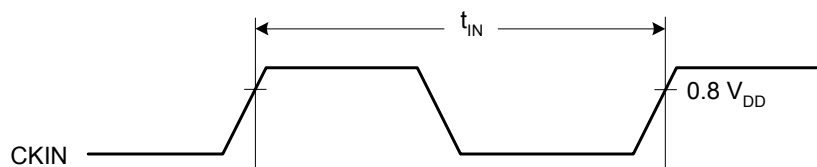
Output Slew Rate
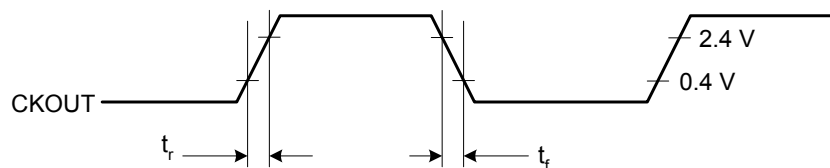
$SR = (2.4 - 0.4) / t_r$, $SR = (2.4 - 0.4) / t_f$

Thermal Characteristics

| Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		150		$^\circ$C/W
	θ_{JA}	1 m/s air flow		140		$^\circ$C/W
	θ_{JA}	3 m/s air flow		120		$^\circ$C/W
Thermal Resistance Junction to Case	θ_{JC}			40		$^\circ$C/W

Package Outline and Package Dimensions (8-pin SOIC, 150 Mil. Body)

Package dimensions are kept current with JEDEC Publication No. 95
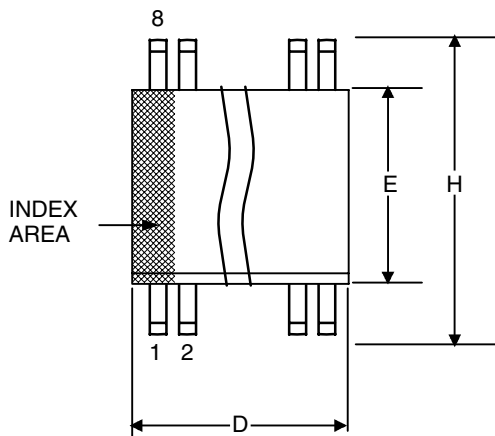
Symbol	Millimeters		Inches*	
	Min	Max	Min	Max
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.013	.020
C	0.19	0.25	.0075	.0098
D	4.80	5.00	.1890	.1968
E	3.80	4.00	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°

*For reference only. Controlling dimensions in mm.

INDEX AREA

SEATING PLANE

- C -

.10 (.004) C

h x 45°
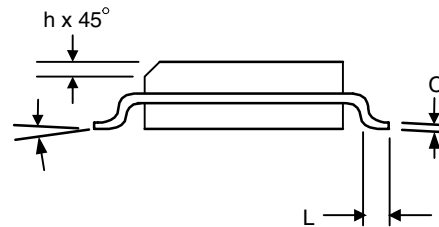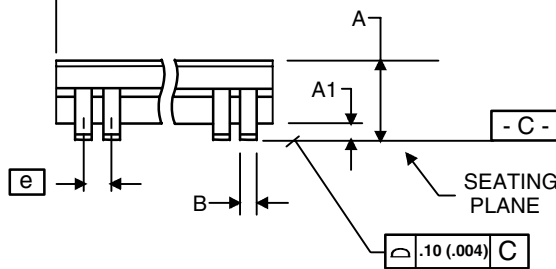
Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
7152AM-02LF	152AM02L	Tubes	8-pin SOIC	0 to +70° C
7152AM-02LFT	152AM02L	Tape and Reel	8-pin SOIC	0 to +70° C
7152AMI-02LF	52AMI02L	Tubes	8-pin SOIC	-40 to +85° C
7152AMI-02LFT	52AMI02L	Tape and Reel	8-pin SOIC	-40 to +85° C
7152AM-11LF	7152A11L	Tubes	8-pin SOIC	0 to +70° C
7152AM-11LFT	7152A11L	Tape and Reel	8-pin SOIC	0 to +70° C
7152AMI-11LF	152AI11L	Tubes	8-pin SOIC	-40 to +85° C
7152AMI-11LFT	152AI11L	Tape and Reel	8-pin SOIC	-40 to +85° C

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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Revision History

Rev.	Originator	Date	Description of Change
A	J. Sarma	10/20/05	Rev A; new device/datasheet.
B		01/10/08	Updated the -11 device markings.
D		11/04/09	Added EOL note for non-green parts.

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