CMOS SyncBiFIFO™ 256 x 36 x 2, 512 x 36 x 2, 1,024 x 36 x 2

IDT723622
IDT723632
IDT723642

FEATURES:

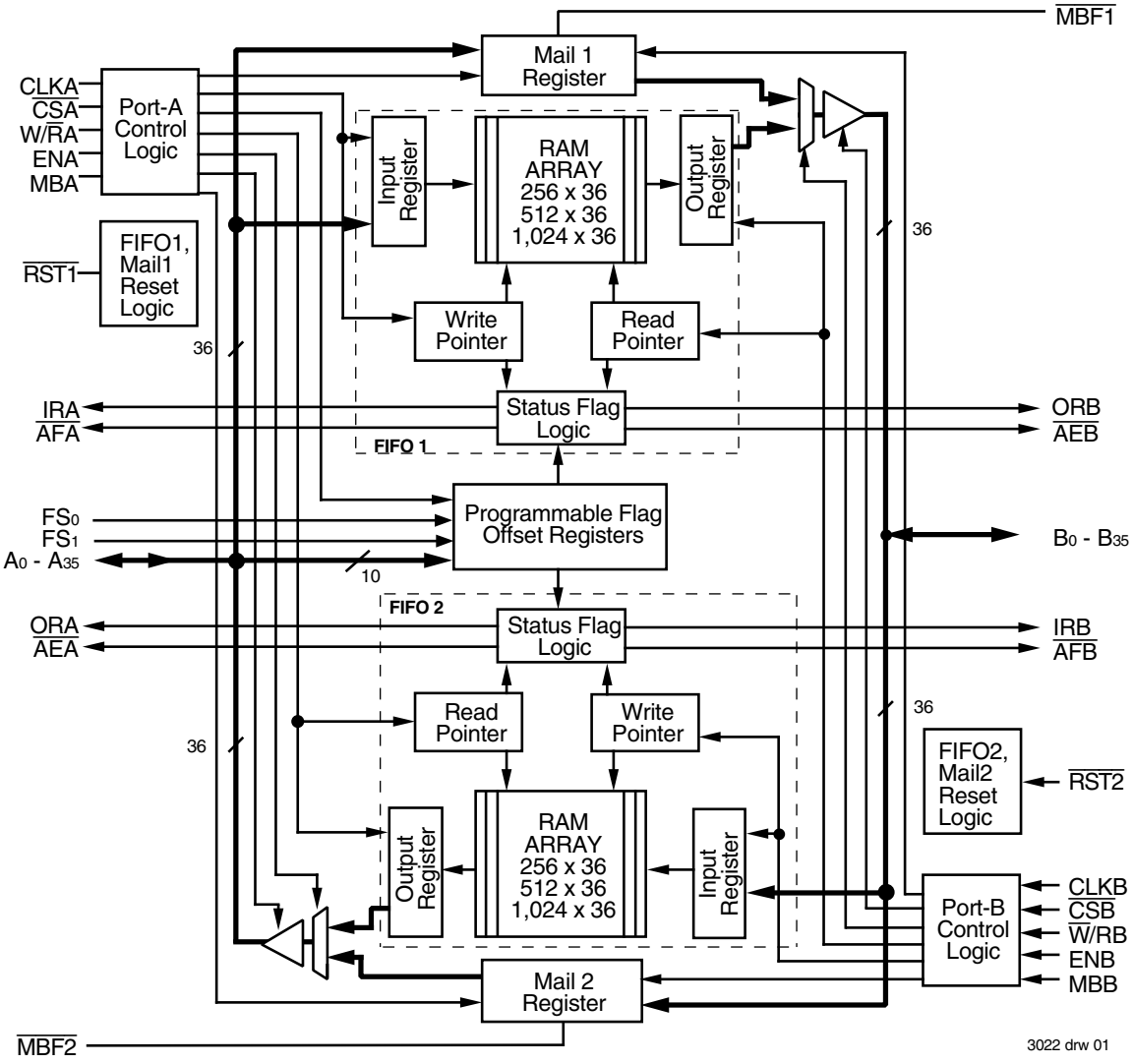
- Memory storage capacity:
  - IDT723622 – 256 x 36 x 2
  - IDT723632 – 512 x 36 x 2
  - IDT723642 – 1,024 x 36 x 2
- Free-running CLKA and CLKB may be asynchronous or coincident (simultaneous reading and writing of data on a single clock edge is permitted)
- Two independent clocked FIFOs buffering data in opposite directions
- Mailbox bypass register for each FIFO
- Programmable Almost-Full and Almost-Empty flags
- Microprocessor Interface Control Logic
- IRA, ORA, $\overline{AEA}$, and $\overline{AFA}$ flags synchronized by CLKA
- IRB, ORB, $\overline{AEB}$, and $\overline{AFB}$ flags synchronized by CLKB
- Supports clock frequencies up to 66.7MHz
- Fast access times of 10ns
- Available in space-saving 120-pin Thin Quad Flatpack (TQFP)
- Green parts available

DESCRIPTION:

The IDT723622/723632/723642 are a monolithic, high-speed, low-power, CMOS Bidirectional SyncFIFO (clocked) memory which supports clock frequencies up to 66.7MHz and have read access times as fast as 10ns. Two independent 256/512/1,024 x 36 dual-port SRAM FIFOs on board each chip buffer data in opposite directions. Communication between each port may bypass the FIFOs via two 36-bit mailbox registers. Each mailbox register has a flag to signal when new mail has been stored.

These devices are a synchronous (clocked) FIFO, meaning each port employs a synchronous interface. All data transfers through a port are gated to the LOW-to-HIGH transition of a port clock by enable signals. The clocks for each port are independent of one another and can be asynchronous or

FUNCTIONAL BLOCK DIAGRAM



DESCRIPTION (CONTINUED)

coincident. The enables for each port are arranged to provide a simple bidirectional interface between microprocessors and/or buses with synchronous control.

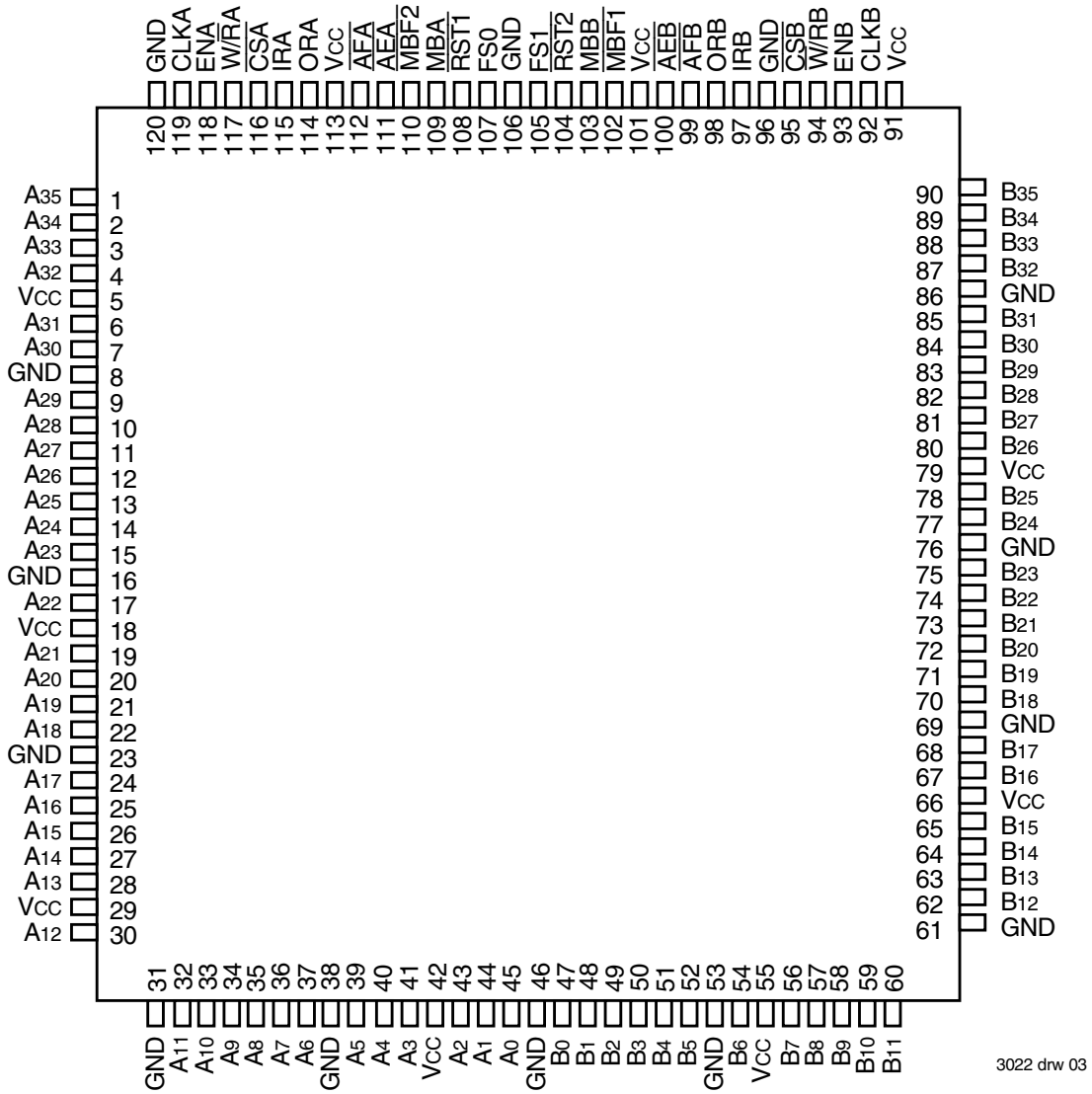
Each FIFO has a programmable Almost-Empty flag ($\overline{AEA}$ and $\overline{AEB}$) and a progammable Almost-Full flag ($\overline{AFA}$ and $\overline{AFB}$). $\overline{AEA}$ and $\overline{AEB}$ indicate when a selected number of words remain in the FIFO memory. $\overline{AFA}$ and $\overline{AFB}$ indicate when the FIFO contains more than a selected number of words.

The Input Ready (IRA, IRB) and Almost-Full ($\overline{AFA}$, $\overline{AFB}$) flags of a FIFO are two-stage synchronized to the port clock that writes data into its array. The Output Ready (ORA, ORB) and Almost-Empty ($\overline{AEA}$, $\overline{AEB}$) flags of a FIFO are two-stage synchronized to the port clock that reads data from its array. Offset values for the Almost-Full and Almost-Empty flags of both FIFOs can be programmed from Port A.

Two or more devices may be used in parallel to create wider data paths. If, at any time, the FIFO is not actively performing a function, the chip will automatically power down. During the power down state, supply current consumption (I_{CC}) is at a minimum. Initiating any operation (by activating control inputs will immediately take the device out of the power down state.

The 723622/723632/723642 are characterized for operation from 0°C to 70°C. They are fabricated using high speed, submicron CMOS technology.

PIN CONFIGURATION



3022 drw 03

TQFP (PNG120, order code: PF)
TOP VIEW

PIN DESCRIPTIONS

Symbol	Name	I/O	Description
A0-A35	Port A Data	I/0	36-bit bidirectional data port for side A.
$\overline{AEA}$	Port A Almost-Empty Flag	O (Port A)	Programmable Almost-Empty flag synchronized to CLKA. It is LOW when the number of words in FIFO2 is less than or equal to the value in the Almost-Empty A Offset register, X2.
$\overline{AEB}$	Port B Almost-Empty Flag	O (Port B)	Programmable Almost-Empty flag synchronized to CLKB. It is LOW when the number of words in FIFO1 is less than or equal to the value in the Almost-Empty B Offset register, X1.
$\overline{AFA}$	Port A Almost-Full Flag	O (Port A)	Programmable Almost-Full flag synchronized to CLKA. It is LOW when the number of empty locations in FIFO1 is less than or equal to the value in the Almost-Full A Offset register, Y1.
$\overline{AFB}$	Port B Almost-Full Flag	O (Port B)	Programmable Almost-Full flag synchronized to CLKB. It is LOW when the number of empty locations in FIFO2 is less than or equal to the value in the Almost-Full B Offset register, Y2.
B0 - B35	Port B Data	I/O	36-bit bidirectional data port for side B.
CLKA	Port A Clock	I	CLKA is a continuous clock that synchronizes all data transfers through port A and can be asynchronous or coincident to CLKB. IRA, ORA, $\overline{AFA}$, and $\overline{AEA}$ are all synchronized to the LOW-to-HIGH transition of CLKA.
CLKB	Port B Clock	I	CLKB is a continuous clock that synchronizes all data transfers through port B and can be asynchronous or coincident to CLKA. IRB, ORB, $\overline{AFB}$, and $\overline{AEB}$ are synchronized to the LOW-to-HIGH transition of CLKB.
$\overline{CSA}$	Port A Chip Select	I	$\overline{CSA}$ must be LOW to enable a LOW-to-HIGH transition of CLKA to read or write on port A. The A0-A35 outputs are in the high-impedance state when $\overline{CSA}$ is HIGH.
$\overline{CSB}$	Port B Chip Select	I	$\overline{CSB}$ must be LOW to enable a LOW-to-HIGH transition of CLKB to read or write data on port B. The B0-B35 outputs are in the high-impedance state when $\overline{CSB}$ is HIGH.
ENA	Port A Enable	I	ENA must be HIGH to enable a LOW-to-HIGH transition of CLKA to read or write data on port A.
ENB	Port B Enable	I	ENB must be HIGH to enable a LOW-to-HIGH transition of CLKB to read or write data on port B.
FS1, FS0	Flag Offset Selects	I	The LOW-to-HIGH transition of a FIFO's Reset input latches the values of FS0 and FS1. If either FS0 or FS1 is HIGH when a Reset goes HIGH, one of three preset values is selected as the offset for the FIFOs Almost-Full and Almost-Empty flags. If both FIFOs are reset simultaneously and both FS0 and FS1 are LOW when $\overline{RST1}$ and $\overline{RST2}$ go HIGH, the first four writes to FIFO1 load the Almost-Empty and Almost-Full offsets for both FIFOs.
IRA	Input Ready Flag	O (Port A)	IRA is synchronized to the LOW-to-HIGH transition of CLKA. When IRA is LOW, FIFO1 is full and writes to its array are disabled. IRA is set LOW when FIFO1 is reset and is set HIGH on the second LOW-to-HIGH transition of CLKA after reset.
IRB	Input Ready Flag	O (Port B)	IRB is synchronized to the LOW-to-HIGH transition of CLKB. When IRB is LOW, FIFO2 is full and writes to its array are disabled. IRB is set LOW when FIFO2 is reset and is set HIGH on the second LOW-to-HIGH transition of CLKB after reset.
MBA	Port A Mailbox Select	I	A HIGH level on MBA chooses a mailbox register for a port A read or write operation. When the A0-A35 outputs are active, a HIGH level on MBA selects data from the mail2 register for output and a LOW level selects FIFO2 output register data for output.
MBB	Port B Mailbox Select	I	A HIGH level on MBB chooses a mailbox register for a port B read or write operation. When the B0-B35 outputs are active, a HIGH level on MBB selects data from the mail1 register or output and a LOW level selects FIFO1 output register data for output.
$\overline{MBF1}$	Mail1 Register Flag	O	$\overline{MBF1}$ is set LOW by a LOW-to-HIGH transition of CLKA that writes data to the mail1 register. Writes to the mail1 register are inhibited while $\overline{MBF1}$ is LOW. $\overline{MBF1}$ is set HIGH by a LOW-to-HIGH transition of CLKB when a port B read is selected and MBB is HIGH. $\overline{MBF1}$ is set HIGH when FIFO1 is reset.
$\overline{MBF2}$	Mail2 Register Flag	O	$\overline{MBF2}$ is set LOW by a LOW-to-HIGH transition of CLKB that writes data to the mail2 register. Writes to the mail2 register are inhibited while $\overline{MBF2}$ is LOW. $\overline{MBF2}$ is set HIGH by a LOW-to-HIGH transition of CLKA when a port A read is selected and MBA is HIGH. $\overline{MBF2}$ is also set HIGH when FIFO2 is reset.

PIN DESCRIPTIONS (CONTINUED)

Symbol	Name	I/O	Description
ORA	Output Ready Flag	O (Port A)	ORA is synchronized to the LOW-to-HIGH transition of CLKA. When ORA is LOW, FIFO2 is empty and reads from its memory are disabled. Ready data is present on the output register of FIFO2 when ORA is HIGH. ORA is forced LOW when FIFO2 is reset and goes HIGH on the third LOW-to-HIGH transition of CLKA after a word is loaded to empty memory.
ORB	Output Ready Flag	O (Port B)	ORB is synchronized to the LOW-to-HIGH transition of CLKB. When ORB is LOW, FIFO1 is empty and reads from its memory are disabled. Ready data is present on the output register of FIFO1 when ORB is HIGH. ORB is forced LOW when FIFO1 is reset and goes HIGH on the third LOW-to-HIGH transition of CLKB after a word is loaded to empty memory.
$\overline{RST1}$	FIFO1 Reset	I	To reset FIFO1, four LOW-to-HIGH transitions of CLKA and four LOW-to-HIGH transitions of CLKB must occur while $\overline{RST1}$ is LOW. The LOW-to-HIGH transition of $\overline{RST1}$ latches the status of FS0 and FS1 for $\overline{AFA}$ and $\overline{AEB}$ offset selection. FIFO1 must be reset upon power up before data is written to its RAM.
$\overline{RST2}$	FIFO2 Reset	I	To reset FIFO2, four LOW-to-HIGH transitions of CLKA and four LOW-to-HIGH transitions of CLKB must occur while $\overline{RST2}$ is LOW. The LOW-to-HIGH transition of $\overline{RST2}$ latches the status of FS0 and FS1 for $\overline{AFB}$ and $\overline{AEA}$ offset selection. FIFO2 must be reset upon power up before data is written to its RAM.
W/$\overline{R}$A	Port A Write/ Read Select	I	A HIGH selects a write operation and a LOW selects a read operation on port A for a LOW-to-HIGH transition of CLKA. The A0-A35 outputs are in the HIGH impedance state when W/$\overline{R}$A is HIGH.
$\overline{W}$/RB	Port B Write/ Read Select	I	A LOW selects a write operation and a HIGH selects a read operation on port B for a LOW-to-HIGH transition of CLKB. The B0-B35 outputs are in the high-impedance state when $\overline{W}$/RB is LOW.

ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (Unless otherwise noted)(1)

Symbol	Rating	Commercial	Unit
V_{CC}	Supply Voltage Range	–0.5 to 7	V
V_I(2)	Input Voltage Range	–0.5 to V_{CC}+0.5	V
V_O(2)	Output Voltage Range	–0.5 to V_{CC}+0.5	V
I_{IK}	Input Clamp Current (V_I < 0 or V_I > V_{CC})	±20	mA
I_{OK}	Output Clamp Current (V_O = < 0 or V_O > V_{CC})	±50	mA
I_{OUT}	Continuous Output Current (V_O = 0 to V_{CC})	±50	mA
I_{CC}	Continuous Current Through V_{CC} or GND	±400	mA
T_{STG}	Storage Temperature Range	–65 to 150	°C

NOTES:
1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded provided the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage (Commercial)	4.5	5.0	5.5	V
V_{IH}	High-Level Input Voltage (Commercial)	2	—	—	V
V_{IL}	Low-Level Input Voltage (Commercial)	—	—	0.8	V
I_{OH}	High-Level Output Current (Commercial)	—	—	–4	mA
I_{OL}	Low-Level Output Current (Commercial)	—	—	8	mA
T_A	Operating Temperature (Commercial)	0	—	70	°C

ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (Unless otherwise noted)

Symbol	Parameter	Test Conditions		IDT723622 IDT723632 IDT723642 Commercial t_{CLK} = 15 ns			Unit
				Min.	Typ.(1)	Max.	
V_{OH}	Output Logic "1" Voltage	V_{CC} = 4.5V,	I_{OH} = –4 mA	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage	V_{CC} = 4.5V,	I_{OL} = 8 mA	—	—	0.5	V
I_{LI}	Input Leakage Current (Any Input)	V_{CC} = 5.5V,	V_I = V_{CC} or 0	—	—	±10	µA
I_{LO}	Output Leakage Current	V_{CC} = 5.5V,	V_O = V_{CC} or 0	—	—	±10	µA
I_{CC2}(2)	Standby Current (with CLKA & CLKB running)	V_{CC} = 5.5V,	V_I = V_{CC} –0.2V or 0V	—	—	8	mA
I_{CC3}(2)	Standby Current (no clocks running)	V_{CC} = 5.5V,	V_I = V_{CC} –0.2V or 0V	—	—	1	mA
C_{IN}(3)	Input Capacitance	V_I = 0,	f = 1 MHz	—	4	—	pF
C_{OUT}(3)	Output Capacitance	V_O = 0,	f = 1 MHZ	—	8	—	pF

NOTES:
1. All typical values are at V_{CC} = 5V, T_A = 25°C.
2. For additional I_{CC} information, see Figure 1, *Typical Characteristics: Supply Current (I_{CC}) vs. Clock Frequency (fs)*.
3. Characterized values, not currently tested.

DETERMINING ACTIVE CURRENT CONSUMPTION AND POWER DISSIPATION

The $I_{CC(f)}$ current for the graph in Figure 1 was taken while simultaneously reading and writing a FIFO on the IDT723622/723632/723642 with CLKA and CLKB set to f_S. All data inputs and data outputs change state during each clock cycle to consume the highest supply current. Data outputs were disconnected to normalize the graph to a zero capacitance load. Once the capacitance load per data-output channel and the number of these device's inputs driven by TTL HIGH levels are known, the power dissipation can be calculated with the equation below.

CALCULATING POWER DISSIPATION

With $I_{CC(f)}$ taken from Figure 1, the maximum power dissipation (P_T) of these FIFOs may be calculated by:

$$P_T = V_{CC} \times [I_{CC(f)} + (N \times \Delta I_{CC} \times dc)] + \Sigma(C_L \times V_{CC}^2 \times fo)$$

where:

N	=	number of outputs = 36
ΔI_{CC}	=	increase in power supply current for each input at a TTL HIGH level
dc	=	duty cycle of inputs at a TTL HIGH level of 3.4 V
C_L	=	output capacitance load
fo	=	switching frequency of an output

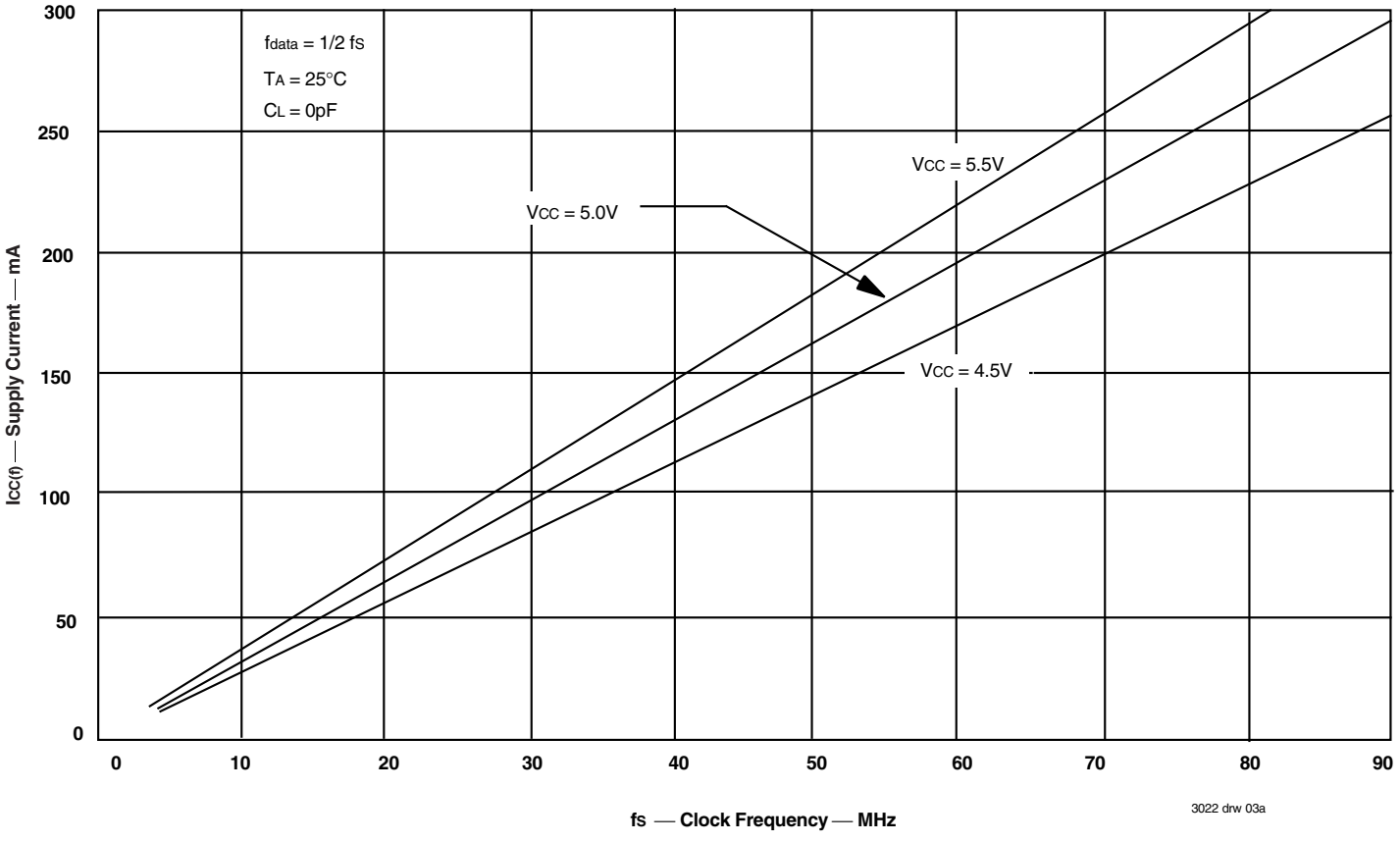


Figure 1. Typical Characteristics: Supply Current (I_{CC}) vs Clock Frequency (f_S)

TIMING REQUIREMENTS OVER RECOMMENDED RANGES OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Commercial IDT723622L15 IDT723632L15 IDT723642L15 Min.	Max.	Unit
f_S	Clock Frequency, CLKA or CLKB	—	66.7	MHz
t_{CLK}	Clock Cycle Time, CLKA or CLKB	15	—	ns
t_{CLKH}	Pulse Duration, CLKA or CLKB HIGH	6	—	ns
t_{CLKL}	Pulse Duration, CLKA and CLKB LOW	6	—	ns
t_{DS}	Setup Time, A0-A35 before CLKA↑ and B0-B35 before CLKB↑	4	—	ns
t_{ENS1}	Setup Time, $\overline{CSA}$ and W/$\overline{RA}$ before CLKA↑; $\overline{CSB}$ and $\overline{W}$/RB before CLKB↑	4.5	—	ns
t_{ENS2}	Setup Time, ENA and MBA, before CLKA↑; ENB and MBB before CLKB↑	4.5	—	ns
t_{RSTS}	Setup Time, $\overline{RST1}$ or $\overline{RST2}$ LOW before CLKA or CLKB (2)	5	—	ns
t_{FSS}	Setup Time, FS0 and FS1 before $\overline{RST1}$ and $\overline{RST2}$ HIGH	7.5	—	ns
t_{DH}	Hold Time, A0-A35 after CLKA↑ and B0-B35 after CLKB↑	1	—	ns
t_{ENH}	Hold Time, $\overline{CSA}$, W/$\overline{RA}$, ENA, and MBA after CLKA↑; $\overline{CSB}$, $\overline{W}$/RB, ENB, and MBB after CLKB↑	1	—	ns
t_{RSTH}	Hold Time, $\overline{RST1}$ or $\overline{RST2}$ LOW after CLKA↑ or CLKB↑(2)	4	—	ns
t_{FSH}	Hold Time, FS0 and FS1 after $\overline{RST1}$ and $\overline{RST2}$ HIGH	2	—	ns
t_{SKEW1}(2)	Skew Time, between CLKA↑ and CLKB↑ for ORA, ORB, IRA, and IRB	7.5	—	ns
t_{SKEW2}(2,3)	Skew Time, between CLKA↑ and CLKB↑ for $\overline{AEA}$, $\overline{AEB}$, $\overline{AFA}$, and $\overline{AFB}$	12	—	ns

NOTES:
1. Requirement to count the clock edge as one of at least four needed to reset a FIFO.
2. Skew time is not a timing constraint for proper device operation and is only included to illustrate the timing relationship between CLKA cycle and CLKB cycle.
3. Design simulated, not tested.

SWITCHING CHARACTERISTICS OVER RECOMMENDED RANGES OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE, CL = 30 PF

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Commercial IDT723622L15 IDT723632L15 IDT723642L15 Min.	Commercial IDT723622L15 IDT723632L15 IDT723642L15 Max.	Unit
t_A	Access Time, CLKA↑ to A0-A35 and CLKB↑ to B0-B35	2	10	ns
t_{PIR}	Propagation Delay Time, CLKA↑ to IRA and CLKB↑ to IRB	2	8	ns
t_{POR}	Propagation Delay Time, CLKA↑ to ORA and CLKB↑ to ORB	1	8	ns
t_{PAE}	Propagation Delay Time, CLKA↑ to $\overline{AEA}$ and CLKB↑ to $\overline{AEB}$	1	8	ns
t_{PAF}	Propagation Delay Time, CLKA↑ to $\overline{AFA}$ and CLKB↑ to $\overline{AFB}$	1	8	ns
t_{PMF}	Propagation Delay Time, CLKA↑ to $\overline{MBF1}$ LOW or $\overline{MBF2}$ HIGH and CLKB↑ to $\overline{MBF2}$ LOW or $\overline{MBF1}$ HIGH	0	8	ns
t_{PMR}	Propagation Delay Time, CLKA↑ to B0-B35[1] and CLKB↑ to A0-A35[2]	2	10	ns
t_{MDV}	Propagation Delay Time, MBA to A0-A35 valid and MBB to B0-B35 Valid	2	10	ns
t_{RSF}	Propagation Delay Time, $\overline{RST1}$ LOW to $\overline{AEB}$ LOW, $\overline{AFA}$ HIGH, and $\overline{MBF1}$ HIGH, and $\overline{RST2}$ LOW to $\overline{AEA}$ LOW, $\overline{AFB}$ HIGH, and $\overline{MBF2}$ HIGH	1	15	ns
t_{EN}	Enable Time, $\overline{CSA}$ and W/$\overline{R}$A LOW to A0-A35 Active and $\overline{CSB}$ LOW and $\overline{W}$/RB HIGH to B0-B35 Active	2	10	ns
t_{DIS}	Disable Time, $\overline{CSA}$ or W/$\overline{R}$A HIGH to A0-A35 at high-impedance and $\overline{CSB}$ HIGH or $\overline{W}$/RB LOW to B0-B35 at high-impedance	1	8	ns

NOTES:
1. Writing data to the mail1 register when the B0-B35 outputs are active and MBB is HIGH.
2. Writing data to the mail2 register when the A0-A35 outputs are active and MBA is HIGH.

SIGNAL DESCRIPTION

RESET

After power up, a Master Reset operation must be performed by providing a LOW pulse to $\overline{RST1}$ and $\overline{RST2}$ simultaneously. Afterwards, the FIFO memories of the IDT723622/723632/723642 are reset separately by taking their Reset ($\overline{RST1}$, $\overline{RST2}$) inputs LOW for at least four port A Clock (CLKA) and four port B Clock (CLKB) LOW-to-HIGH transitions. The Reset inputs can switch asynchronously to the clocks. A FIFO reset initializes the internal read and write pointers and forces the Input Ready flag (IRA, IRB) LOW, the Output Ready flag (ORA, ORB) LOW, the Almost-Empty flag ($\overline{AEA}$, $\overline{AEB}$) LOW, and the Almost-Full flag ($\overline{AFA}$, $\overline{AFB}$) HIGH. Resetting a FIFO also forces the Mailbox Flag ($\overline{MBF1}$, $\overline{MBF2}$) of the parallel mailbox register HIGH. After a FIFO is reset, its Input Ready flag is set HIGH after two clock cycles to begin normal operation.

A LOW-to-HIGH transition on a FIFO Reset ($\overline{RST1}$, $\overline{RST2}$) input latches the value of the Flag Select (FS0, FS1) inputs for choosing the Almost-Full and Almost-Empty offset programming method (for details see Table 1, *Flag Programming* and the *Almost-Empty Flag and Almost-Full Flag Offset Programming* section that follows). The relevant FIFO Reset timing diagram can be found in Figure 2.

ALMOST-EMPTY FLAG AND ALMOST-FULL FLAG OFFSET PROGRAMMING

Four registers in these devices are used to hold the offset values for the Almost-Empty and Almost-Full flags. The port B Almost-Empty flag ($\overline{AEB}$) Offset register is labeled X1 and the port A Almost-Empty flag ($\overline{AEA}$) Offset register is labeled X2. The port A Almost-Full flag ($\overline{AFA}$) Offset register is labeled Y1 and the port B Almost-Full flag ($\overline{AFB}$) Offset register is labeled Y2. The index of each register name corresponds to its FIFO number. The offset registers can be loaded with preset values during the reset of a FIFO or they can be programmed from port A (see Table 1).

— PRESET VALUES

To load the FIFO's Almost-Empty flag and Almost-Full flag Offset registers with one of the three preset values listed in Table 1, at least one of the flag select inputs must be HIGH during the LOW-to-HIGH transition of its Reset input. For example, to load the preset value of 64 into X1 and Y1, FS0 and FS1 must be HIGH when FIFO1 Reset ($\overline{RST1}$) returns HIGH. Flag offset registers associated with FIFO2 are loaded with one of the preset values in the same way with FIFO2 Reset ($\overline{RST2}$) toggled simultaneously with FIFO1 Reset ($\overline{RST1}$). For preset value loading timing diagram, see Figure 2.

— PARALLEL LOAD FROM PORT A

To program the X1, X2, Y1, and Y2 registers from port A, both FIFOs should be reset simultaneously with FS0 and FS1 LOW during the LOW-to-HIGH transition of the Reset inputs. After this reset is complete, the first four writes to FIFO1 do not store data in the FIFO memory but load the offset registers in the order Y1, X1, Y2, X2. The port A data inputs used by the offset registers are (A7-A0), (A8-A0), or (A9-A0) for the IDT723622, IDT723632, or IDT723642, respectively. The highest numbered input is used as the most significant bit of the binary number in each case. Valid programming values for the registers ranges from 1 to 252 for the IDT723622; 1 to 508 for the IDT723632; and 1 to 1,020 for the IDT723642. After all the offset registers are programmed from port A, the port B Input Ready flag (IRB) is set HIGH, and both FIFOs begin normal operation. See Figure 3 for relevant offset register parallel programming timing diagram.

FIFO WRITE/READ OPERATION

The state of the port A data (A0-A35) outputs is controlled by port A Chip Select ($\overline{CSA}$) and port A Write/Read select (W/$\overline{RA}$). The A0-A35 outputs are in the high-impedance state when either $\overline{CSA}$ or W/$\overline{RA}$ is HIGH. The A0-A35 outputs are active when both $\overline{CSA}$ and W/$\overline{RA}$ are LOW.

Data is loaded into FIFO1 from the A0-A35 inputs on a LOW-to-HIGH transition of CLKA when $\overline{CSA}$ is LOW, W/$\overline{RA}$ is HIGH, ENA is HIGH , MBA is LOW, and IRA is HIGH. Data is read from FIFO2 to the A0-A35 outputs by a LOW-to-HIGH transition of CLKA when $\overline{CSA}$ is LOW, W/$\overline{RA}$ is LOW, ENA is HIGH, MBA is LOW, and ORA is HIGH (see Table 2). FIFO reads and writes on port A are independent of any concurrent port B operation. Write and Read cycle timing diagrams for port A can be found in Figure 4 and 7.

The port B control signals are identical to those of port A with the exception that the port B Write/Read select ($\overline{W}$/RB) is the inverse of the port A Write/Read select (W/$\overline{RA}$). The state of the port B data (B0-B35) outputs is controlled by the port B Chip Select ($\overline{CSB}$) and port B Write/Read select ($\overline{W}$/RB). The B0-B35 outputs are in the high-impedance state when either $\overline{CSB}$ is HIGH or $\overline{W}$/RB is LOW. The B0-B35 outputs are active when $\overline{CSB}$ is LOW and $\overline{W}$/RB is HIGH.

Data is loaded into FIFO2 from the B0-B35 inputs on a LOW-to-HIGH transition of CLKB when $\overline{CSB}$ is LOW, $\overline{W}$/RB is LOW, ENB is HIGH, MBB is LOW, and IRB is HIGH. Data is read from FIFO1 to the B0-B35 outputs by a LOW-to-HIGH transition of CLKB when $\overline{CSB}$ is LOW, $\overline{W}$/RB is HIGH, ENB is HIGH, MBB is LOW, and ORB is HIGH (see Table 3) . FIFO reads and writes on port B are independent of any concurrent port A operation. Write and Read cycle

TABLE 1 — FLAG PROGRAMMING

FS1	FS0	$\overline{RST1}$	$\overline{RST2}$	X1 AND Y1 REGISTERS(1)	X2 AND Y2 REGISTERS(2)
H	H	↑	X	64	X
H	H	X	↑	X	64
H	L	↑	X	16	X
H	L	X	↑	X	16
L	H	↑	X	8	X
L	H	X	↑	X	8
L	L	↑	↑	Programmed from port A	Programmed from port A

NOTES:
1. X1 register holds the offset for $\overline{AEB}$; Y1 register holds the offset for $\overline{AFA}$.
2. X2 register holds the offset for $\overline{AEA}$; Y2 register holds the offset for $\overline{AFB}$.

timing diagrams for port B can be found in Figure 5 and 6.

The setup and hold time constraints to the port Clocks for the port Chip Selects and Write/Read selects are only for enabling write and read operations and are not related to high-impedance control of the data outputs. If a port enable is LOW during a clock cycle, the port's Chip Select and Write/Read select may change states during the setup and hold time window of the cycle.

When a FIFO Output Ready flag is LOW, the next word written is automatically sent to the FIFO output register automatically by the LOW-to-HIGH transition of the port clock that sets the Output Ready flag HIGH. When the Output Ready flag is HIGH, subsequent data is clocked to the output registers only when a FIFO read is selected using the port's Chip Select, Write/Read select, Enable, and Mailbox select.

SYNCHRONIZED FIFO FLAGS

Each FIFO is synchronized to its port clock through at least two flip-flop stages. This is done to improve flag-signal reliability by reducing the probability of metastable events when CLKA and CLKB operate asynchronously to one another. ORA, $\overline{AEA}$, IRA, and $\overline{AFA}$ are synchronized to CLKA. ORB, $\overline{AEB}$, IRB, and $\overline{AFB}$ are synchronized to CLKB. Tables 4 and 5 show the relationship of each port flag to FIFO1 and FIFO2.

OUTPUT READY FLAGS (ORA, ORB)

The Output Ready flag of a FIFO is synchronized to the port clock that reads data from its array. When the Output Ready flag is HIGH, new data is present in the FIFO output register. When the Output Ready flag is LOW, the previous data word is present in the FIFO output register and attempted FIFO reads are ignored.

A FIFO read pointer is incremented each time a new word is clocked to its output register. The state machine that controls an Output Ready flag monitors a write pointer and read pointer comparator that indicates when the FIFO memory status is empty, empty+1, or empty+2. From the time a word is written to a FIFO, it can be shifted to the FIFO output register in a minimum of three cycles of the Output Ready flag synchronizing clock. Therefore, an Output Ready flag is LOW if a word in memory is the next data to be sent to the FIFO output register and three cycles of the port Clock that reads data from the FIFO have not elapsed since the time the word was written. The Output Ready flag of the FIFO remains LOW until the third LOW-to-HIGH transition of the synchronizing clock occurs, simultaneously forcing the Output Ready flag HIGH and shifting the word to the FIFO output register.

A LOW-to-HIGH transition on an Output Ready flag synchronizing clock begins the first synchronization cycle of a write if the clock transition occurs at time t_{SKEW1} or greater after the write. Otherwise, the subsequent clock cycle can be the first synchronization cycle (see Figures 8 and 9 for ORA and ORB timing diagrams).

INPUT READY FLAGS (IRA, IRB)

The Input Ready flag of a FIFO is synchronized to the port clock that writes data to its array. When the Input Ready flag is HIGH, a memory location is free in the FIFO to receive new data. No memory locations are free when the Input Ready flag is LOW and attempted writes to the FIFO are ignored.

Each time a word is written to a FIFO, its write pointer is incremented. The state machine that controls an Input Ready flag monitors a write pointer and read

TABLE 2 — PORT A ENABLE FUNCTION TABLE

$\overline{CSA}$	W/$\overline{R}$A	ENA	MBA	CLKA	Data A (A0-A35) I/O	PORT FUNCTION
H	X	X	X	X	High-Impedance	None
L	H	L	X	X	Input	None
L	H	H	L	↑	Input	FIFO1 write
L	H	H	H	↑	Input	Mail1 write
L	L	L	L	X	Output	None
L	L	H	L	↑	Output	FIFO2 read
L	L	L	H	X	Output	None
L	L	H	H	↑	Output	Mail2 read (set $\overline{MBF2}$ HIGH)

TABLE 3 — PORT B ENABLE FUNCTION TABLE

$\overline{CSB}$	$\overline{W}$/RB	ENB	MBB	CLKB	Data B (B0-B35) I/O	PORT FUNCTION
H	X	X	X	X	High-Impedance	None
L	L	L	X	X	Input	None
L	L	H	L	↑	Input	FIFO2 write
L	L	H	H	↑	Input	Mail2 write
L	H	L	L	X	Output	None
L	H	H	L	↑	Output	FIFO1 read
L	H	L	H	X	Output	None
L	H	H	H	↑	Output	Mail1 read (set $\overline{MBF1}$ HIGH)

pointer comparator that indicates when the FIFO memory status is full, full-1, or full-2. From the time a word is read from a FIFO, its previous memory location is ready to be written in a minimum of two cycles of the Input Ready flag synchronizing clock. Therefore, an Input Ready flag is LOW if less than two cycles of the Input Ready flag synchronizing clock have elapsed since the next memory write location has been read. The second LOW-to-HIGH transition on the Input Ready flag synchronizing Clock after the read sets the Input Ready flag HIGH.

A LOW-to-HIGH transition on an Input Ready flag synchronizing clock begins the first synchronization cycle of a read if the clock transition occurs at time t_{SKEW1} or greater after the read. Otherwise, the subsequent clock cycle can be the first synchronization cycle (see Figures 10 and 11 for timing diagrams).

ALMOST-EMPTY FLAGS ($\overline{AEA}$, $\overline{AEB}$)

The Almost-Empty flag of a FIFO is synchronized to the port clock that reads data from its array. The state machine that controls an Almost-Empty flag monitors a write pointer and read pointer comparator that indicates when the FIFO memory status is almost-empty, almost-empty+1, or almost-empty+2. The almost-empty state is defined by the contents of register X1 for $\overline{AEB}$ and register X2 for $\overline{AEA}$. These registers are loaded with preset values during a FIFO reset or programmed from port A (see *Almost-Empty flag and Almost-Full flag offset programming* section). An Almost-Empty flag is LOW when its FIFO contains X or less words and is HIGH when its FIFO contains (X+1) or more words. A data word present in the FIFO output register has been read from memory.

Two LOW-to-HIGH transitions of the Almost-Empty flag synchronizing clock are required after a FIFO write for its Almost-Empty flag to reflect the new level of fill. Therefore, the Almost-Full flag of a FIFO containing (X+1) or more words remains LOW if two cycles of its synchronizing clock have not elapsed since the write that filled the memory to the (X+1) level. An Almost-Empty flag is set HIGH by the second LOW-to-HIGH transition of its synchronizing clock after the FIFO write that fills memory to the (X+1) level. A LOW-to-HIGH transition of an Almost-Empty flag synchronizing clock begins the first synchronization cycle if it occurs at time t_{SKEW2} or greater after the write that fills the FIFO to (X+1) words.

TABLE 4 — FIFO1 FLAG OPERATION

Number of Words in FIFO[1,2]			Synchronized to CLKB		Synchronized to CLKA	
IDT723622[3]	IDT723632[3]	IDT723642[3]	ORB	$\overline{AEB}$	$\overline{AFA}$	IRA
0	0	0	L	L	H	H
1 to X1	1 to X1	1 to X1	H	L	H	H
(X1+1) to [256-(Y1+1)]	(X1+1) to [512-(Y1+1)]	(X1+1) to [1,024-(Y1+1)]	H	H	H	H
(256-Y1) to 255	(512-Y1) to 511	(1,024-Y1) to 1,023	H	H	L	H
256	512	1,024	H	H	L	L

NOTES:
1. When a word loaded to an empty FIFO is shifted to the output register, its previous FIFO memory location is free.
2. Data in the output register does not count as a "word in FIFO memory". Since the first word written to an empty FIFO goes unrequested to the output register (no read operation necessary), it is not included in the FIFO memory count.
3. X1 is the Almost-Empty offset for FIFO1 used by $\overline{AEB}$. Y1 is the Almost-Full offset for FIFO1 used by $\overline{AFA}$. Both X1 and Y1 are selected during a reset of FIFO1 or programmed from port A.

TABLE 5 — FIFO2 FLAG OPERATION

Number of Words in FIFO[1,2]			Synchronized to CLKA		Synchronized to CLKB	
IDT723622[3]	IDT723632[3]	IDT723642[3]	ORA	$\overline{AEA}$	$\overline{AFB}$	IRB
0	0	0	L	L	H	H
1 to X2	1 to X2	1 to X2	H	L	H	H
(X2+1) to [256-(Y2+1)]	(X2+1) to [512-(Y2+1)]	(X2+1) to [1,024-(Y2+1)]	H	H	H	H
(256-Y2) to 255	(512-Y2) to 511	(1,024-Y2) to 1,023	H	H	L	H
256	512	1,024	H	H	L	L

NOTES:
1. When a word loaded to an empty FIFO is shifted to the output register, its previous FIFO memory location is free.
2. Data in the output register does not count as a "word in FIFO memory". Since the first word written to an empty FIFO goes unrequested to the output register (no read operation necessary), it is not included in the FIFO memory count.
3. X2 is the Almost-Empty offset for FIFO2 used by $\overline{AEA}$. Y2 is the Almost-Full offset for FIFO2 used by $\overline{AFB}$. Both X2 and Y2 are selected during a reset of FIFO2 or programmed from port A.

Otherwise, the subsequent synchronizing clock cycle may be the first synchronization cycle. (See Figures 12 and 13).

ALMOST-FULL FLAGS (**$\overline{AFA}$**, **$\overline{AFB}$**)

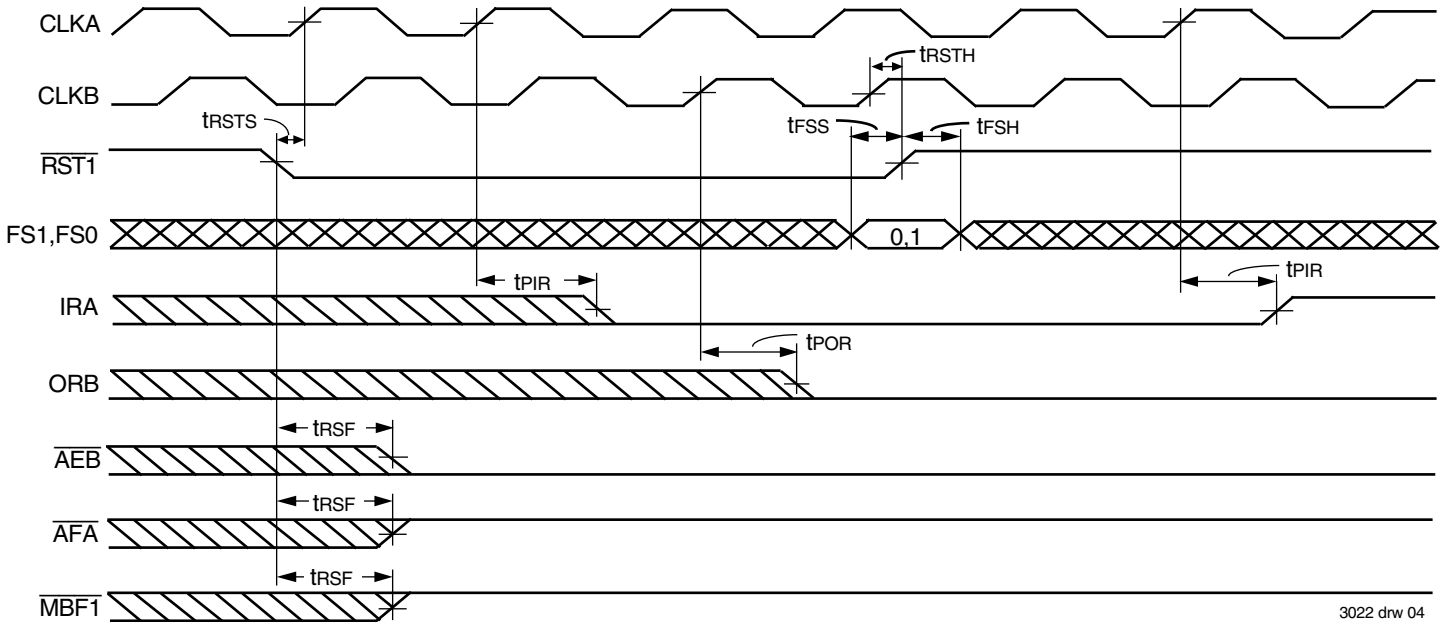
The Almost-Full flag of a FIFO is synchronized to the port clock that writes data to its array. The state machine that controls an Almost-Full flag monitors a write pointer and read pointer comparator that indicates when the FIFO memory status is almost-full, almost-full-1, or almost-full-2. The almost-full state is defined by the contents of register Y1 for $\overline{AFA}$ and register Y2 for $\overline{AFB}$. These registers are loaded with preset values during a FIFO reset or programmed from port A (see *Almost-Empty flag and Almost-Full flag offset programming* section). An Almost-Full flag is LOW when the number of words in its FIFO is greater than or equal to (256-Y), (512-Y), or (1,024-Y) for the IDT723622, IDT723632, or IDT723642 respectively. An Almost-Full flag is HIGH when the number of words in its FIFO is less than or equal to [256-(Y+1)], [512-(Y+1)], or [1,024-(Y+1)] for the IDT723622, IDT723632, or IDT723642 respectively. Note that a data word present in the FIFO output register has been read from memory.

Two LOW-to-HIGH transitions of the Almost-Full flag synchronizing clock are required after a FIFO read for its Almost-Full flag to reflect the new level of fill. Therefore, the Almost-Full flag of a FIFO containing [256/512/1,024-(Y+1)] or less words remains LOW if two cycles of its synchronizing clock have not elapsed since the read that reduced the number of words in memory to [256/512/1,024-(Y+1)]. An Almost-Full flag is set HIGH by the second LOW-to-HIGH transition of its synchronizing clock after the FIFO read that reduces the number of words in memory to [256/512/1,024-(Y+1)]. A LOW-to-HIGH transition of an Almost-Full flag synchronizing clock begins the first synchronization cycle if it occurs at time t_{SKEW2} or greater after the read that reduces the number of words in memory to [256/512/1,024-(Y+1)]. Otherwise, the subsequent synchronizing clock cycle may be the first synchronization cycle (see Figures 14 and 15).

MAILBOX REGISTERS

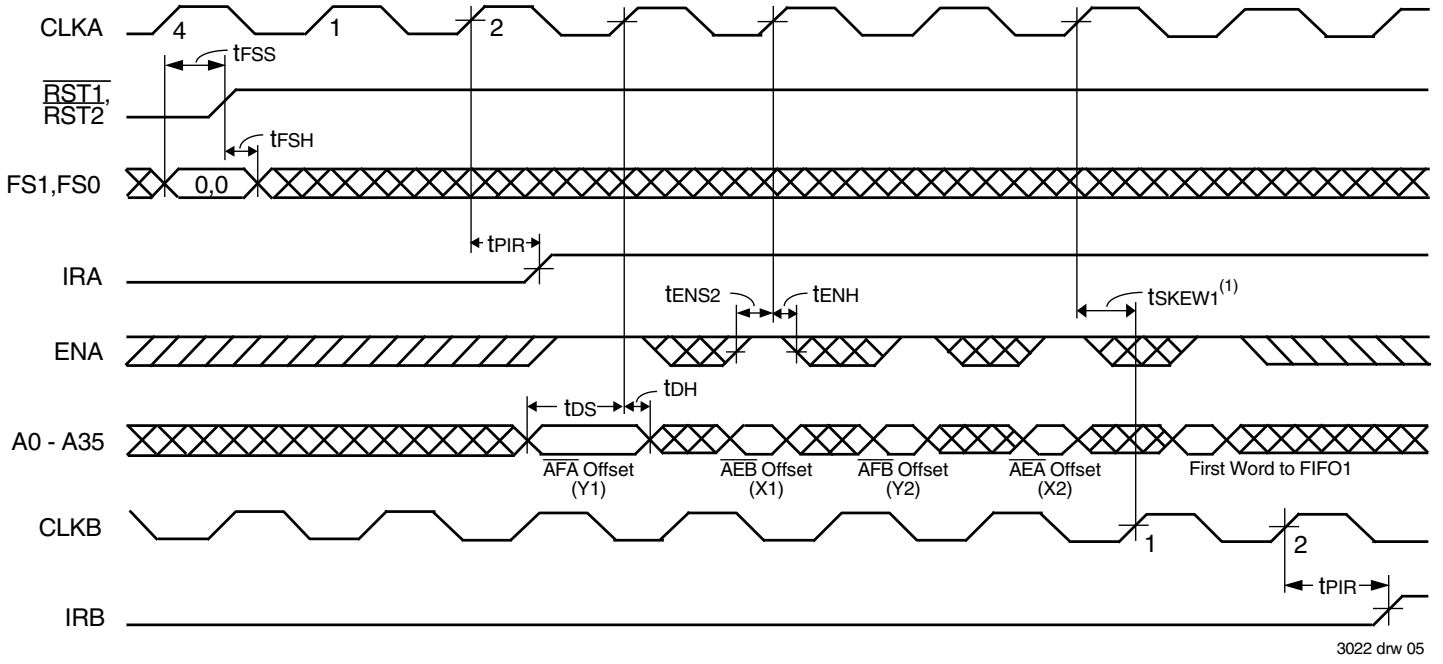
Each FIFO has a 36-bit bypass register to pass command and control information between port A and port B without putting it in queue. The Mailbox select (MBA, MBB) inputs choose between a mail register and a FIFO for a port data transfer operation. A LOW-to-HIGH transition on CLKA writes A0-A35 data to the mail1 register when a port A Write is selected by $\overline{CSA}$, W/$\overline{RA}$, and ENA and with MBA HIGH. A LOW-to-HIGH transition on CLKB writes B0-B35 data to the mail2 register when a port B Write is selected by $\overline{CSB}$, $\overline{W}$/RB, and ENB and with MBB HIGH. Writing data to a mail register sets its corresponding flag ($\overline{MBF1}$ or $\overline{MBF2}$) LOW. Attempted writes to a mail register are ignored while the mail flag is LOW.

When data outputs of a port are active, the data on the bus comes from the FIFO output register when the port Mailbox select input is LOW and from the mail register when the port-mailbox select input is HIGH. The Mail1 Register Flag ($\overline{MBF1}$) is set HIGH by a LOW-to-HIGH transition on CLKB when a port B Read is selected by $\overline{CSB}$, $\overline{W}$/RB, and ENB and with MBB HIGH. The Mail2 Register Flag ($\overline{MBF2}$) is set HIGH by a LOW-to-HIGH transition on CLKA when a port A read is selected by $\overline{CSA}$, W/$\overline{RA}$, and ENA and with MBA HIGH. The data in a mail register remains intact after it is read and changes only when new data is written to the register. For mail register and Mail Register flag timing diagrams, see Figure 16 and 17.



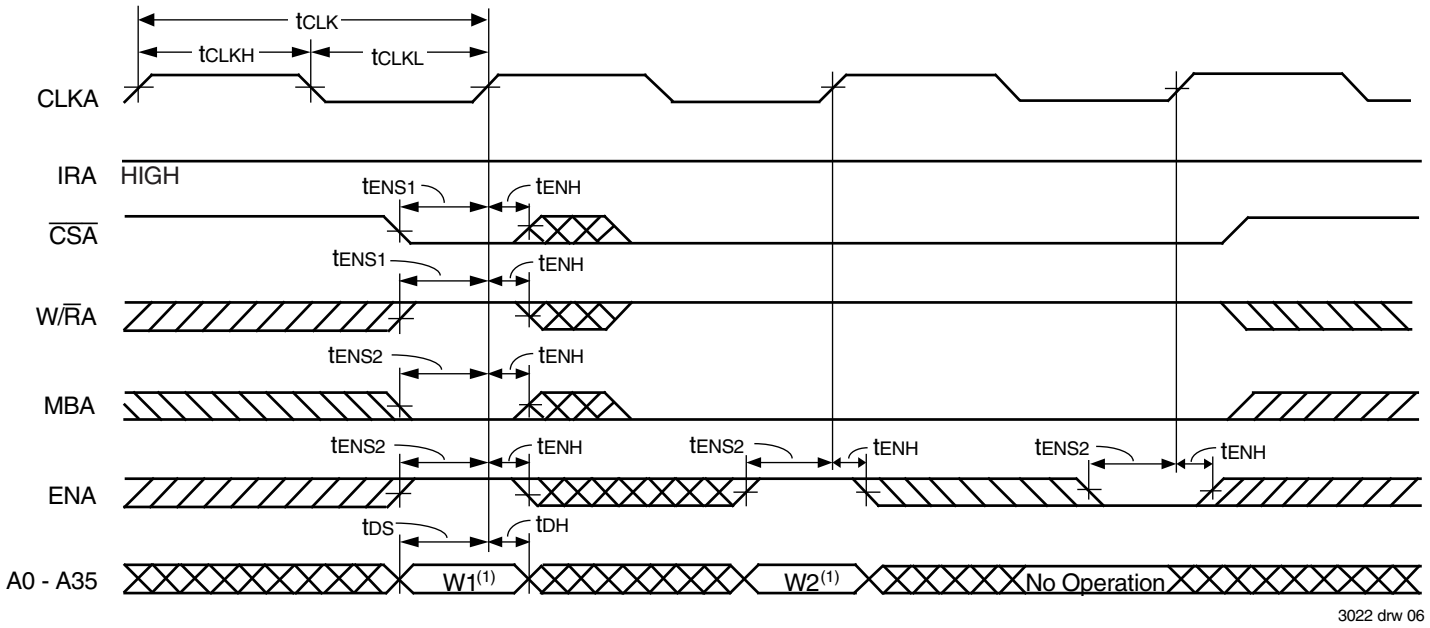
NOTE:
1. FIFO2 is reset in the same manner to load X2 and Y2 with a preset value.

Figure 2. FIFO1 Reset and Loading X1 and Y1 with a Preset Value of Eight(1)



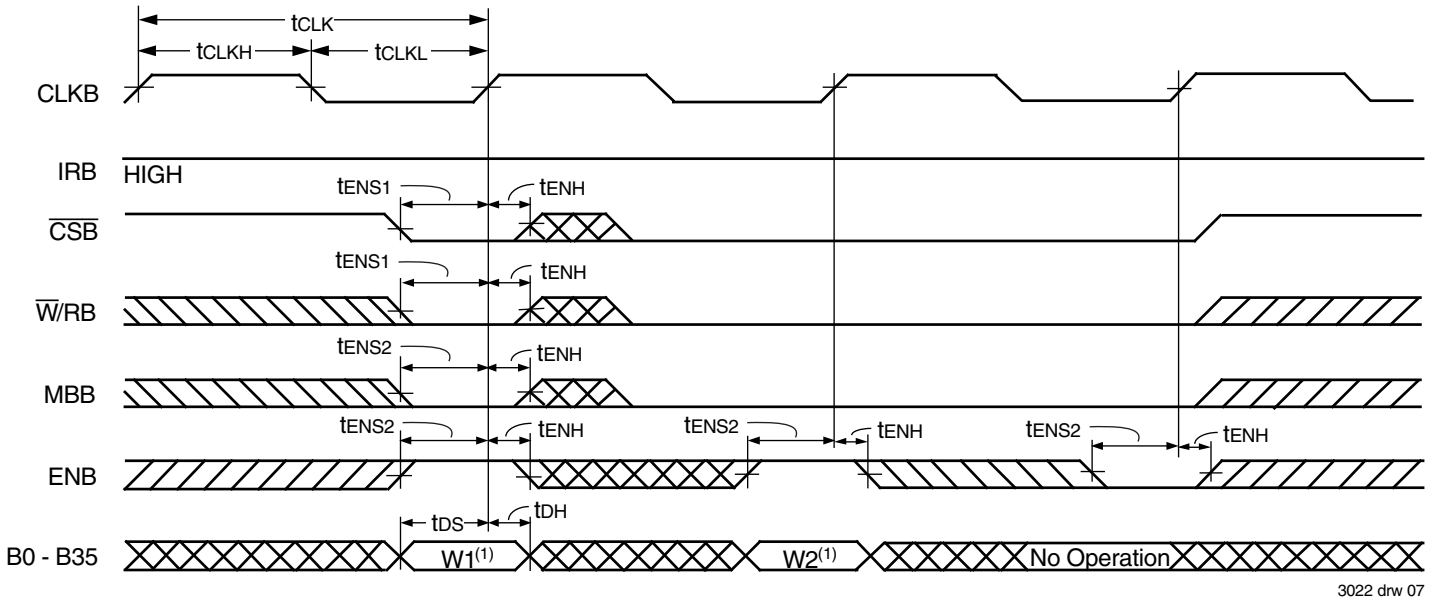
NOTES:
1. tSKEW1 is the minimum time between the rising CLKA edge and a rising CLKB edge for IRB to transition HIGH in the next cycle. If the time between the rising edge of CLKA and rising edge of CLKB is less than tSKEW1, then IRB may transition HIGH one CLKB cycle later than shown.
2. CSA = LOW, W/RA = HIGH, MBA = LOW. It is not necessary to program offset register on consecutive clock cycles.

Figure 3. Parallel Programming of the Almost-Full Flag and Almost-Empty Flag Offset Values after Reset



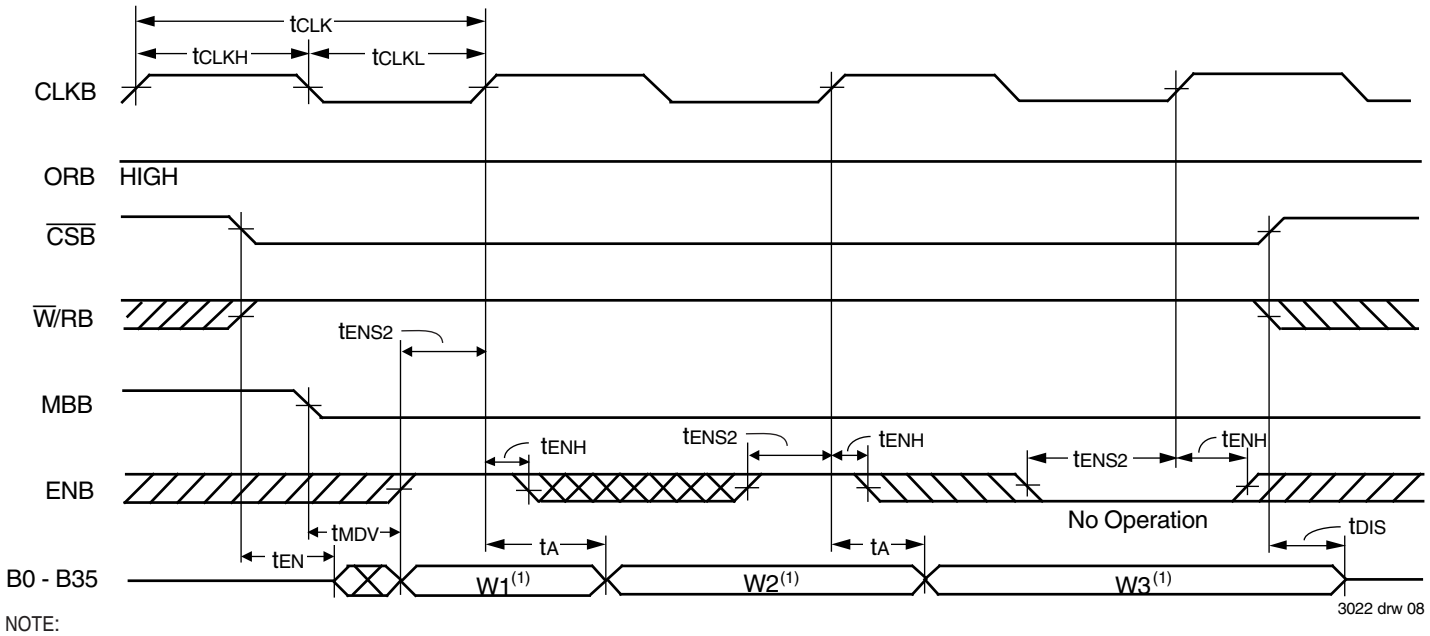
NOTE:
1. Written to FIFO1.

Figure 4. Port A Write Cycle Timing for FIFO1



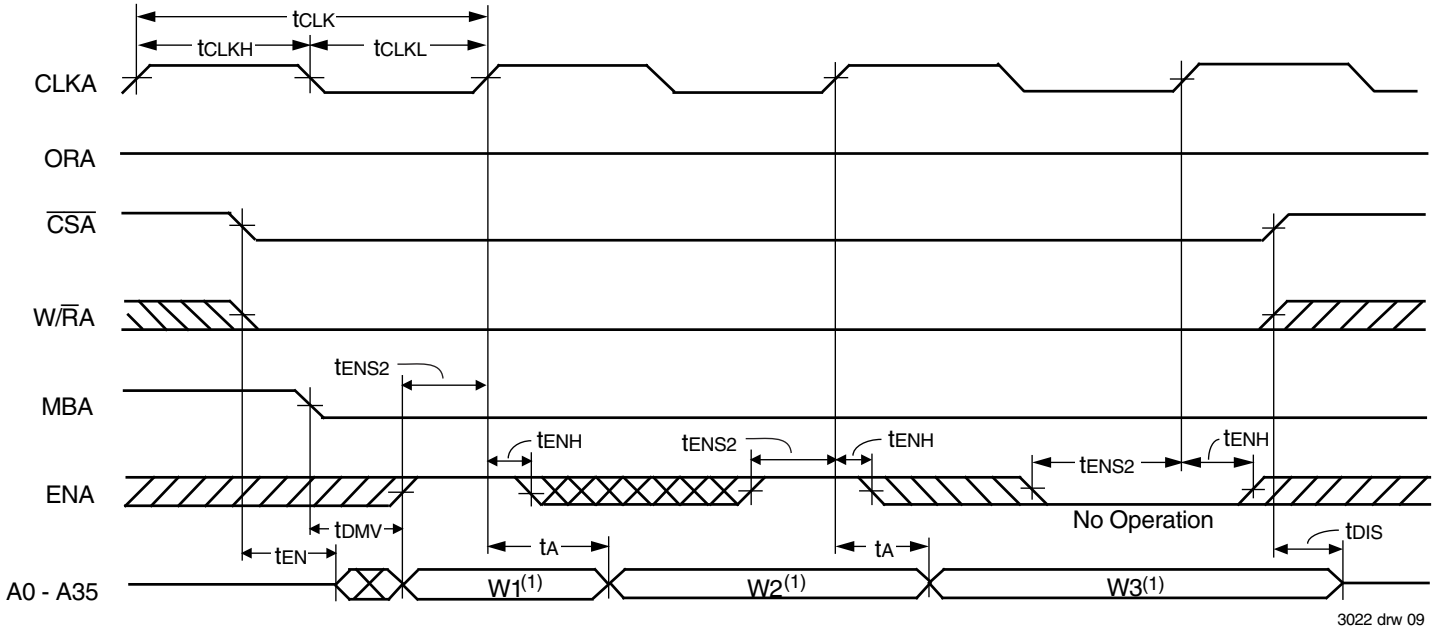
NOTE:
1. Written to FIFO2.

Figure 5. Port B Write Cycle Timing for FIFO2



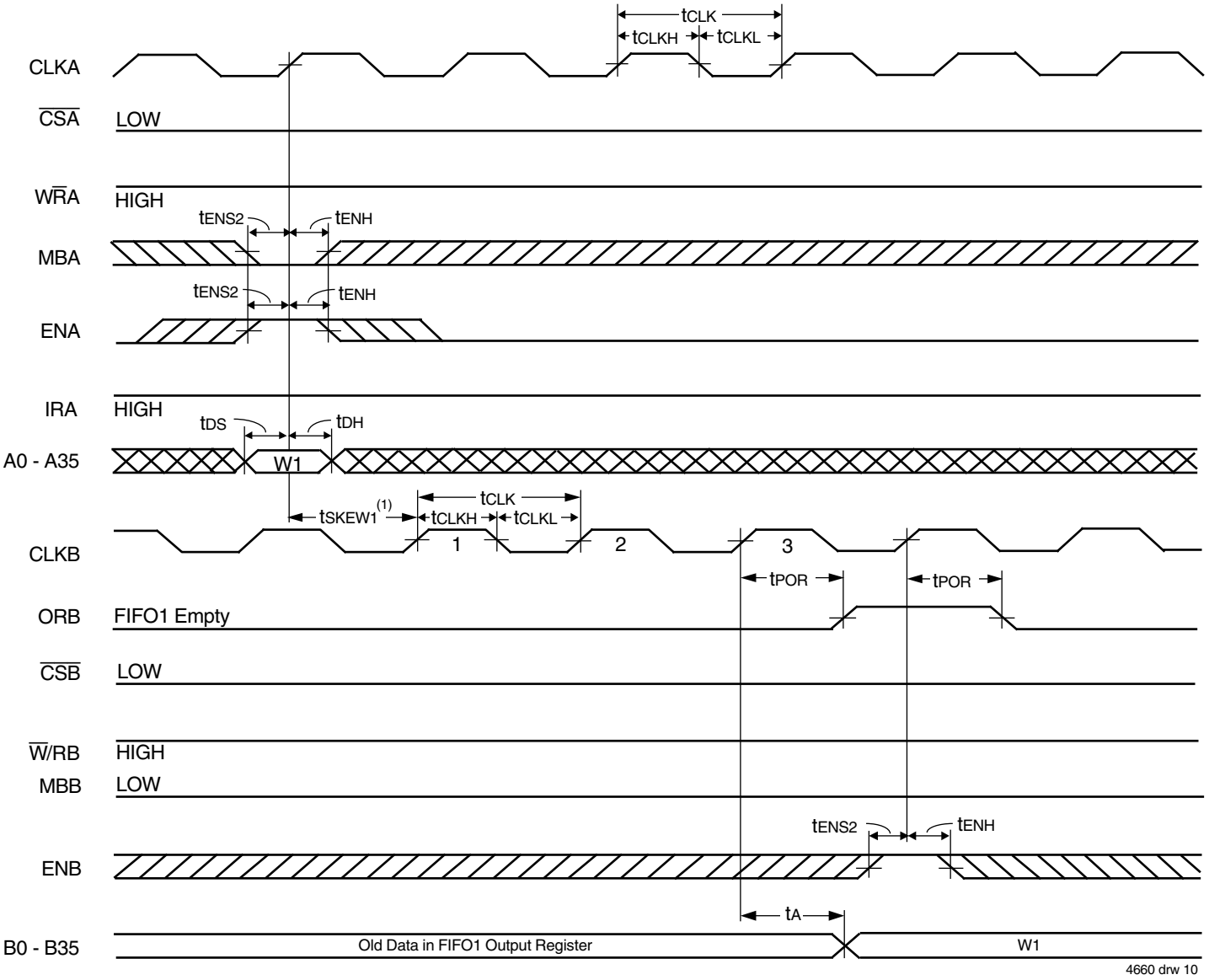
NOTE:
1. Read From FIFO1.

Figure 6. Port B Read Cycle Timing for FIFO1



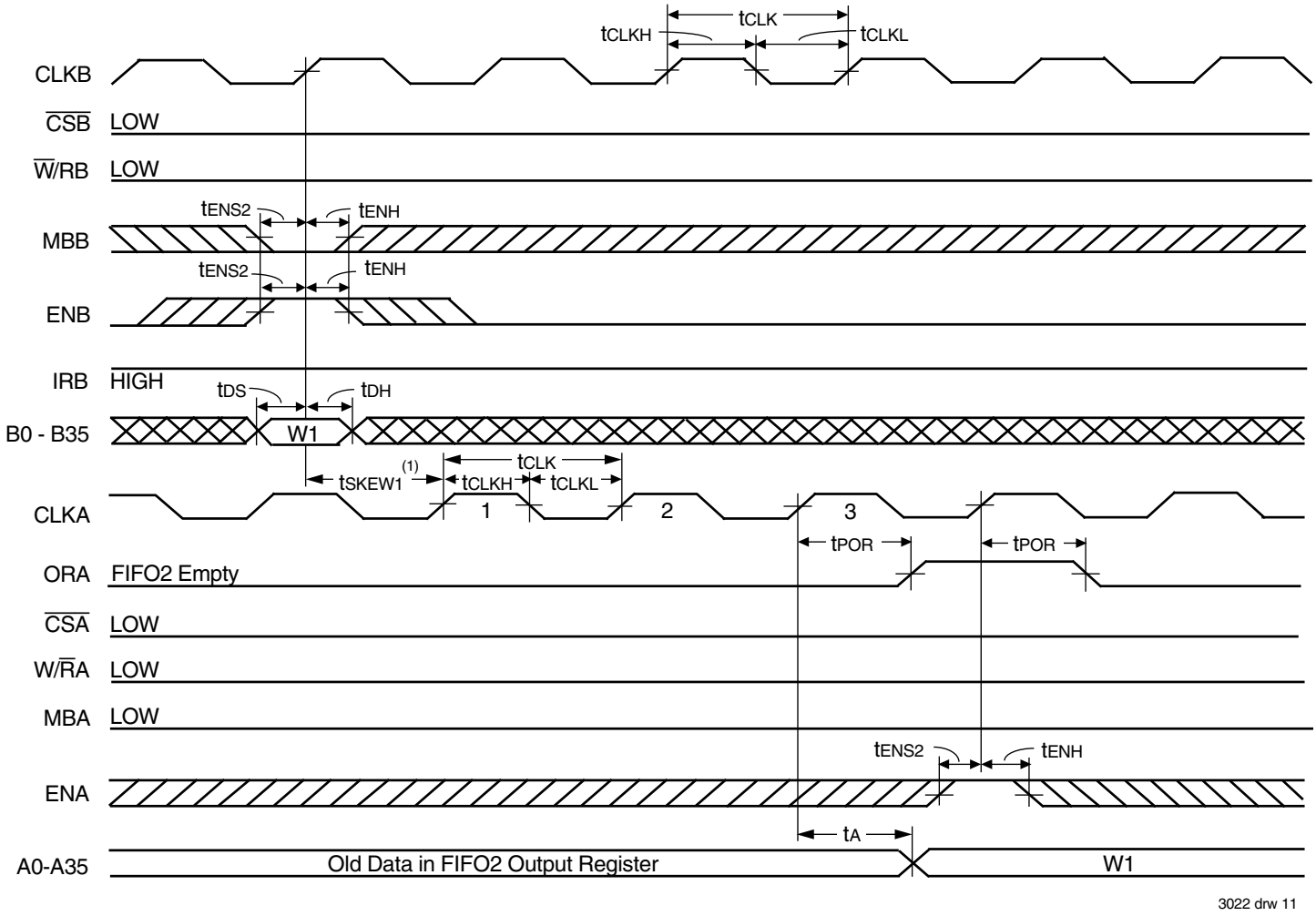
NOTE:
1. Read From FIFO2.

Figure 7. Port A Read Cycle Timing for FIFO2



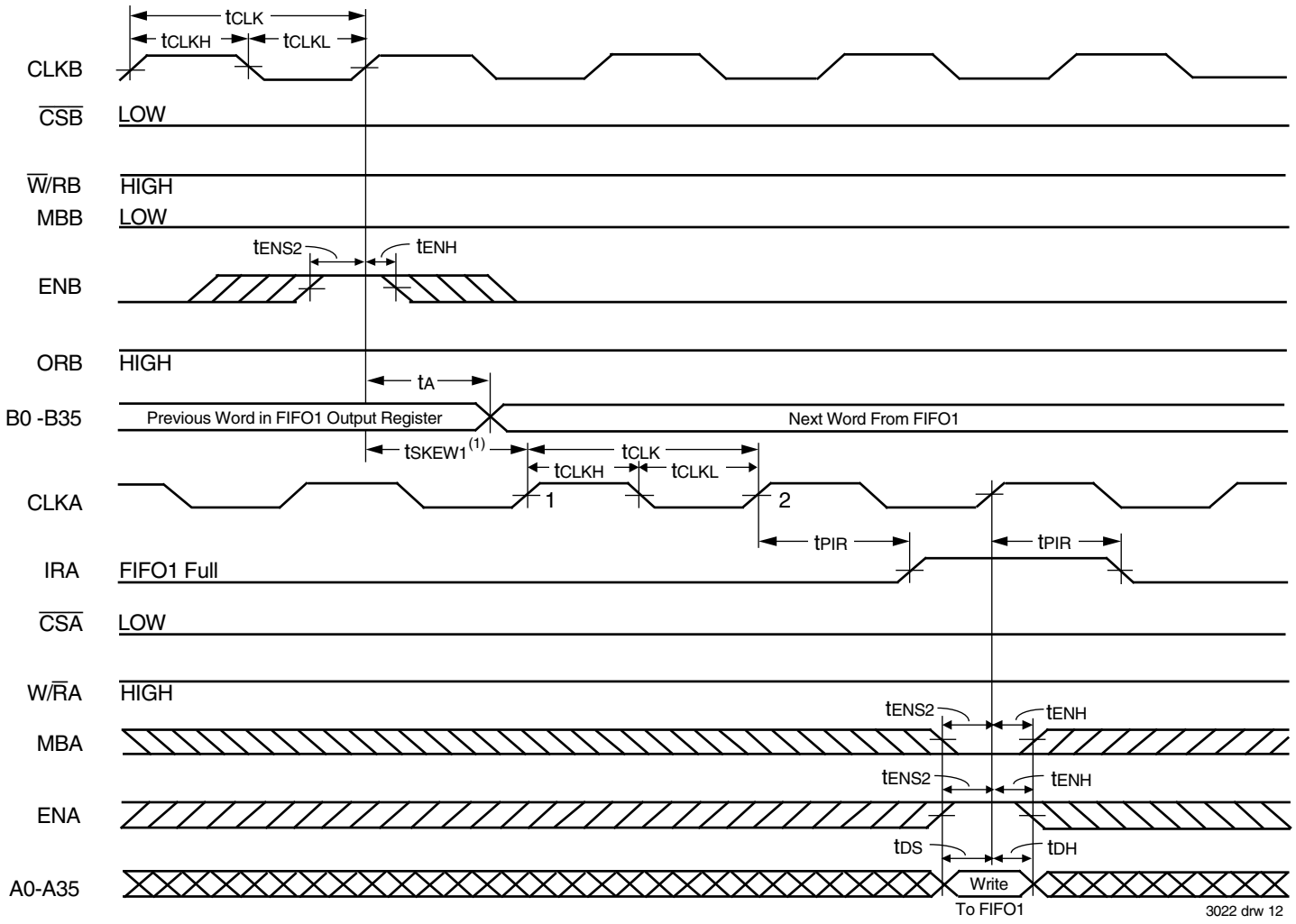
NOTE:
1. t_{SKEW1} is the minimum time between a rising CLKA edge and a rising CLKB edge for ORB to transition HIGH and to clock the next word to the FIFO1 output register in three CLKB cycles. If the time between the rising CLKA edge and rising CLKB edge is less than t_{SKEW1}, then the transition of ORB HIGH and load of the first word to the output register may occur one CLKB cycle later than shown.

Figure 8. ORB Flag Timing and First Data Word Fall Through when FIFO1 is Empty



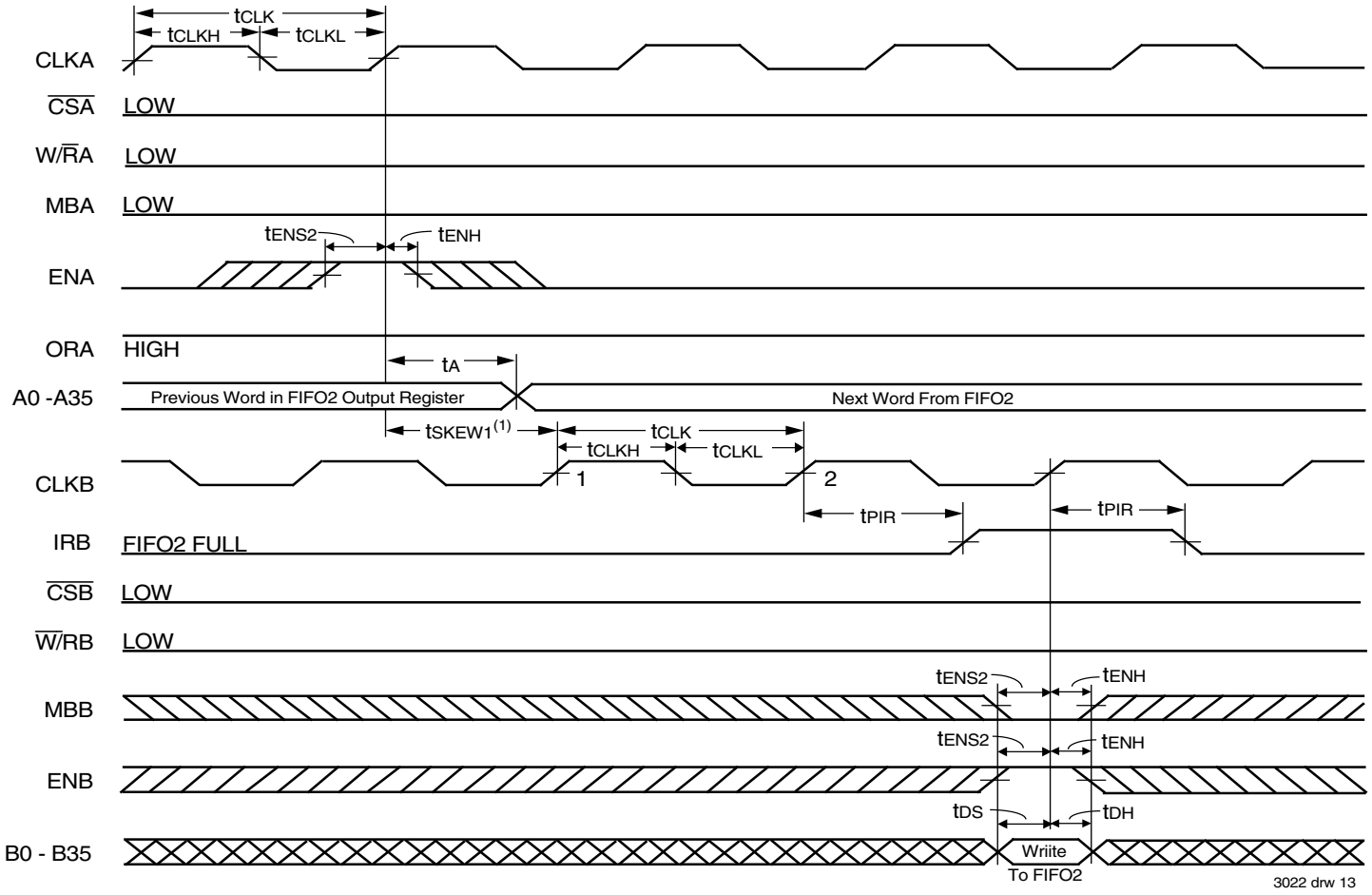
NOTE:
1. t_{SKEW1} is the minimum time between a rising CLKB edge and a rising CLKA edge for ORA to transition HIGH and to clock the next word to the FIFO2 output register in three CLKA cycles. If the time between the rising CLKB edge and rising CLKA edge is less than t_{SKEW1}, then the transition of ORA HIGH and load of the first word to the output register may occur one CLKA cycle later than shown.

Figure 9. ORA Flag Timing and First Data Word Fall Through when FIFO2 is Empty



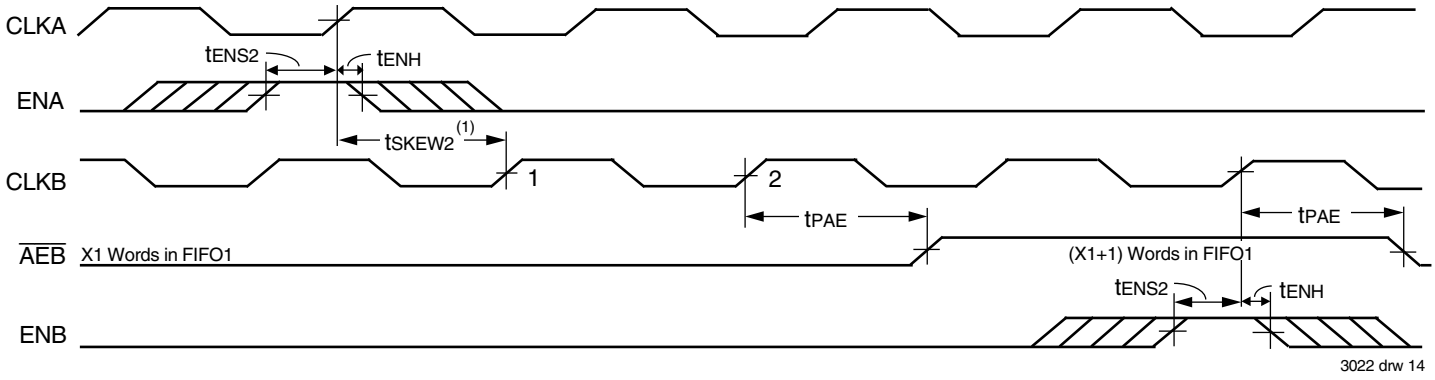
NOTE:
1. t_{SKEW1} is the minimum time between a rising CLKB edge and a rising CLKA edge for IRA to transition HIGH in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{SKEW1}, then IRA may transition HIGH one CLKA cycle later than shown.

Figure 10. IRA Flag Timing and First Available Write when FIFO1 is Full



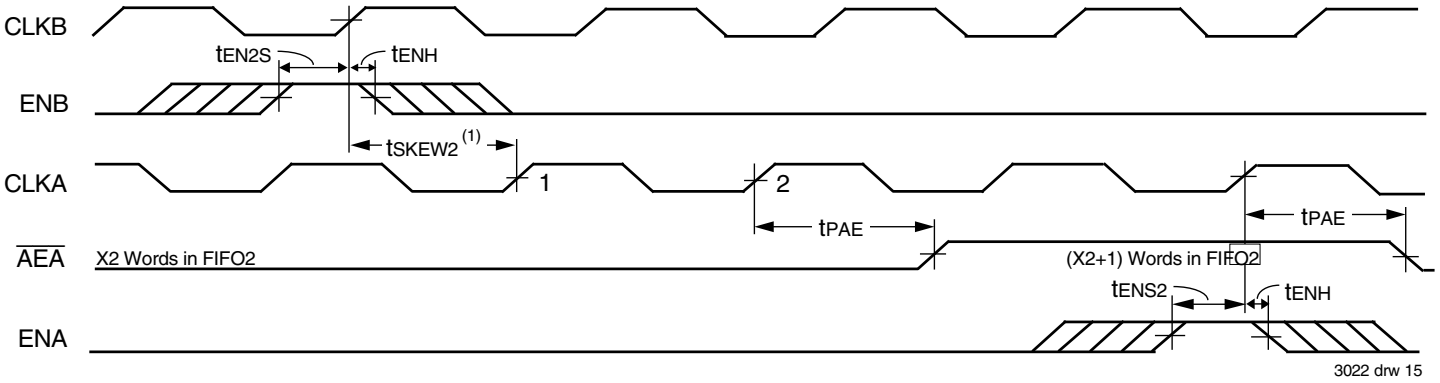
NOTE:
1. t_{SKEW1} is the minimum time between a rising CLKA edge and a rising CLKB edge for IRB to transition HIGH in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{SKEW1}, then IRB may transition HIGH one CLKB cycle later than shown.

Figure 11. IRB Flag Timing and First Available Write when FIFO2 is Full



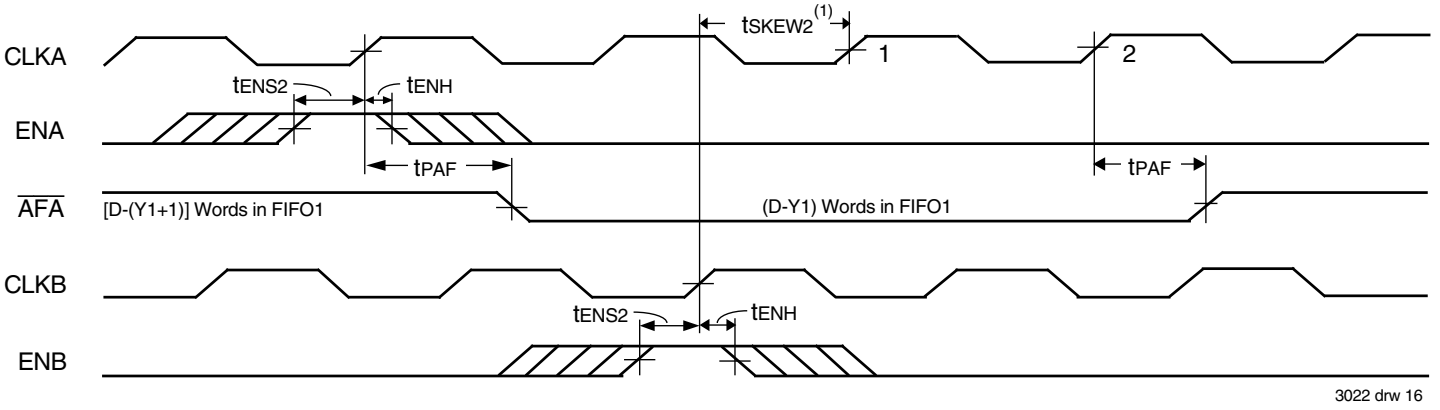
NOTES:
1. t_{SKEW2} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AEB}$ to transition HIGH in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{SKEW2}, then $\overline{AEB}$ may transition HIGH one CLKB cycle later than shown.
2. FIFO1 Write ($\overline{CSA}$ = LOW, W/$\overline{RA}$ = LOW, MBA = LOW), FIFO1 read ($\overline{CSB}$ = LOW, $\overline{W}$/RB = HIGH, MBB = LOW). Data in the FIFO1 output register has been read from the FIFO.

Figure 12. Timing for $\overline{AEB}$ when FIFO1 is Almost-Empty



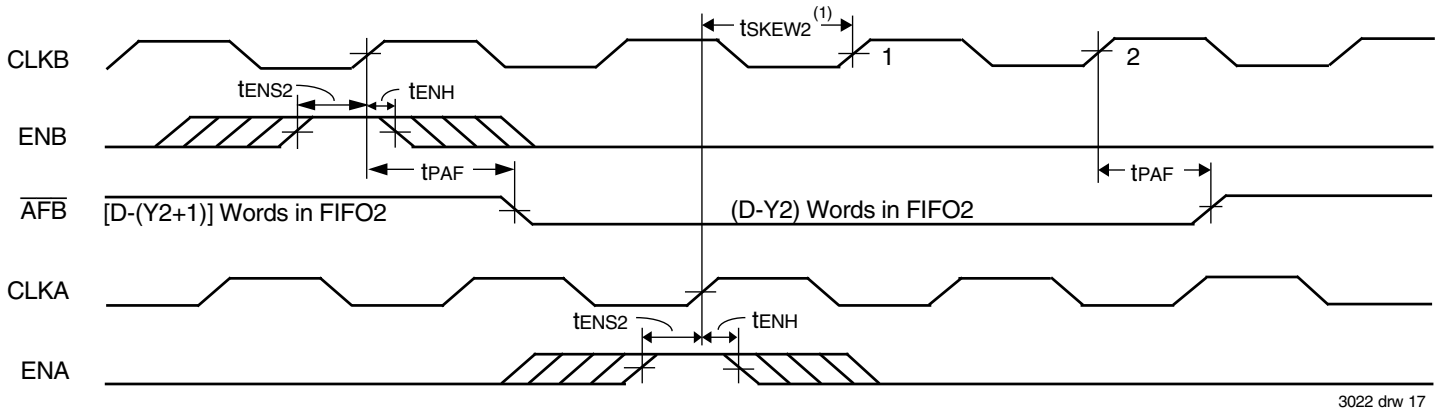
NOTES:
1. tSKEW2 is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{AEA}$ to transition HIGH in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than tSKEW2, then $\overline{AEA}$ may transition HIGH one CLKA cycle later than shown.
2. FIFO2 Write ($\overline{CSB}$ = LOW, W/$\overline{RB}$ = LOW, MBB = LOW), FIFO2 read ($\overline{CSA}$ = LOW, W/$\overline{RA}$ = LOW, MBA = LOW). Data in the FIFO2 output register has been read from the FIFO.

Figure 13. Timing for $\overline{AEA}$ when FIFO2 is Almost-Empty



NOTES:
1. tSKEW2 is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AFA}$ to transition HIGH in the next CLKA cycle. If the time between the rising CLKA edge and rising CLKB edge is less than tSKEW2, then $\overline{AFA}$ may transition HIGH one CLKA cycle later than shown.
2. FIFO1 Write ($\overline{CSA}$ = LOW, W/$\overline{RA}$ = HIGH, MBA = LOW), FIFO1 read ($\overline{CSB}$ = LOW, W/$\overline{RB}$ = HIGH, MBB = LOW). Data in the FIFO1 output register has been read from the FIFO.
3. D = Maximum FIFO Depth = 256 for the IDT723622, 512 for the IDT723632, 1,024 for the IDT723642.

Figure 14. Timing for $\overline{AFA}$ when FIFO1 is Almost-Full



NOTES:
1. tSKEW2 is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{AFB}$ to transition HIGH in the next CLKB cycle. If the time between the rising CLKB edge and rising CLKA edge is less than tSKEW2, then $\overline{AFB}$ may transition HIGH one CLKB cycle later than shown.
2. FIFO2 write ($\overline{CSB}$ = LOW, W/$\overline{RB}$ = LOW, MBB = LOW), FIFO2 read ($\overline{CSA}$ = LOW, W/$\overline{RA}$ = LOW, MBA = LOW). Data in the FIFO2 output register has been read from the FIFO.
3. D = Maximum FIFO Depth = 256 for the IDT723622, 512 for the IDT723632, 1,024 for the IDT723642.

Figure 15. Timing for $\overline{AFB}$ when FIFO2 is Almost-Full

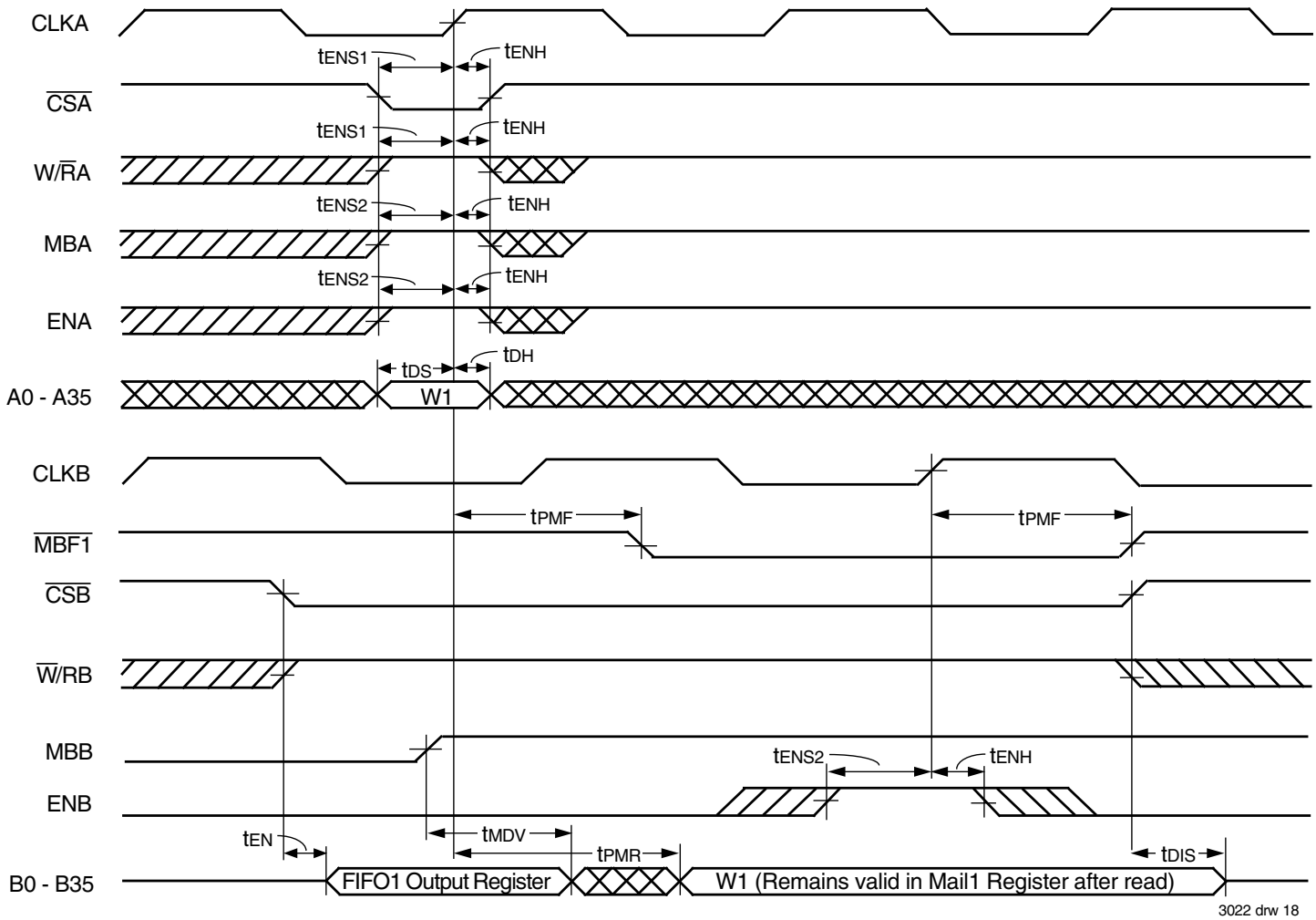


Figure 16. Timing for Mail1 Register and $\overline{MBF1}$ Flag

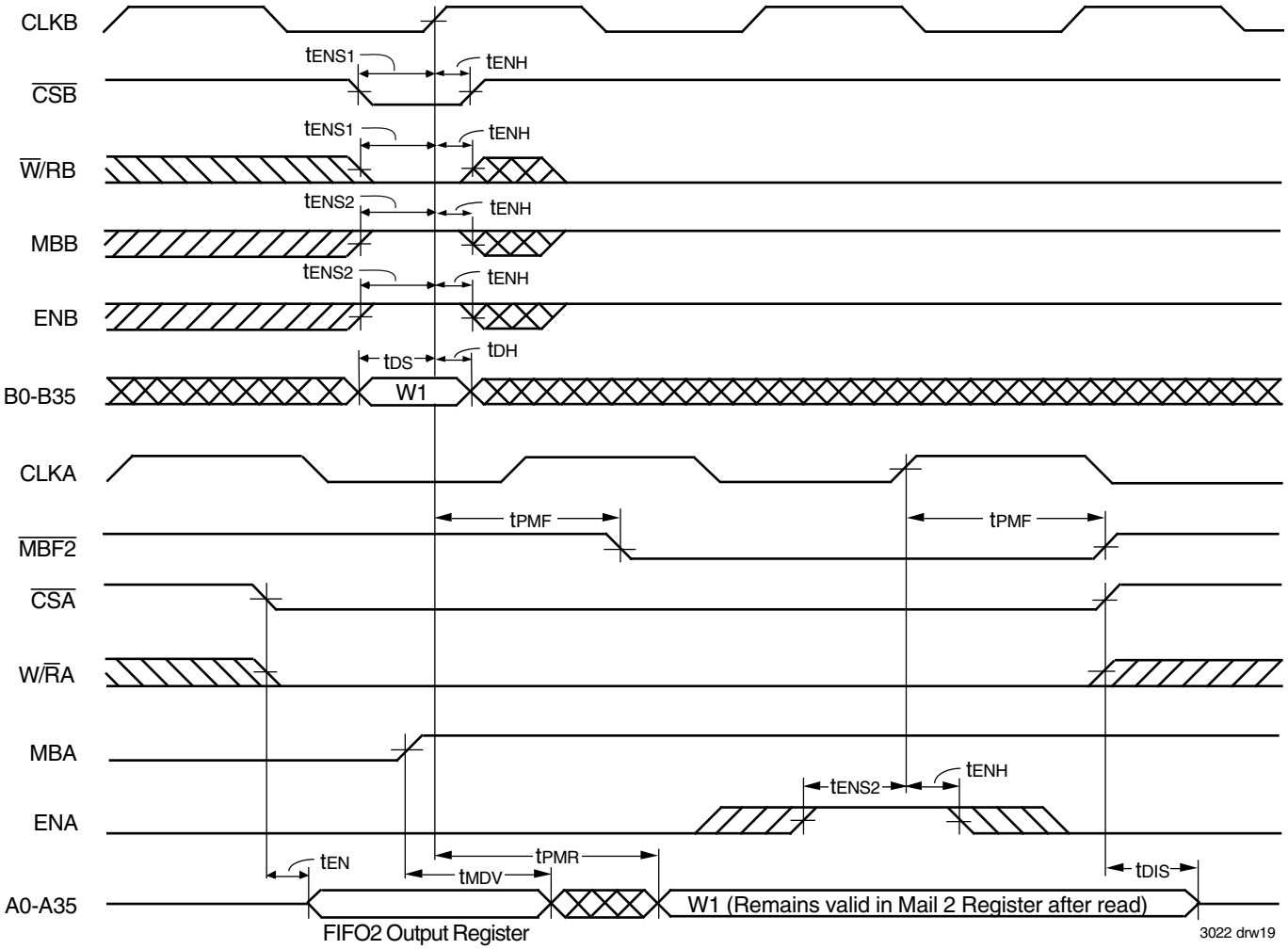
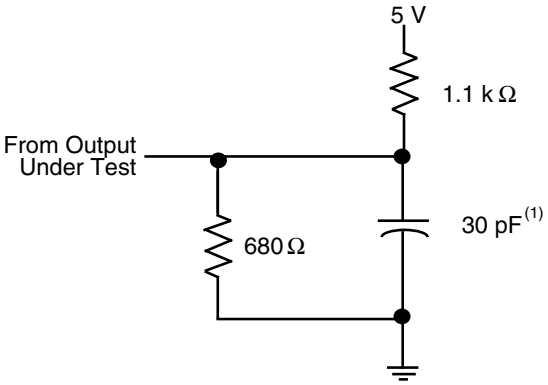
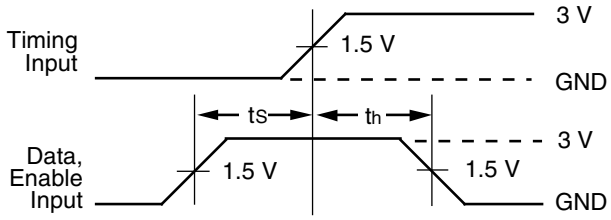


Figure 17. Timing for Mail2 Register and ***MBF2*** *Flag*

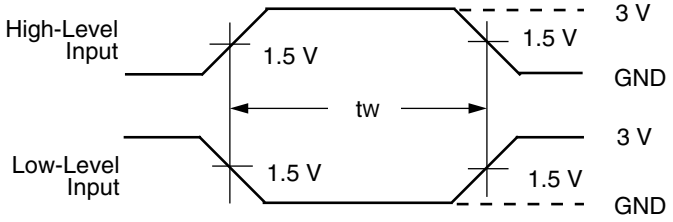
PARAMETER MEASUREMENT INFORMATION



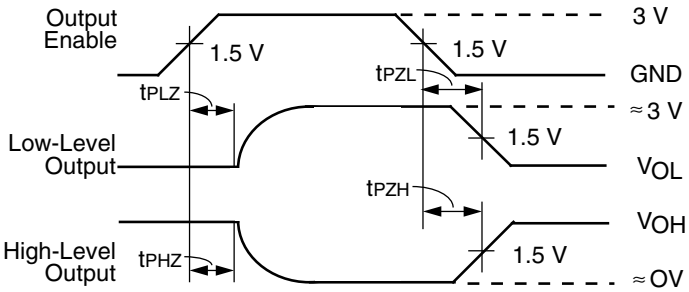
PROPAGATION DELAY LOAD CIRCUIT



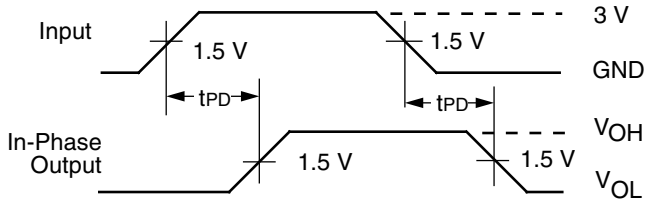
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES



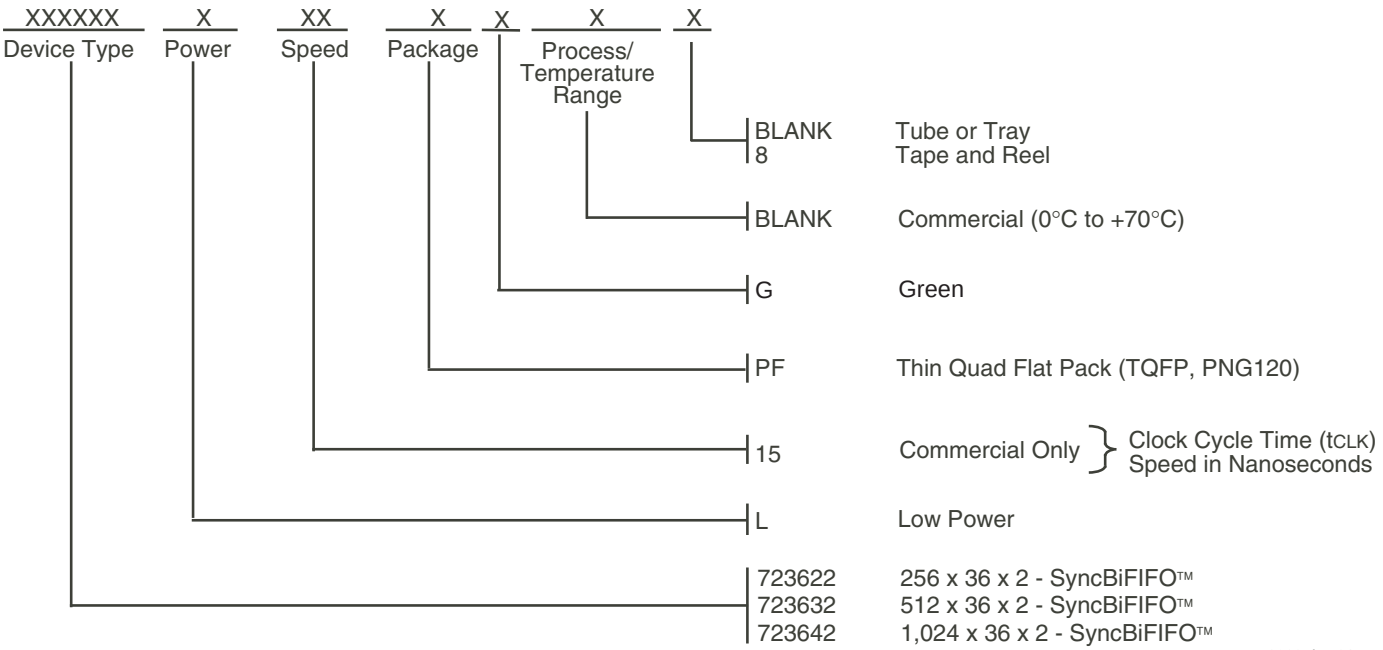
VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES

3022 drw 20

NOTE:
1. Includes probe and jig capacitance.

Figure 18. Load Circuit and Voltage Waveforms

ORDERING INFORMATION



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DATASHEET DOCUMENT HISTORY

10/04/2000	pgs.	1 through 25, except pages 35.
03/21/2001	pgs.	6 and 7.
08/01/2001	pgs.	1, 6, 8, 9 and 25.
12/18/2001	pg.	23.
02/05/2009	pgs.	1 and 25.
02/19/2015	pgs.	1, 2, 5, 7, 8, 9 and 24.

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