

FEATURES:

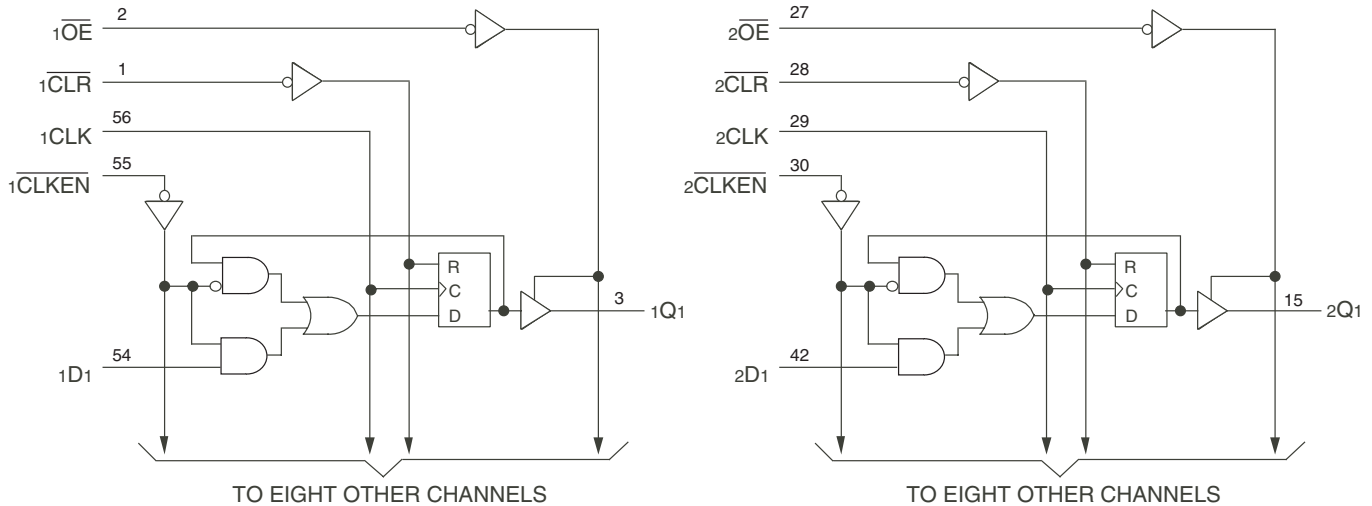
- 0.5 MICRON CMOS Technology
- High-speed, low-power CMOS replacement for ABT functions
- Typical $t_{sk(o)}$ (Output Skew) < 250ps
- Low input and output leakage $\leq 1\mu A$ (max.)
- $V_{CC} = 5V \pm 10\%$
- Balanced Output Drivers of $\pm 24mA$
- Reduced system switching noise
- Typical V_{OLP} (Output Ground Bounce) < 0.6V at $V_{CC} = 5V$, $T_A = 25^\circ C$
- Available in SSOP and TSSOP packages

DESCRIPTION:

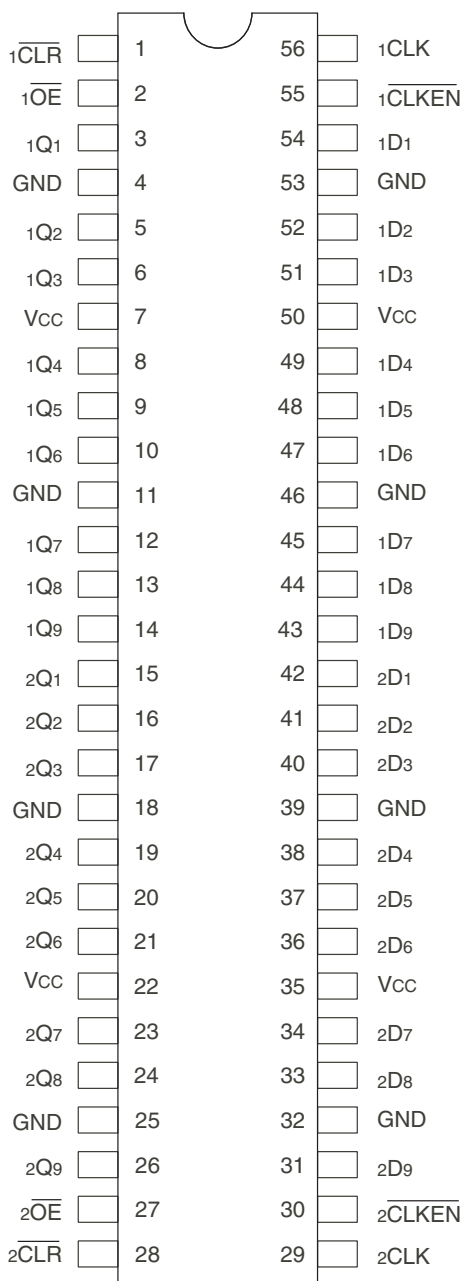
The FCT162823T 18-bit bus interface register is built using advanced, dual metal CMOS technology. These high-speed, low-power registers with clock enable (\overline{xCLKEN}) and clear (\overline{xCLR}) controls are ideal for parity bus interfacing in high-performance synchronous systems. The control inputs are organized to operate the device as two 9-bit registers or one 18-bit register. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

The FCT162823T has balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times – reducing the need for external series terminating resistors. The FCT162823T is a plug-in replacement for the FCT16823T and ABT16823T for on-board interface applications.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SSOP/ TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to 7	V
V _{TERM} ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to V _{CC} +0.5	V
T _{STG}	Storage Temperature	-65 to +150	°C
I _{OUT}	DC Output Current	-60 to +120	mA

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- All device terminals except FCT162XXX Output and I/O terminals.
- Outputs and I/O terminals for FCT162XXX.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	3.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	3.5	8	pF

NOTE:

- This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
xD _x	Data Inputs
xCLK	Clock Inputs
x $\overline{\text{CLKEN}}$	Clock Enable Inputs (Active LOW)
x $\overline{\text{CLR}}$	Asynchronous clear Inputs (Active LOW)
x $\overline{\text{OE}}$	Output Enable Inputs (ActiveLOW)
xO _x	3-State Outputs

FUNCTION TABLE⁽¹⁾

Inputs					Outputs	Function
x $\overline{\text{OE}}$	x $\overline{\text{CLR}}$	x $\overline{\text{CLKEN}}$	xCLK	xD _x	xQ _x	
H	X	X	X	X	Z	High Z
L	L	X	X	X	L	Clear
L	H	H	X	X	Q ⁽²⁾	Hold
H	H	L	↑	L	Z	Load
H	H	L	↑	H	Z	
L	H	L	↑	L	L	
L	H	L	↑	H	H	

NOTES:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-Impedance
- Output level before indicated steady-state input conditions were established.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins) ⁽⁴⁾	$V_{CC} = \text{Max.}$	$V_i = V_{CC}$	—	—	± 1	μA
	Input HIGH Current (I/O pins) ⁽⁴⁾		$V_i = \text{GND}$	—	—	± 1	
I_{IL}	Input LOW Current (Input pins) ⁽⁴⁾		$V_o = 2.7\text{V}$	—	—	± 1	
	Input LOW Current (I/O pins) ⁽⁴⁾		$V_o = 0.5\text{V}$	—	—	± 1	
I_{OZH}	High Impedance Output Current (3-State Output pins) ⁽⁴⁾	$V_{CC} = \text{Max.}$	$V_o = 2.7\text{V}$	—	—	± 1	μA
I_{OZL}			$V_o = 0.5\text{V}$	—	—	± 1	
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}, V_o = \text{GND}^{(3)}$		-80	-140	-250	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL}	Quiescent Power Supply Current	$V_{CC} = \text{Max}$		—	5	500	μA
I_{CCH}		$V_{IN} = \text{GND or } V_{CC}$					
I_{CCZ}							

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I_{ODL}	Output LOW Current	$V_{CC} = 5\text{V}, V_{IN} = V_{IH} \text{ or } V_{IL}, V_o = 1.5\text{V}^{(3)}$		60	115	200	mA
I_{ODH}	Output HIGH Current	$V_{CC} = 5\text{V}, V_{IN} = V_{IH} \text{ or } V_{IL}, V_o = 1.5\text{V}^{(3)}$		-60	-115	-200	mA
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -24\text{mA}$	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 24\text{mA}$	—	0.3	0.55	V

NOTES:

- For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0\text{V}$, $+25^{\circ}\text{C}$ ambient.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This test limit for this parameter is $\pm 5\mu\text{A}$ at $T_A = -55^{\circ}\text{C}$.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V _{CC} = Max. V _{IN} = 3.4V ⁽³⁾		—	0.5	1.5	mA
I _{CCD}	Dynamic Power Supply Current ⁽⁴⁾	V _{CC} = Max. Outputs Open $\overline{xOE} = \overline{xCLKEN} = GND$ One Input Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND	—	75	120	μA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max. Outputs Open f _{CP} = 10MHz 50% Duty Cycle $\overline{xOE} = \overline{xCLKEN} = GND$ at f _i = 5MHz 50% Duty Cycle One Bit Toggling	V _{IN} = V _{CC} V _{IN} = GND	—	0.8	1.7	mA
			V _{IN} = 3.4V V _{IN} = GND	—	1.3	3.2	
		V _{CC} = Max. Outputs Open f _{CP} = 10MHz 50% Duty Cycle $\overline{xOE} = \overline{xCLKEN} = GND$ at f _i = 2.5MHz 50% Duty Cycle Eighteen Bits Toggling	V _{IN} = V _{CC} V _{IN} = GND	—	4.2	7.1 ⁽⁵⁾	
			V _{IN} = 3.4V V _{IN} = GND	—	9.2	22.1 ⁽⁵⁾	

NOTES:

- For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP} / 2 + f_i N_i)$
 I_{CC} = Quiescent Current (I_{CC1}, I_{CC2} and I_{CC3})
 ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
 D_H = Duty Cycle for TTL Inputs High
 N_T = Number of TTL Inputs at D_H
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 N_{CP} = Number of Clock Inputs at f_{CP}
 f_i = Input Frequency
 N_i = Number of Inputs at f_i

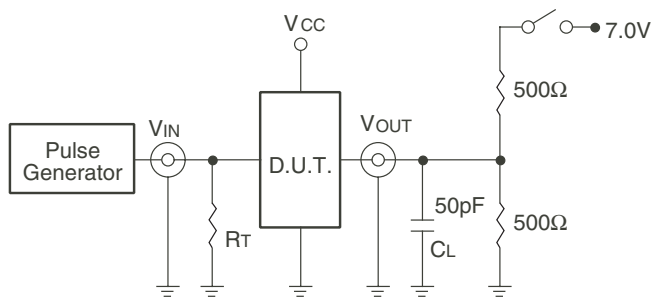
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition ⁽¹⁾	FCT162823AT		FCT162823CT		Unit
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
t _{PLH} t _{PHL}	Propagation Delay xCLKx to xOx	CL = 50pF RL = 500Ω	1.5	10	1.5	4.7	ns
		CL = 300pF ⁽⁴⁾ RL = 500Ω	1.5	20	1.5	8	
t _{PHL}	Propagation Delay x $\overline{\text{CLR}}$ to xOx	CL = 50pF RL = 500Ω	1.5	14	1.5	4.7	ns
t _{PZH} t _{PZL}	Output Enable Time x $\overline{\text{OE}}$ to xOx	CL = 50pF RL = 500Ω	1.5	12	1.5	4.4	ns
		CL = 300pF ⁽⁴⁾ RL = 500Ω	1.5	23	1.5	9	
t _{PHZ} t _{PLZ}	Output Disable Time x $\overline{\text{OE}}$ to xOx	CL = 50pF ⁽⁴⁾ RL = 500Ω	1.5	7	1.5	3.6	ns
		CL = 50pF RL = 500Ω	1.5	8	1.5	3.6	
t _{SU}	Set-up Time HIGH or LOW xDx to xCLK	CL = 50pF RL = 500Ω	3	—	1.5	—	ns
t _H	Hold Time HIGH or LOW, xDx to xCLK		1.5	—	0	—	ns
t _{SU}	Set-up Time HIGH or LOW, x $\overline{\text{CLKEN}}$ to xCLK		3	—	2.5	—	ns
t _H	Hold Time HIGH or LOW, x $\overline{\text{CLKEN}}$ to xCLK		0	—	0	—	ns
t _w	xCLK Pulse Width HIGH or LOW		6	—	3	—	ns
t _w	x $\overline{\text{CLR}}$ Pulse Width LOW		6	—	3	—	ns
t _{REM}	Recovery Time, x $\overline{\text{CLR}}$ to xCLK		6	—	3	—	ns
t _{SK(o)}	Output Skew ⁽³⁾		—	0.5	—	0.5	ns

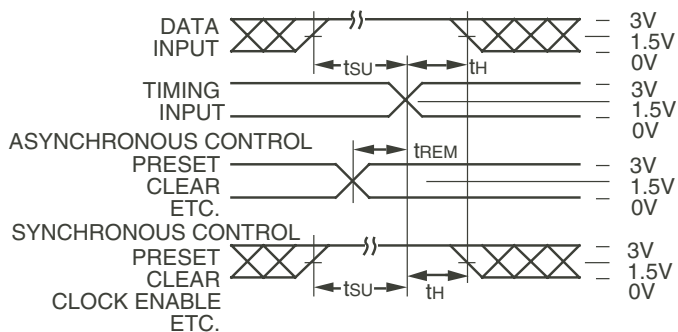
NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.
4. This condition is guaranteed but not tested.

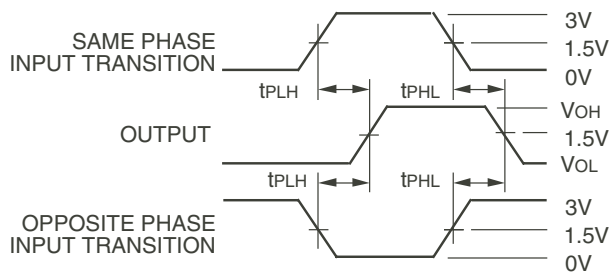
TEST CIRCUITS AND WAVEFORMS



Test Circuits for All Outputs



Set-up, Hold, and Release Times



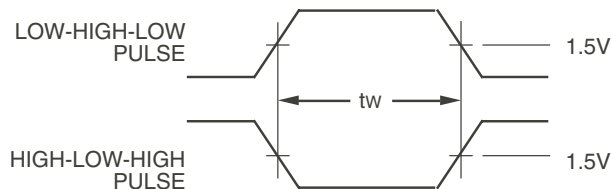
Propagation Delay

SWITCH POSITION

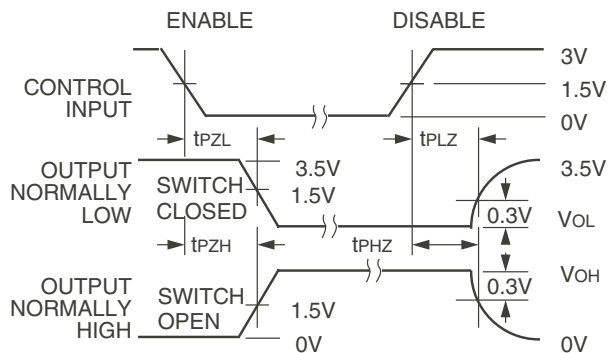
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.



Pulse Width

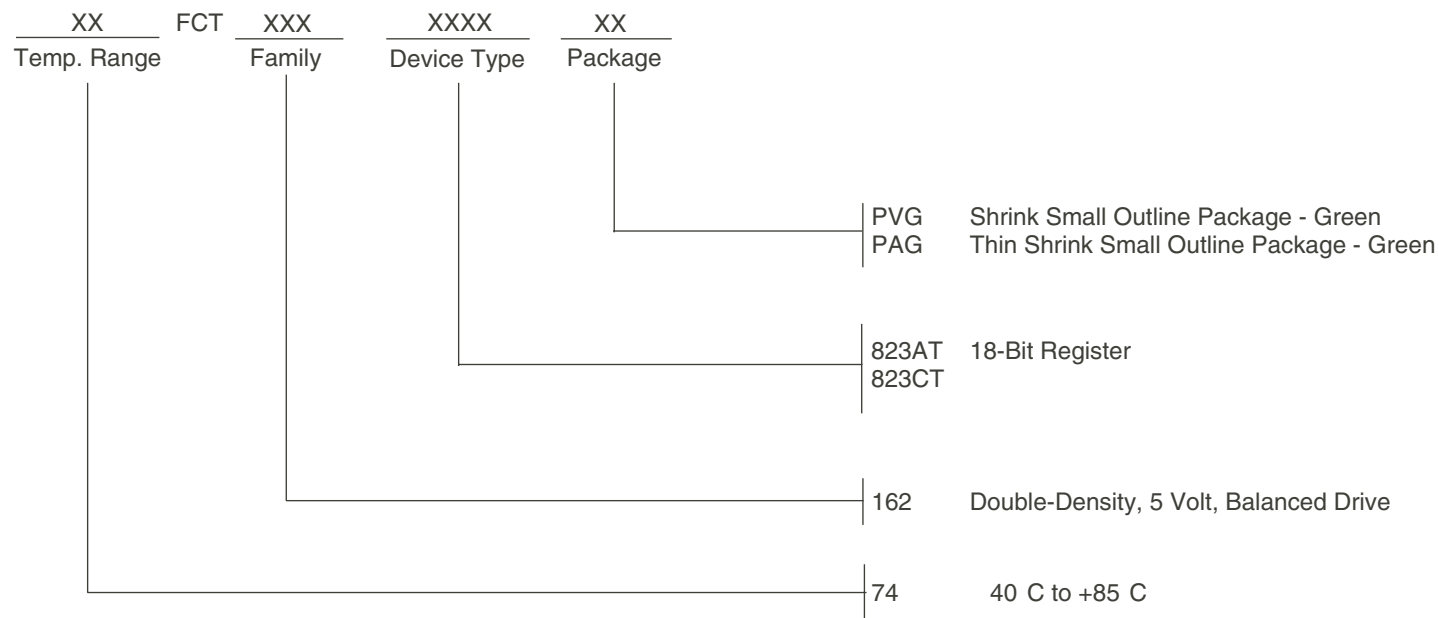


Enable and Disable Times

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate \leq 1.0MHz; $t_r \leq$ 2.5ns; $t_f \leq$ 2.5ns.

ORDERING INFORMATION



Datasheet Document History

09/06/09 Pg. 7 Updated the ordering information by removing the "IDT" notation and non RoHS part.

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