# RENESAS

## FAST CMOS 16-BIT LATCHED TRANSCEIVER

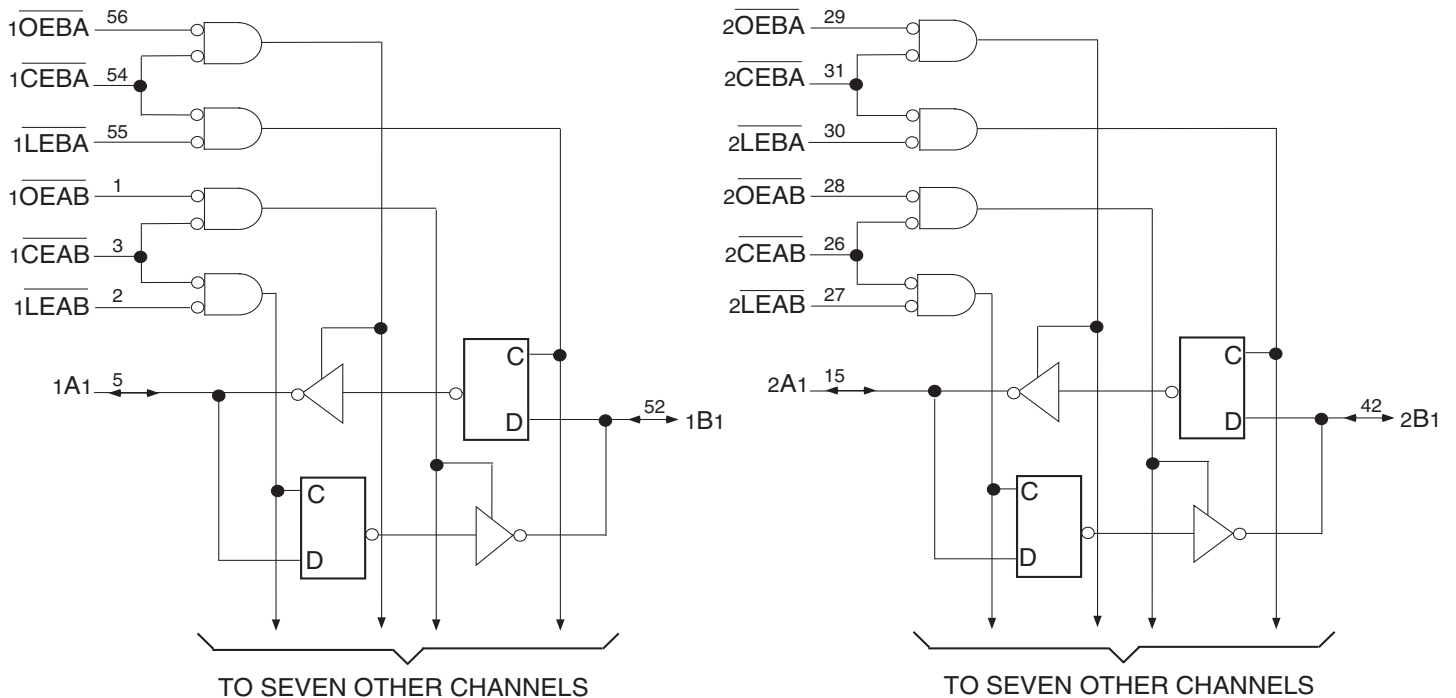### IDT74FCT16543AT/CT

## FEATURES:

- **0.5 MICRON CMOS Technology**
- **High-speed, low-power CMOS replacement for ABT functions**
- **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
- **Low input and output leakage ≤1µA (max.)**
- **$V_{CC}$ = 5V ±10%**
- **High drive outputs (–32mA $I_{OH}$, 64mA $I_{OL}$)**
- **Power off disable outputs permit "live insertion"**
- **Typical $V_{OLP}$ (Output Ground Bounce) < 1.0V at $V_{CC}$ = 5V, $T_A$ = 25°C**
- **Available in SSOP and TSSOP packages**

## DESCRIPTION:

The FCT16543T 16-bit latched transceivers are built using advanced dual metal CMOS technology. These high-speed, low-power devices are organized as two independent 8-bit D-type latched transceivers with separate input and output control to permit independent control of data flow in either direction. For example, the A-to-B Enable (x$\overline{\text{CEAB}}$) must be low in order to enter data from the A port or to output data from the B port. x$\overline{\text{LEAB}}$ controls the latch function. When x$\overline{\text{LEAB}}$ is low, the latches are transparent. A subsequent low-to-high transition of x$\overline{\text{LEAB}}$ signal puts the A latches in the storage mode. x$\overline{\text{OEAB}}$ performs output enable function on the B port. Data flow from the B port to the A port is similar but requires using x$\overline{\text{CEBA}}$, x$\overline{\text{LEBA}}$, and x$\overline{\text{OEBA}}$ inputs. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

The FCT16543T is ideally suited for driving high-capacitance loads and low-impedance backplanes. The output buffers are designed with power off disable capability to allow "live insertion" of boards when used as backplane drivers.

## FUNCTIONAL BLOCK DIAGRAM



TO SEVEN OTHER CHANNELS

TO SEVEN OTHER CHANNELS

INDUSTRIAL TEMPERATURE RANGE

JULY 2017

subject to change without notice.

DSC-5444/6

## PIN CONFIGURATION

| | | | | |
|---|---|---|---|---|
| $1\overline{OEAB}$ | 1 | | 56 | $1\overline{OEBA}$ |
| $1\overline{LEAB}$ | 2 | | 55 | $1\overline{LEBA}$ |
| $1\overline{CEAB}$ | 3 | | 54 | $1\overline{CEBA}$ |
| GND | 4 | | 53 | GND |
| $1A_1$ | 5 | | 52 | $1B_1$ |
| $1A_2$ | 6 | | 51 | $1B_2$ |
| $V_{CC}$ | 7 | | 50 | $V_{CC}$ |
| $1A_3$ | 8 | | 49 | $1B_3$ |
| $1A_4$ | 9 | | 48 | $1B_4$ |
| $1A_5$ | 10 | | 47 | $1B_5$ |
| GND | 11 | | 46 | GND |
| $1A_6$ | 12 | | 45 | $1B_6$ |
| $1A_7$ | 13 | | 44 | $1B_7$ |
| $1A_8$ | 14 | | 43 | $1B_8$ |
| $2A_1$ | 15 | | 42 | $2B_1$ |
| $2A_2$ | 16 | | 41 | $2B_2$ |
| $2A_3$ | 17 | | 40 | $2B_3$ |
| GND | 18 | | 39 | GND |
| $2A_4$ | 19 | | 38 | $2B_4$ |
| $2A_5$ | 20 | | 37 | $2B_5$ |
| $2A_6$ | 21 | | 36 | $2B_6$ |
| $V_{CC}$ | 22 | | 35 | $V_{CC}$ |
| $2A_7$ | 23 | | 34 | $2B_7$ |
| $2A_8$ | 24 | | 33 | $2B_8$ |
| GND | 25 | | 32 | GND |
| $2\overline{CEAB}$ | 26 | | 31 | $2\overline{CEBA}$ |
| $2\overline{LEAB}$ | 27 | | 30 | $2\overline{LEBA}$ |
| $2\overline{OEAB}$ | 28 | | 29 | $2\overline{OEBA}$ |

**TOP VIEW**

| Package Type | Package Code | Order Code |
|---|---|---|
| TSSOP | PAG56 | PAG |
| SSOP | PVG56 | PVG |

## PIN DESCRIPTION

| Pin Names | Description |
|---|---|
| $x\overline{OEAB}$ | A-to-B Output Enable Input (Active LOW) |
| $x\overline{OEBA}$ | B-to-A Output Enable Input (Active LOW) |
| $x\overline{CEAB}$ | A-to-B Enable Input (Active LOW) |
| $x\overline{CEBA}$ | B-to-A Enable Input (Active LOW) |
| $x\overline{LEAB}$ | A-to-B Latch Enable Input (Active LOW) |
| $x\overline{LEBA}$ | B-to-A Latch Enable Input (Active LOW) |
| x A x | A-to-B Data Inputs or B-to-A 3-State Outputs |
| x B x | B-to-A Data Inputs or A-to-B 3-State Outputs |

## ABSOLUTE MAXIMUM RATINGS[1]

| Symbol | Description | Max | Unit |
|---|---|---|---|
| $V_{TERM}$[2] | Terminal Voltage with Respect to GND | –0.5 to 7 | V |
| $V_{TERM}$[3] | Terminal Voltage with Respect to GND | –0.5 to $V_{CC}$+0.5 | V |
| $T_{STG}$ | Storage Temperature | –65 to +150 | °C |
| $I_{OUT}$ | DC Output Current | –60 to +120 | mA |

**NOTES:**
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXX Output and I/O terminals.
3. Outputs and I/O terminals for FCT162XXX.

## CAPACITANCE ($T_A$ = +25°C, f = 1.0MHz)

| Symbol | Parameter[1] | Conditions | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | 3.5 | 6 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0V | 3.5 | 8 | pF |

**NOTE:**
1. This parameter is measured at characterization but not tested.

## FUNCTION TABLE[1, 2]

For A-to-B (Symmetric with B-to-A)

| Inputs | | | Latch Status | Output Buffers |
|---|---|---|---|---|
| $x\overline{CEAB}$ | $x\overline{LEAB}$ | $x\overline{OEAB}$ | xAx to xBx | xBx |
| H | X | X | Storing | Z |
| X | H | X | Storing | X |
| L | L | L | Transparent | Current A Inputs |
| L | H | L | Storing | Previous* A Inputs |
| L | L | H | Transparent | Z |
| L | H | H | Storing | Z |

**NOTES:**
1. * Before $x\overline{LEAB}$ LOW-to-HIGH Transition
   H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
2. A-to-B data flow shown; B-to-A flow control is the same, except using $x\overline{CEBA}$, $x\overline{LEBA}$ and $x\overline{OEBA}$.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Industrial: $T_A$ = –40°C to +85°C, $V_{CC}$ = 5.0V ±10%

| Symbol | Parameter | Test Conditions[1] | | Min. | Typ.[2] | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Level | Guaranteed Logic HIGH Level | | 2 | — | — | V |
| $V_{IL}$ | Input LOW Level | Guaranteed Logic LOW Level | | — | — | 0.8 | V |
| $I_{IH}$ | Input HIGH Current (Input pins)[5] | $V_{CC}$ = Max. | $V_I$ = $V_{CC}$ | — | — | ±1 | µA |
| | Input HIGH Current (I/O pins)[5] | | | — | — | ±1 | |
| $I_{IL}$ | Input LOW Current (Input pins)[5] | | $V_I$ = GND | — | — | ±1 | |
| | Input LOW Current (I/O pins)[5] | | | — | — | ±1 | |
| $I_{OZH}$ | High Impedance Output Current | $V_{CC}$ = Max. | $V_O$ = 2.7V | — | — | ±1 | µA |
| $I_{OZL}$ | (3-State Output pins)[5] | | $V_O$ = 0.5V | — | — | ±1 | |
| $V_{IK}$ | Clamp Diode Voltage | $V_{CC}$ = Min., $I_{IN}$ = –18mA | | — | –0.7 | –1.2 | V |
| $I_{OS}$ | Short Circuit Current | $V_{CC}$ = Max., $V_O$ = GND[3] | | –80 | –140 | –250 | mA |
| $V_H$ | Input Hysteresis | — | | — | 100 | — | mV |
| $I_{CCL}$ $I_{CCH}$ $I_{CCZ}$ | Quiescent Power Supply Current | $V_{CC}$ = Max $V_{IN}$ = GND or $V_{CC}$ | | — | 5 | 500 | µA |

## OUTPUT DRIVE CHARACTERISTICS

| Symbol | Parameter | Test Conditions[1] | | Min. | Typ.[2] | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $I_O$ | Output Drive Current | $V_{CC}$ = Max., $V_O$ = 2.5V[3] | | –50 | — | –180 | mA |
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min. $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = –3mA | 2.5 | 3.5 | — | V |
| | | | $I_{OH}$ = –15mA | 2.4 | 3.5 | — | V |
| | | | $I_{OH}$ = –32mA[4] | 2 | 3 | — | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min. $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 64mA | — | 0.2 | 0.55 | V |
| $I_{OFF}$ | Input/Output Power Off Leakage[5] | $V_{CC}$ = 0V, $V_{IN}$ = or $V_O$ ≤ 4.5V | | — | — | ±1 | µA |

**NOTES:**
1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC}$ = 5.0V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. This test limit for this parameter is ±5µA at $T_A$ = –55°C.

## POWER SUPPLY CHARACTERISTICS

| Symbol | Parameter | Test Conditions[1] | | Min. | Typ.[2] | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $\Delta I_{CC}$ | Quiescent Power Supply Current TTL Inputs HIGH | $V_{CC}$ = Max. $V_{IN}$ = 3.4V[3] | | — | 0.5 | 1.5 | mA |
| $I_{CCD}$ | Dynamic Power Supply Current[4] | $V_{CC}$ = Max., Outputs Open x$\overline{CEAB}$ and x$\overline{OEAB}$ = GND x$\overline{CEBA}$ = $V_{CC}$ One Input Toggling 50% Duty Cycle | $V_{IN} = V_{CC}$ $V_{IN}$ = GND | — | 60 | 100 | µA/MHz |
| $I_C$ | Total Power Supply Current[6] | $V_{CC}$ = Max., Outputs Open $f_i$ = 10MHz 50% Duty Cycle x$\overline{LEAB}$, x$\overline{CEAB}$ and x$\overline{OEAB}$ = GND x$\overline{CEBA}$ = $V_{CC}$ One Bit Toggling | $V_{IN} = V_{CC}$ $V_{IN}$ = GND | — | 0.6 | 1.5 | mA |
| | | | $V_{IN}$ = 3.4V $V_{IN}$ = GND | — | 0.9 | 2.3 | |
| | | $V_{CC}$ = Max., Outputs Open $f_i$ = 2.5MHz 50% Duty Cycle x$\overline{LEAB}$, x$\overline{CEAB}$ and x$\overline{OEAB}$ = GND x$\overline{CEBA}$ = $V_{CC}$ Sixteen Bits Toggling | $V_{IN} = V_{CC}$ $V_{IN}$ = GND | — | 2.4 | 4.5[5] | |
| | | | $V_{IN}$ = 3.4V $V_{IN}$ = GND | — | 6.4 | 16.5[5] | |

**NOTES:**

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC}$ = 5.0V, +25°C ambient.
3. Per TTL driven input ($V_{IN}$ = 3.4V). All other inputs at $V_{CC}$ or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the $I_{CC}$ formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$

   $I_{CC}$ = Quiescent Current ($I_{CCL}$, $I_{CCH}$ and $I_{CCZ}$)

   $\Delta I_{CC}$ = Power Supply Current for a TTL High Input ($V_{IN}$ = 3.4V)

   $D_H$ = Duty Cycle for TTL Inputs High

   $N_T$ = Number of TTL Inputs at $D_H$

   $I_{CCD}$ = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

   $f_{CP}$ = Clock Frequency for Register Devices (Zero for Non-Register Devices)

   $N_{CP}$ = Number of Clock Inputs at $f_{CP}$

   $f_i$ = Input Frequency

   $N_i$ = Number of Inputs at $f_i$

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

| Symbol | Parameter | Condition[2] | 74FCT16543AT | | 74FCT16543CT | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min.[2] | Max. | Min.[2] | Max. | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Transparent Mode xAx to xBx or xBx to xAx | $C_L = 50pF$ $R_L = 500\Omega$ | 1.5 | 6.5 | 1.5 | 5.1 | ns |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay x$\overline{LEBA}$ to xAx, x$\overline{LEAB}$ to xBx | | 1.5 | 8 | 1.5 | 5.6 | ns |
| $t_{PHZ}$ $t_{PLZ}$ | Output Enable Time x$\overline{OEBA}$ or x$\overline{OEAB}$ to xAx or xBx x$\overline{CEBA}$ or x$\overline{CEAB}$ to xAx or xBx | | 1.5 | 9 | 1.5 | 7.8 | ns |
| $t_{PZH}$ $t_{PZL}$ | Output Disable Time x$\overline{OEBA}$ or x$\overline{OEAB}$ to xAx or xBx x$\overline{CEBA}$ or x$\overline{CEAB}$ to xAx or xBx | | 1.5 | 7.5 | 1.5 | 6.5 | ns |
| $t_{SU}$ | Set-up Time HIGH or LOW xAx or xBx to x$\overline{LEAB}$ or x$\overline{LEBA}$ | | 2 | — | 2 | — | ns |
| $t_H$ | Hold Time HIGH or LOW xAx or xBx to x$\overline{LEAB}$ or x$\overline{LEBA}$ | | 2 | — | 2 | — | ns |
| $t_W$ | x$\overline{LEAB}$ or x$\overline{LEBA}$ Pulse Width LOW | | 4 | — | 4 | — | ns |
| $t_{SK(o)}$ | Output Skew[3] | | — | 0.5 | — | 0.5 | ns |

**NOTES:**
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested.
3. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.
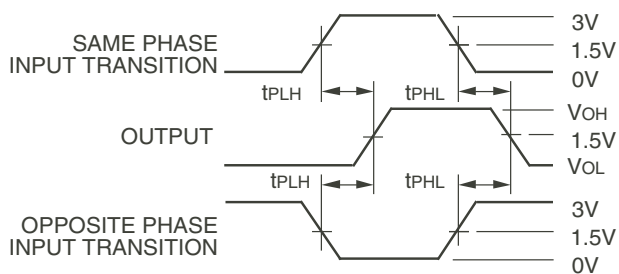
# TEST CIRCUITS AND WAVEFORMS
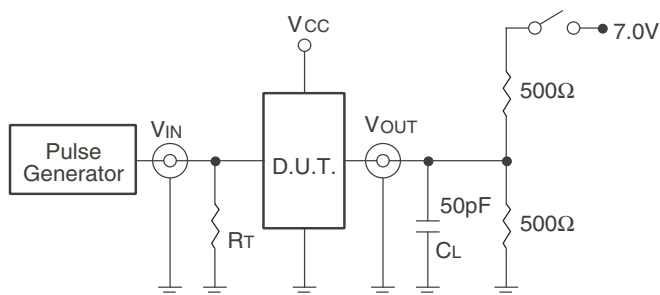


*Test Circuits for All Outputs*

## SWITCH POSITION

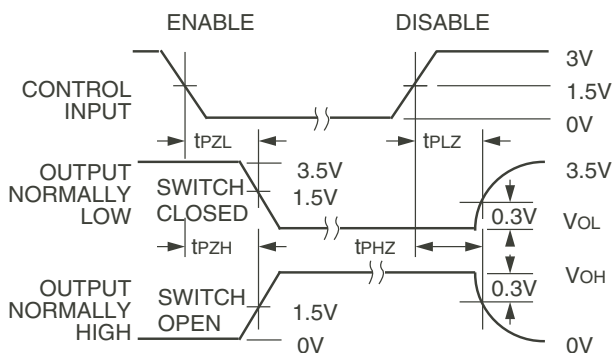| Test | Switch |
|---|---|
| Open Drain<br>Disable Low<br>Enable Low | Closed |
| All Other Tests | Open |

**DEFINITIONS:**

$C_L$ = Load capacitance: includes jig and probe capacitance.

$R_T$ = Termination resistance: should be equal to $Z_{OUT}$ of the Pulse Generator.



*Set-up, Hold, and Release Times*



*Pulse Width*
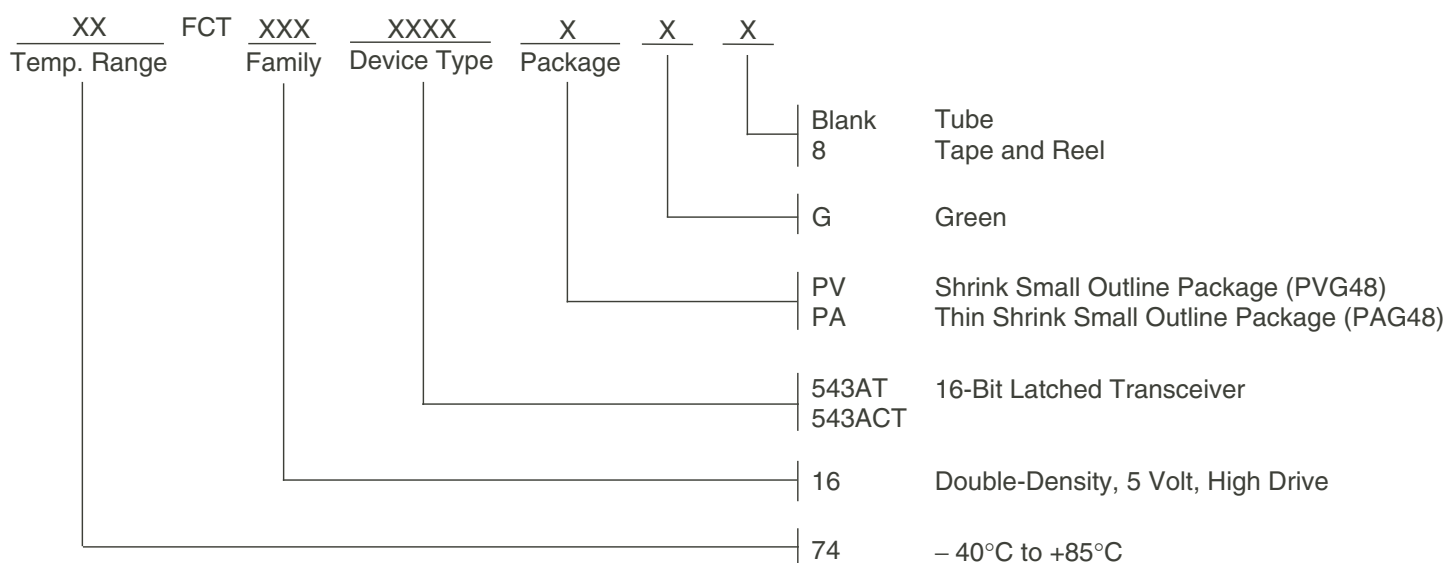


*Propagation Delay*



*Enable and Disable Times*

**NOTES:**

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate $\leq$ 1.0MHz; $t_F \leq$ 2.5ns; $t_R \leq$ 2.5ns.

## ORDERING INFORMATION

| <u>XX</u> | FCT | <u>XXX</u> | <u>XXXX</u> | <u>X</u> | X | X |
|---|---|---|---|---|---|---|
| Temp. Range | | Family | Device Type | Package | | |

| | |
|---|---|
| Blank | Tube |
| 8 | Tape and Reel |

| | |
|---|---|
| G | Green |

| | |
|---|---|
| PV | Shrink Small Outline Package (PVG48) |
| PA | Thin Shrink Small Outline Package (PAG48) |

| | |
|---|---|
| 543AT | 16-Bit Latched Transceiver |
| 543ACT | |

| | |
|---|---|
| 16 | Double-Density, 5 Volt, High Drive |

| | |
|---|---|
| 74 | − 40°C to +85°C |

## Orderable Part Information

| Speed (ns) | Orderable Part ID | Pkg. Code | Pkg. Type | Temp. Grade |
|---|---|---|---|---|
| A | 74FCT16543ATPAG | PAG56 | TSSOP | I |
| | 74FCT16543ATPAG8 | PAG56 | TSSOP | I |
| | 74FCT16543ATPVG | PVG56 | SSOP | I |
| | 74FCT16543ATPVG8 | PVG56 | SSOP | I |
| C | 74FCT16543CTPAG | PAG56 | TSSOP | I |
| | 74FCT16543CTPAG8 | PAG56 | TSSOP | I |
| | 74FCT16543CTPVG | PVG56 | SSOP | I |
| | 74FCT16543CTPVG8 | PVG56 | SSOP | I |

## Datasheet Document History

09/28/2009    Pg. 7              Updated the ordering information by removing the "IDT" notation and non RoHS part.
07/31/2017    Pg. 1, 2, 5, 7     Added table under pin configuration diagram with detailed package information. Updated the ordering information diagram by deleting 543ET, TSSOP package and adding Tube, Tape and Reel. Added orderable part information table.

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