3.3V CMOS OCTAL BUFFER/LINE DRIVER

74FCT3244/A

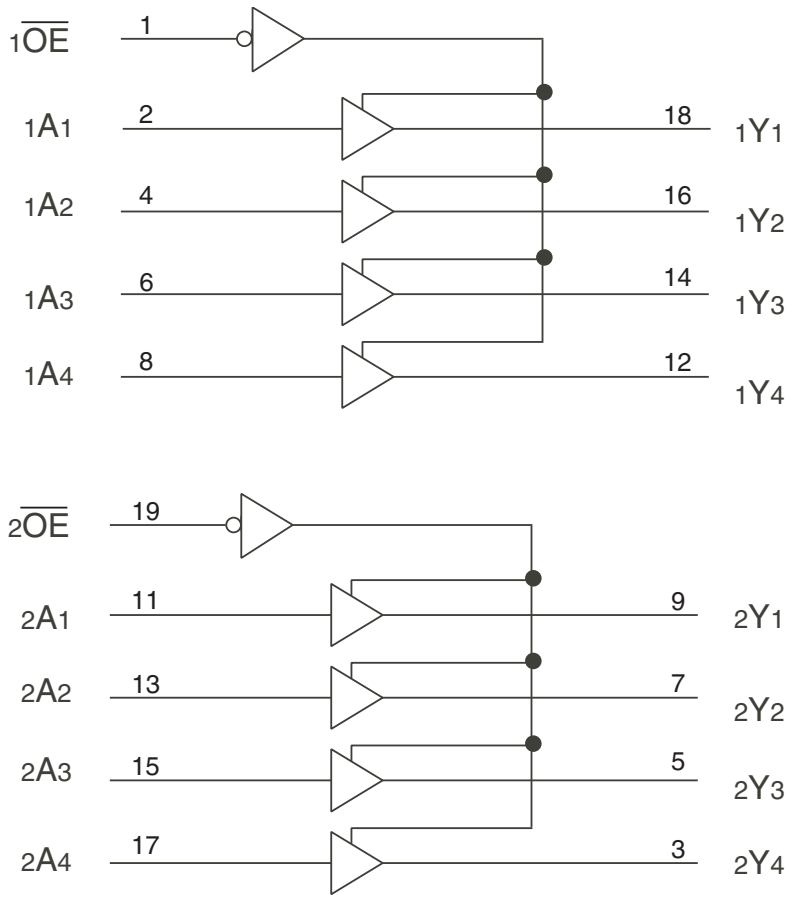
FEATURES:

- **0.5 MICRON CMOS Technology**
- **ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)**
- **V_{CC} = 3.3V ±0.3V, Normal Range**
- **V_{CC} = 2.7V to 3.6V, Extended Range**
- **CMOS power levels (0.4µW typ. static)**
- **Rail-to-Rail output swing for increased noise margin**
- **Available in QSOP, SOIC, SSOP, and TSSOP packages**

DESCRIPTION:

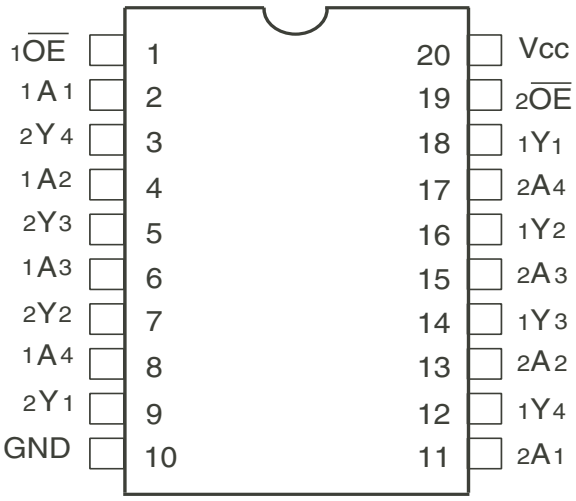
The FCT3244/A octal buffer/line drivers are built using advanced dual metal CMOS technology. These high-speed, low-power buffers are designed to be used as memory data and address drivers, clock drivers, and bus-oriented transmitter/receivers. The three-state controls are designed to operate these devices in a dual-nibble or single-byte mode. All inputs are designed with hysteresis for improved noise margin.

FUNCTIONAL BLOCK DIAGRAM



INDUSTRIAL TEMPERATURE RANGE

PIN CONFIGURATION



TOP VIEW

Package Type	Package Code	Order Code
QSOP	PCG20	QG
SOIC	PSG20	SOG
TSSOP	PGG20	PGG
SSOP	PYG20	PYG

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +4.6	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to +7	V
V_{TERM}(4)	Terminal Voltage with Respect to GND	–0.5 to V_{CC}+0.5	V
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	DC Output Current	–60 to +60	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{CC} terminals.
3. Input terminals.
4. Outputs and I/O terminals.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3.5	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	4	8	pF

NOTE:

1. This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
x$\overline{OE}$	3–State Output Enable Inputs (Active LOW)
xAx	Data Inputs
xYx	3-State Outputs

FUNCTION TABLE(1)

Inputs		Outputs
x$\overline{OE}$	xAx	xYx
L	L	L
L	H	H
H	X	Z

NOTE:

1. H = HIGH Voltage Level
   X = Don't Care
   L = LOW Voltage Level
   Z = High Impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Industrial: T_A = -40°C to +85°C, V_{CC} = 2.7V to 3.6V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level		2	—	5.5	V
	Input HIGH Level (I/O pins)			2	—	Vcc+0.5	
V_{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		–0.5	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)	V_{CC} = Max.	V_I = 5.5V	—	—	±1	µA
	Input HIGH Current (I/O pins)		V_I = V_{CC}	—	—	±1	
I_{IL}	Input LOW Current (Input pins)		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)		V_I = GND	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	±1	µA
I_{OZL}	(3-State Output pins)		V_O = GND	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{ODH}	Output HIGH Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		–36	–60	–110	mA
I_{ODL}	Output LOW Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		50	90	200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –0.1mA	V_{CC}–0.2	—	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –3mA	2.4	3	—	
		V_{CC} = 3V V_{IN} = V_{IH} or V_{IL}	I_{OH} = –8mA	2.4[5]	3	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 0.1mA	—	—	0.2	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA	—	0.2	0.4	
			I_{OL} = 24mA	—	0.3	0.55	
		V_{CC} = 3V V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA		0.3	0.5	
I_{OS}	Short Circuit Current[4]	V_{CC} = Max., V_O = GND[3]		–60	–135	–240	mA
V_H	Input Hysteresis	—		—	150	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.1	10	µA

NOTES:
1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient and maximum loading.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. V_{OH} = V_{CC} - 0.6V at rated current.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max.	V_{IN} = V_{CC} - 0.6V	—	2	30	µA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open xOE = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	60	85	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle xOE = GND One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	0.6	0.9	mA
			V_{IN} = V_{CC} - 0.6V V_{IN} = GND	—	0.6	0.9	
		V_{CC} = Max. Outputs Open f_i = 2.5MHz 50% Duty Cycle xOE = GND Eight Bits Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	1.2	1.7[5]	
			V_{IN} = V_{CC} - 0.6V V_{IN} = GND	—	1.2	1.8[5]	

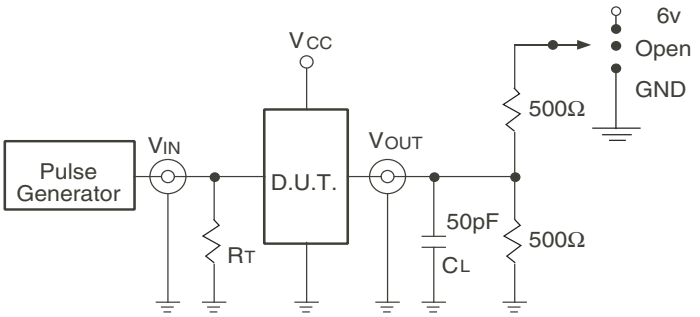
NOTES:
1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Per TTL driven input. All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of ΔI_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CC}, I_{CCH}, and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for register devices (zero for non-register devices)
   N_{CP} = Number of clock inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE[1]

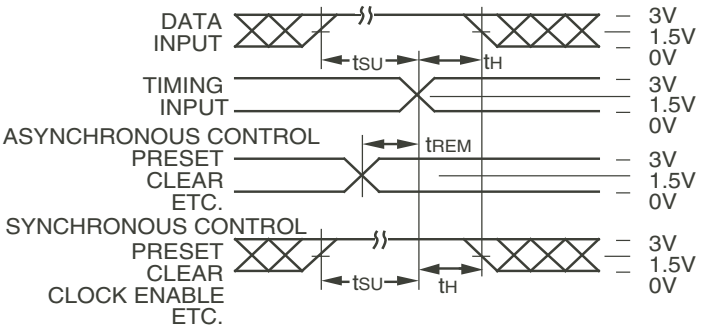
Symbol	Parameter	Condition[2]	74FCT3244		74FCT3244A		Unit
			Min.[3]	Max.	Min.[3]	Max.	
t_{PLH} t_{PHL}	Propagation Delay xAx to xYx	C_L = 50pF R_L = 500Ω	1.5	6.5	1.5	4.8	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	8	1.5	6.2	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	7	1.5	5.6	ns

NOTES:
1. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ±0.3V, Normal Range. For V_{CC} = 2.7V to 3.6V, Extended Range, all Propagation Delays and Enable/ Disable times should be degraded by 20%.
2. See test circuit and waveforms.
3. Minimum limits are guaranteed but not tested on Propagation Delays.

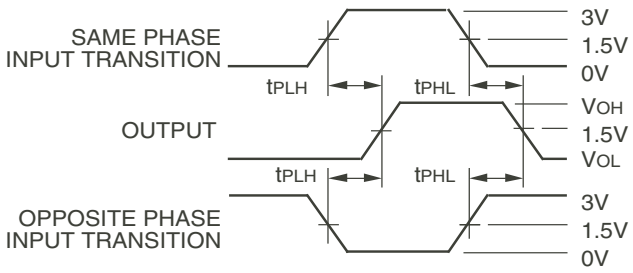
TEST CIRCUITS AND WAVEFORMS



Test Circuits for All Outputs



Set-Up, Hold, and Release Times



Propagation Delay

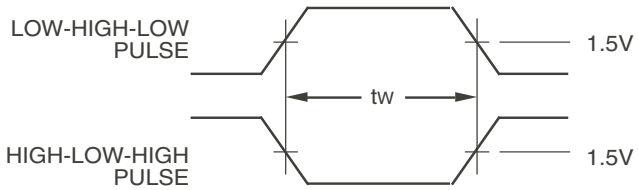
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	6V
Disable High Enable High	GND
All Other Tests	Open

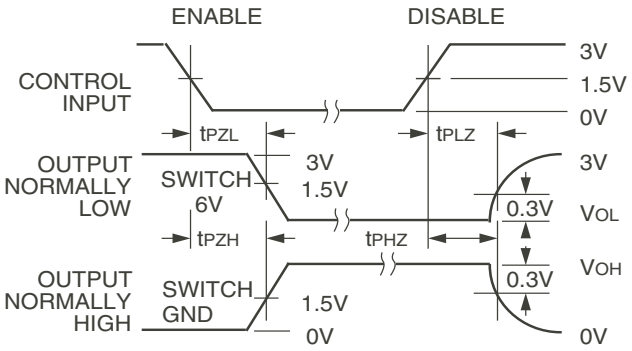
DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.



Pulse Width

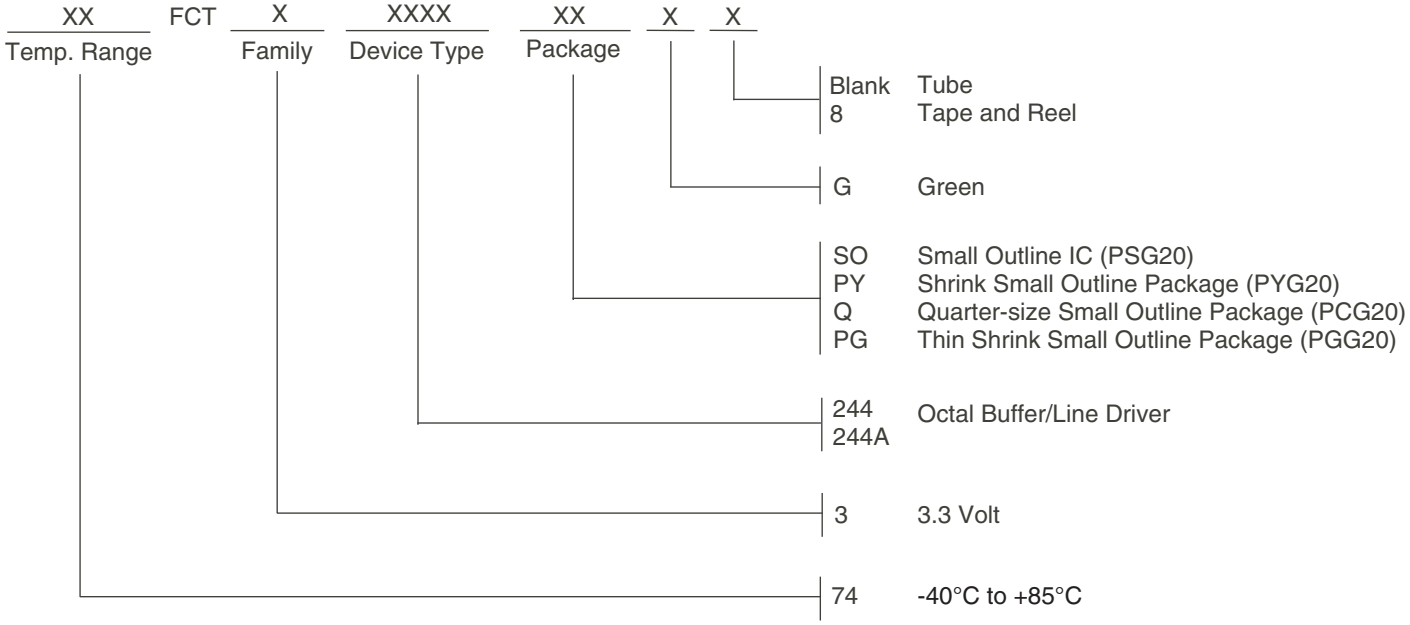


Enable and Disable Times

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_O ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
3. If Vcc is below 3V, input voltage swings should be adjusted not to exceed Vcc.

ORDERING INFORMATION



Orderable Part Information

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
A	74FCT3244APGG	PGG20	TSSOP	I
	74FCT3244APGG8	PGG20	TSSOP	I
	74FCT3244APYG	PYG20	SSOP	I
	74FCT3244APYG8	PYG20	SSOP	I
	74FCT3244AQG	PCG20	QSOP	I
	74FCT3244AQG8	PCG20	QSOP	I
	74FCT3244ASOG	PSG20	SOIC	I
	74FCT3244ASOG8	PSG20	SOIC	I

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
	74FCT3244PGG	PGG20	TSSOP	I
	74FCT3244PGG8	PGG20	TSSOP	I
	74FCT3244PYG	PYG20	SSOP	I
	74FCT3244PYG8	PYG20	SSOP	I
	74FCT3244QG	PCG20	QSOP	I
	74FCT3244QG8	PCG20	QSOP	I
	74FCT3244SOG	PSG20	SOIC	I
	74FCT3244SOG8	PSG20	SOIC	I

Datasheet Document History

09/30/2009	Pg. 6	Updated the ordering information by removing the "IDT" notation and non RoHS part.
08/31/2011	Pg. 6	Added PGG to ordering information.
07/31/2017	Pgs. 2, 6	Added table under pin configuration diagram with detailed package information. Updated the ordering information diagram adding Tube, Tape and Reel. Added new table of orderable part information.
05/23/2018	Pg. 6	Updated new table of orderable part information.
02/11/2020	Pgs. 1-7	Rebranded as Renesas datasheet.

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