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April 1st, 2010 Renesas Electronics Corporation

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HD74LV1GT125A

Bus Buffer Gate with 3-state Output / CMOS Logic Level Shifter

REJ03D0123-0900 Rev.9.00 Mar 21, 2008

Description

The HD74LV1GT125A has a bus buffer gate with 3–state output in a 5 pin package. Output is disabled when the associated output enable (\overline{OE}) input is high. To ensure the high impedance state during power up or power down, \overline{OE} should be connected to V_{CC} through a pull-down resistor; the minimum value of the resistor is determined by the current sourcing capability of the driver. The input protection circuitry on this device allows over voltage tolerance on the input, allowing the device to be used as a logic–level translator from 3.0 V CMOS Logic to 5.0 V CMOS Logic or from 1.8 V CMOS logic to 3.0 V CMOS Logic while operating at the high-voltage power supply. Low voltage and high-speed operation is suitable for the battery powered products (e.g., notebook computers), and the low power consumption extends the battery life.

Features

- The basic gate function is lined up as Renesas uni logic series.
- Supplied on emboss taping for high-speed automatic mounting.
- TTL compatible input level.

Supply voltage range: 3.0 to 5.5 V

Operating temperature range : -40 to +85°C

• Logic-level translate function

3.0 V CMOS logic \rightarrow 5.0 V CMOS logic (@V_{CC} = 5.0 V)

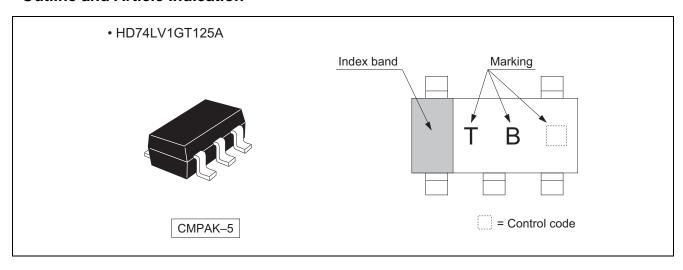
1.8 V or 2.5 V CMOS logic \rightarrow 3.3 V CMOS logic (@V_{CC} = 3.3 V)

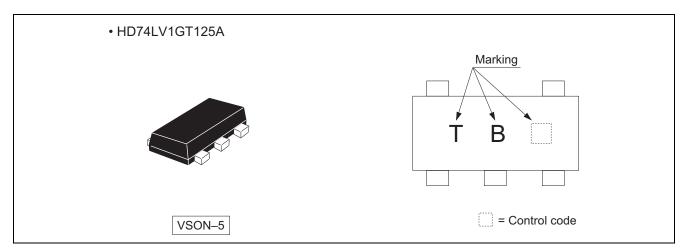
- All inputs V_{IH} (Max.) = 5.5 V (@ V_{CC} = 0 V to 5.5 V) All outputs V_{O} (Max.) = 5.5 V (@ V_{CC} = 0 V, Output : Z)
- Output current $\pm 6 \text{ mA}$ (@V_{CC} = 3.0 V to 3.6 V), $\pm 12 \text{ mA}$ (@V_{CC} = 4.5 V to 5.5 V)
- All the logical input has hysteresis voltage for the slow transition.
- Ordering Information

Part Name	Pookogo Typo	Package Code	Package	Taping Abbreviation	
Part Name	Package Type	(Previous Code)	Abbreviation	(Quantity)	
HD74LV1GT125ACME	CMPAK-5 pin	PTSP0005ZC-A	CM	E (3000 pcs/reel)	
IND/4LV IGT 125ACIVIE	CIVIPAN-5 PIII	(CMPAK-5V)	Civi		
LIDZAL VA CTA DE A VOE	VCON F nin	PUSN0005KA-A	\/C	E (3000 pcs/reel)	
HD74LV1GT125AVSE	VSON-5 pin	(TNP-5DV)	VS		

Note: Please consult the sales office for the above package availability.

Outline and Article Indication



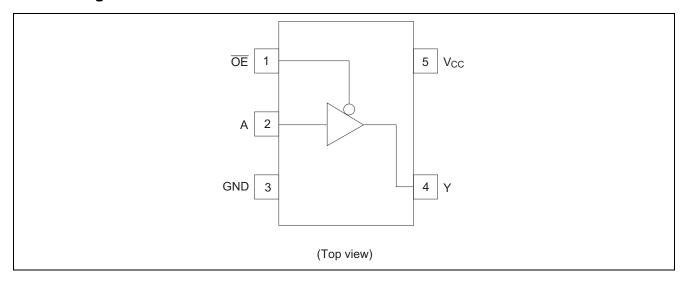


Function Table

Inp	Output Y		
ŌĒ	Α	Output 1	
L	Н	Н	
L	L	L	
Н	X	Z	

H : High level
L : Low level
X : Immaterial
Z : High impedance

Pin Arrangement



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Test Conditions
Supply voltage range	Vcc	-0.5 to 7.0	V	
Input voltage range *1	VI	-0.5 to 7.0	V	
Output voltage range *1, 2	1/	-0.5 to V _{CC} + 0.5	V	Output : H or L
Output voltage range	Vo	-0.5 to 7.0	v	V _{CC} : OFF or Output : Z
Input clamp current	I _{IK}	-20	mA	V _I < 0
Output clamp current	lok	±50	mA	$V_0 < 0$ or $V_0 > V_{CC}$
Continuous output current	lo	±25	mA	$V_O = 0$ to V_{CC}
Continuous current through V _{CC} or GND	I _{CC} or I _{GND}	±50	mA	
Maximum power dissipation at Ta = 25°C (in still air) *3	P _T	200	mW	
Storage temperature	Tstg	-65 to 150	°C	

Notes: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore no two of which may be realized at the same time.

- 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- 2. This value is limited to 5.5 V maximum.
- 3. The maximum package power dissipation was calculated using a junction temperature of 150°C.

Recommended Operating Conditions

Item	Symbol	Min	Max	Unit	Conditions
Supply voltage range	V _{CC}	3.0	5.5	V	
Input voltage range	VI	0	5.5	V	
Output voltage range	Vo	0	V _{CC}	V	
Output voltage range	Vo	0	5.5	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	Output : Z
	I _{OH}	_	6	mA	$V_{CC} = 3.0 \text{ to } 3.6 \text{ V}$
Output current		_	12	IIIA	$V_{CC} = 4.5 \text{ to } 5.5 \text{ V}$
Output current	I _{OL}	_	-6	mA	$V_{CC} = 3.0 \text{ to } 3.6 \text{ V}$
		_	-12	IIIA	$V_{CC} = 4.5 \text{ to } 5.5 \text{ V}$
Input transition rise or fall rate	Δt / Δν	0	100	ns / V	$V_{CC} = 3.0 \text{ to } 3.6 \text{ V}$
input transition lise of fall fate	Δι / Δν	0	20	115 / V	$V_{CC} = 4.5 \text{ to } 5.5 \text{ V}$
Operating free-air temperature	Ta	-40	85	°C	

Note: Unused or floating inputs must be held high or low.



Electrical Characteristic

• $Ta = -40 \text{ to } 85^{\circ}\text{C}$

Item	Symbol	V _{CC} (V) *	Min	Тур	Max	Unit	Test condition
	V _{IH}	3.0 to 3.6	1.5				
Input voltage	VIH	4.5 to 5.5	2.0			V	
input voltage	V_{IL}	3.0 to 3.6	_		0.6	V	
	V IL	4.5 to 5.5	_		0.8		
Hysteresis voltage	VH	3.3	_	0.10		V	$V_T^+ - V_T^-$
Trysteresis voltage	VН	5.0	_	0.15		V	V _T - V _T
		Min to Max	V _{CC} -0.1				$I_{OH} = -50 \mu A$
	V_{OH}	3.0	2.48				$I_{OH} = -6 \text{ mA}$
Output voltage		4.5	3.8	_	_	V	$I_{OH} = -12 \text{ mA}$
Output voltage	V _{OL}	Min to Max	_	_	0.1		$I_{OL} = 50 \mu A$
		3.0	_	_	0.44		$I_{OL} = 6 \text{ mA}$
		4.5	_	_	0.55		I _{OL} = 12 mA
Input current	I _{IN}	0 to 5.5	_	_	±1	μΑ	$V_{IN} = 5.5 \text{ V or GND}$
Off state output current	l _{OZ}	Min to Max	_	_	±5	μΑ	V _O = 5.5 V or GND
Quiescent supply current	I _{CC}	5.5	_	_	10	μΑ	$V_{IN} = V_{CC}$ or GND, $I_O = 0$
	ΔI_{CC}	5.5	_		1.5	mA	One input $V_{IN} = 3.4 \text{ V}$, other input V_{CC} or GND
Output leakage current	I _{OFF}	0			5	μΑ	V_{IN} or $V_O = 0$ to 5.5 V
Input capacitance	C _{IN}	5.0	_	3.0	_	pF	$V_{IN} = V_{CC}$ or GND

Note: For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

Switching Characteristics

• $V_{CC} = 3.3 \pm 0.3 \text{ V}$

Item	Symbol	Ta = 25°C		Ta = -40 to 85°C		Unit	Test	FROM	ТО	
		Min	Тур	Max	Min	Max	Unit	Conditions	(Input)	(Output)
Propagation	t _{PLH}	_	4.5	9.0	1.0	10.5	ne	$C_L = 15 pF$	Α	Υ
delay time	t _{PHL}	_	6.0	11.5	1.0	13.0	ns	$C_L = 50 pF$	^	
Enable time	t _{ZH}	_	4.5	9.0	1.0	10.5	⊣ ns	$C_L = 15 pF$	ŌĒ	Y
Enable time t _{ZL}	t_{ZL}	_	6.0	11.5	1.0	13.0		$C_L = 50 pF$		
Disable time	t _{HZ}	_	4.0	10.0	1.0	11.5	— ns	$C_L = 15 pF$	ŌĒ	>
Disable time	t_{LZ}	_	5.5	13.5	1.0	15.0		C _L = 50 pF	OE	r

• $V_{CC} = 5.0 \pm 0.5 \text{ V}$

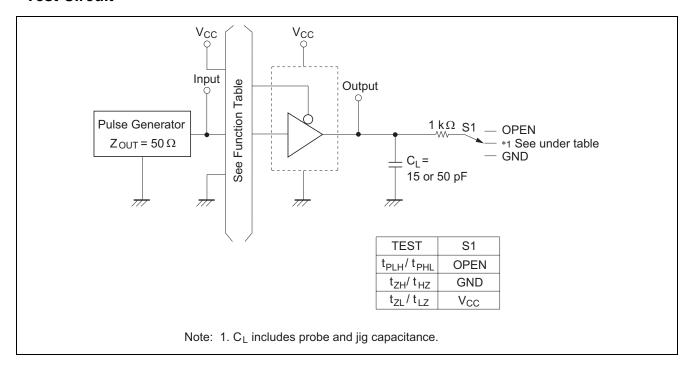
Itama Cum	Symbol	•	Ta = 25°C		Ta = -40 to 85°C		Unit	Test	FROM	ТО
ltem	Symbol	Symbol Min Typ Max Min Max Unit	Unit	Conditions	(Input)	(Output)				
Propagation	t _{PLH}	_	3.4	5.5	1.0	6.5	กร	$C_L = 15 pF$	Α	Υ
delay time	t_{PHL}	_	4.3	7.5	1.0	8.5		$C_L = 50 pF$	A	
Enable time	t _{zH}	_	3.4	5.1	1.0	6.0	ns	$C_L = 15 pF$	ŌĒ	Y
Enable time t _{ZL}	t_{ZL}	_	4.4	7.1	1.0	8.0		$C_L = 50 pF$		
Diaable time	t _{HZ}	_	3.2	6.8	1.0	8.0	ns	$C_L = 15 pF$	ŌĒ	Y
Disable time t_{LZ}	t_LZ	_	4.0	8.8	1.0	10.0		$C_L = 50 pF$		

Operating Characteristics

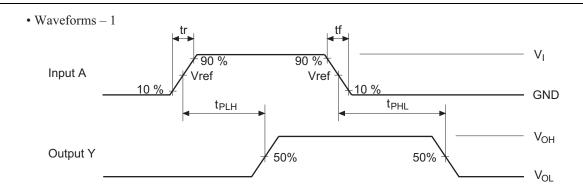
• $C_L = 50 \text{ pF}$

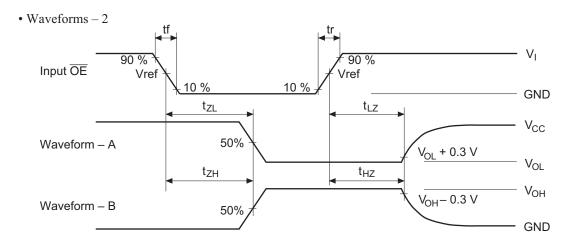
Item	Symbol	V _{cc} (V)	Ta = 25°C			Unit	Test Conditions	
iteiii	Symbol	VCC (V)	Min	Тур	Max	Onit	rest Conditions	
Power dissipation capacitance	C _{PD}	5.0	_	11.5		pF	f = 10 MHz	

Test Circuit



Waveforms



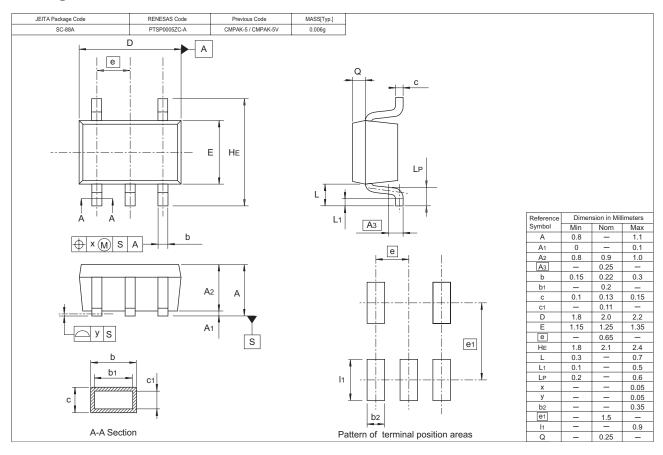


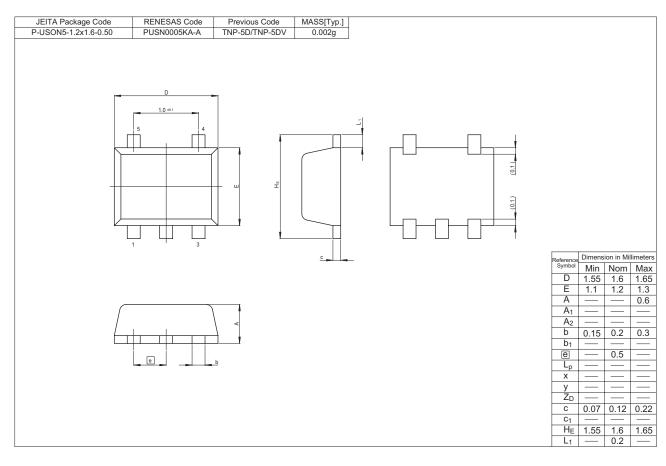
V _{CC} (V)	IN	Vref		
VCC (V)	V _I t _r / t _f		VICI	
3.3±0.3	2.5 V	≤ 3.0 ns	50%	
5.0±0.5	3 V	≤ 3.0 ns	1.5 V	

Notes: 1. Input waveform : PRR \leq 1 MHz, Zo = 50 Ω .

- 2. Waveform A is for an output with internal conditions such that the output is low except when disabled by the output control.
- 3. Waveform B is for an output with internal conditions such that the output is high except when disabled by the output control.
- 4. The output are measured one at a time with one transition per measurement.

Package Dimensions





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