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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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# HD74LV2GT125A

## Dual Bus Buffer with 3–state Output / CMOS Logic Level Shifter

REJ03D0148–0200Z  
(Previous ADE-205-676A (Z))  
Rev.2.00  
Oct.23.2003

### Description

The HD74LV2GT125A has dual bus buffer with 3–state output in an 8 pin package. Output is disabled when the associated output enable ( $\overline{OE}$ ) input is high. To ensure the high impedance state during power up or power down,  $\overline{OE}$  should be connected to  $V_{CC}$  through a pull-up resistor; the minimum value of the resistor is determined by the current sinking capability of the driver. The input protection circuitry on this device allows over voltage tolerance on the input, allowing the device to be used as a logic–level translator from 3.0 V CMOS Logic to 5.0 V CMOS Logic or from 1.8 V CMOS logic to 3.0 V CMOS Logic while operating at the high-voltage power supply. Low voltage and high-speed operation is suitable for the battery powered products (e.g., notebook computers), and the low power consumption extends the battery life.

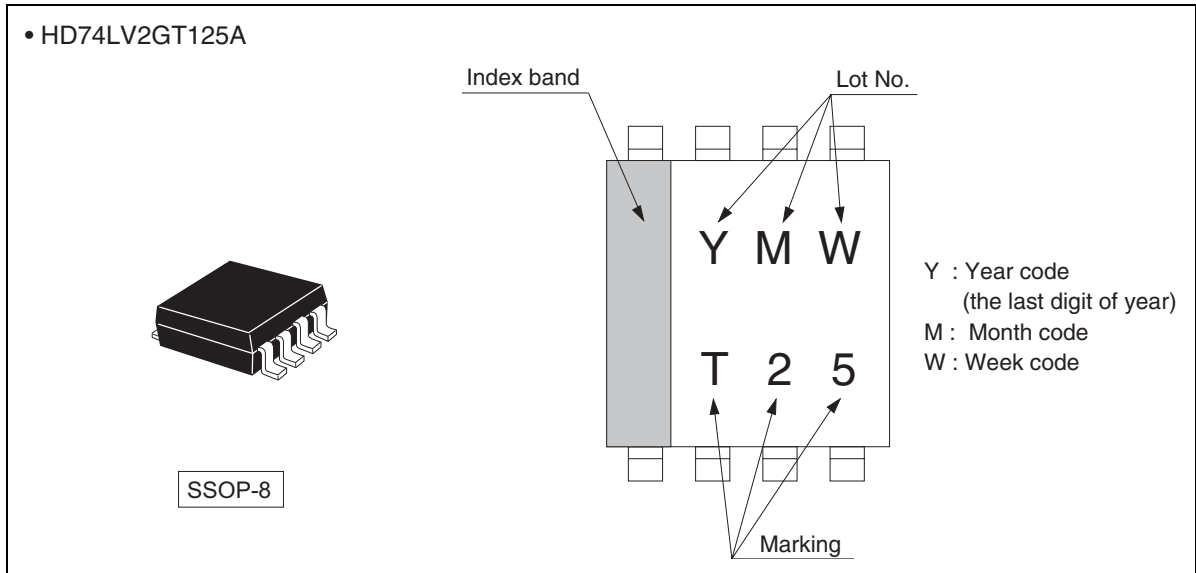
### Features

- The basic gate function is lined up as Renesas uni logic series.
- Supplied on emboss taping for high-speed automatic mounting.
- TTL compatible input level.  
Supply voltage range : 3.0 to 5.5 V  
Operating temperature range : –40 to +85°C
- Logic-level translate function  
3.0 V CMOS logic → 5.0 V CMOS logic (@ $V_{CC} = 5.0$  V)  
1.8 V or 2.5 V CMOS logic → 3.3 V CMOS logic (@ $V_{CC} = 3.3$  V)
- All inputs  $V_{IH}$  (Max.) = 5.5 V (@ $V_{CC} = 0$  V to 5.5 V)  
All outputs  $V_O$  (Max.) = 5.5 V (@ $V_{CC} = 0$  V, Output : Z)
- Output current  $\pm 6$  mA (@ $V_{CC} = 3.0$  V to 3.6 V),  $\pm 12$  mA (@ $V_{CC} = 4.5$  V to 5.5 V)
- All the logical input has hysteresis voltage for the slow transition.
- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LV2GT125AUSE	SSOP-8 pin	TTP-8DBV	US	E (3,000 pcs/reel)

## HD74LV2GT125A

### Outline and Article Indication



### Function Table

#### Inputs

$\overline{\text{OE}}$	A	Output Y
L	H	H
L	L	L
H	X	Z

H : High level

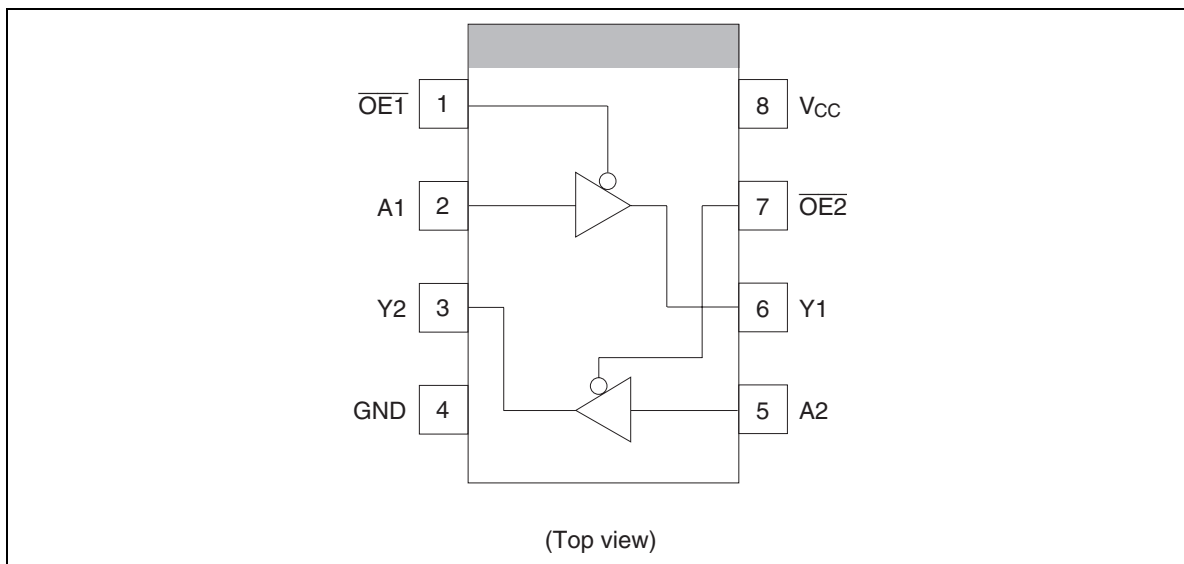
L : Low level

X : Immaterial

Z : High impedance

## HD74LV2GT125A

### Pin Arrangement



### Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Test Conditions
Supply voltage range	$V_{CC}$	-0.5 to 7.0	V	
Input voltage range <sup>*1</sup>	$V_I$	-0.5 to 7.0	V	
Output voltage range <sup>*1,2</sup>	$V_O$	-0.5 to $V_{CC} + 0.5$ -0.5 to 7.0	V	Output : H or L $V_{CC}$ : OFF or output : Z
Input clamp current	$I_{IK}$	-20	mA	$V_I < 0$
Output clamp current	$I_{OK}$	$\pm 50$	mA	$V_O < 0$ or $V_O > V_{CC}$
Continuous output current	$I_O$	$\pm 25$	mA	$V_O = 0$ to $V_{CC}$
Continuous current through $V_{CC}$ or GND	$I_{CC}$ or $I_{GND}$	$\pm 50$	mA	
Maximum power dissipation at $T_a = 25^\circ\text{C}$ (in still air) <sup>*3</sup>	$P_T$	200	mW	
Storage temperature	$T_{stg}$	-65 to 150	$^\circ\text{C}$	

Notes: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore no two of which may be realized at the same time.

1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The maximum package power dissipation was calculated using a junction temperature of  $150^\circ\text{C}$ .

## HD74LV2GT125A

### Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Test Conditions
Supply voltage	$V_{CC}$	3.0 to 5.5	V	
Input voltage	$V_{IN}$	0 to 5.5	V	
Output voltage	$V_{OUT}$	0 to $V_{CC}$ 0 to 5.5	V	Output : Z
Operating temperature	$T_{opr}$	-40 to +85	°C	
Input rise / fall time	$t_r, t_f$	0 to 100 ( $V_{CC} = 3.0$ to 3.6 V) 0 to 20 ( $V_{CC} = 4.5$ to 5.5 V)	ns	

### Electrical Characteristics

- $T_a = -40$  to  $85^\circ\text{C}$

Item	Symbol	$V_{CC}$ (V) *	Min	Typ	Max	Unit	Test condition
Input voltage	$V_{IH}$	3.0 to 3.6	1.5	—	—	V	
		4.5 to 5.5	2.0	—	—		
	$V_{IL}$	3.0 to 3.6	—	—	0.6		
		4.5 to 5.5	—	—	0.8		
Hysteresis voltage	$V_H$	3.3	—	0.10	—	V	$V_{T^+} - V_{T^-}$
		5.0	—	0.15	—		
Output voltage	$V_{OH}$	Min to Max	$V_{CC}-0.1$	—	—	V	$I_{OH} = -50 \mu\text{A}$
		3.0	2.48	—	—		$I_{OH} = -6 \text{ mA}$
		4.5	3.8	—	—		$I_{OH} = -12 \text{ mA}$
	$V_{OL}$	Min to Max	—	—	0.1		$I_{OL} = 50 \mu\text{A}$
		3.0	—	—	0.44		$I_{OL} = 6 \text{ mA}$
		4.5	—	—	0.55		$I_{OL} = 12 \text{ mA}$
Input current	$I_{IN}$	0 to 5.5	—	—	$\pm 1$	$\mu\text{A}$	$V_{IN} = 5.5 \text{ V}$ or GND
Off state output current	$I_{OZ}$	Min to Max	—	—	$\pm 5$	$\mu\text{A}$	$V_O = 5.5 \text{ V}$ or GND
Quiescent supply current	$I_{CC}$	5.5	—	—	10	$\mu\text{A}$	$V_{IN} = V_{CC}$ or GND, $I_O = 0$
	$\Delta I_{CC}$	5.5	—	—	1.5	mA	One input $V_{IN} = 3.4 \text{ V}$ , other input $V_{CC}$ or GND
Output leakage current	$I_{OFF}$	0	—	—	5	$\mu\text{A}$	$V_O = 5.5 \text{ V}$
Input capacitance	$C_{IN}$	5.0	—	3.0	—	pF	$V_{IN} = V_{CC}$ or GND

Note: For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

## HD74LV2GT125A

### Switching Characteristics

- $V_{CC} = 3.3 \pm 0.3$  V

Item	Symbol	T <sub>a</sub> = 25°C			T <sub>a</sub> = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Propagation delay time	t <sub>PLH</sub>	—	4.5	9.0	1.0	10.5	ns	C <sub>L</sub> = 15 pF	A	Y
	t <sub>PHL</sub>	—	6.0	11.5	1.0	13.0		C <sub>L</sub> = 50 pF		
Enable time	t <sub>ZH</sub>	—	4.5	9.0	1.0	10.5	ns	C <sub>L</sub> = 15 pF	$\overline{OE}$	Y
	t <sub>ZL</sub>	—	6.0	11.5	1.0	13.0		C <sub>L</sub> = 50 pF		
Disable time	t <sub>HZ</sub>	—	4.0	10.0	1.0	11.5	ns	C <sub>L</sub> = 15 pF	$\overline{OE}$	Y
	t <sub>LZ</sub>	—	5.5	13.5	1.0	15.0		C <sub>L</sub> = 50 pF		

- $V_{CC} = 5.0 \pm 0.5$  V

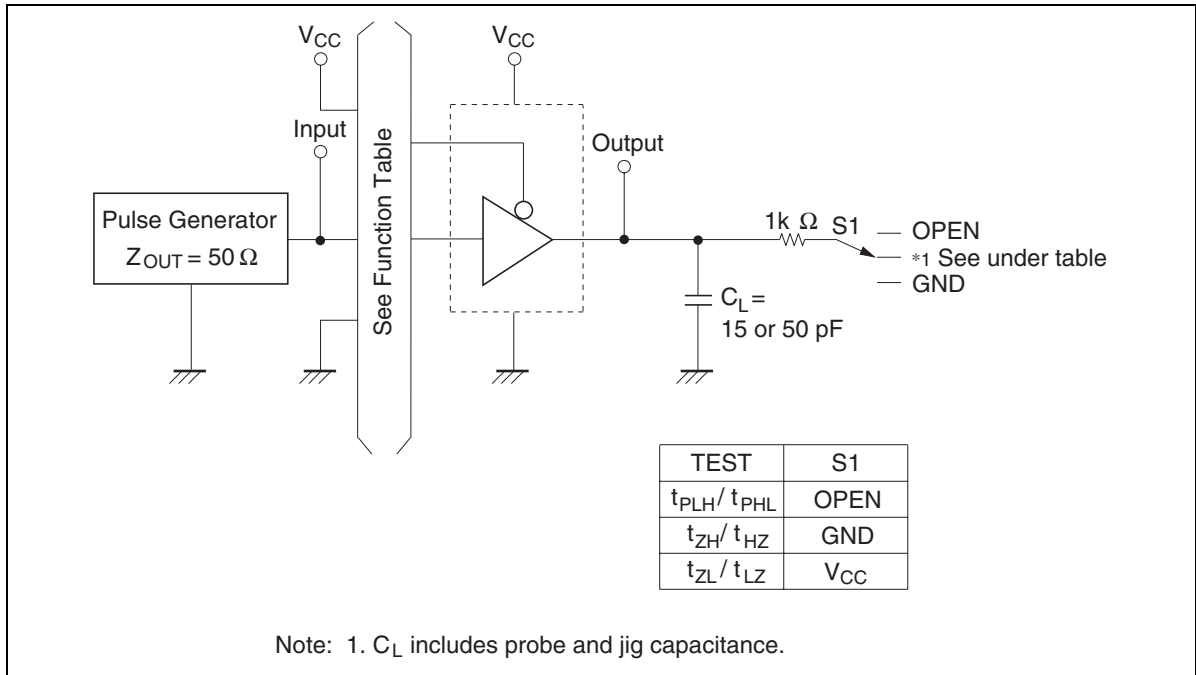
Item	Symbol	T <sub>a</sub> = 25°C			T <sub>a</sub> = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Propagation delay time	t <sub>PLH</sub>	—	3.4	5.5	1.0	6.5	ns	C <sub>L</sub> = 15 pF	A	Y
	t <sub>PHL</sub>	—	4.3	7.5	1.0	8.5		C <sub>L</sub> = 50 pF		
Enable time	t <sub>ZH</sub>	—	3.4	5.1	1.0	6.0	ns	C <sub>L</sub> = 15 pF	$\overline{OE}$	Y
	t <sub>ZL</sub>	—	4.4	7.1	1.0	8.0		C <sub>L</sub> = 50 pF		
Disable time	t <sub>HZ</sub>	—	3.2	6.8	1.0	8.0	ns	C <sub>L</sub> = 15 pF	$\overline{OE}$	Y
	t <sub>LZ</sub>	—	4.0	8.8	1.0	10.0		C <sub>L</sub> = 50 pF		

### Operating Characteristics

- C<sub>L</sub> = 50 pF

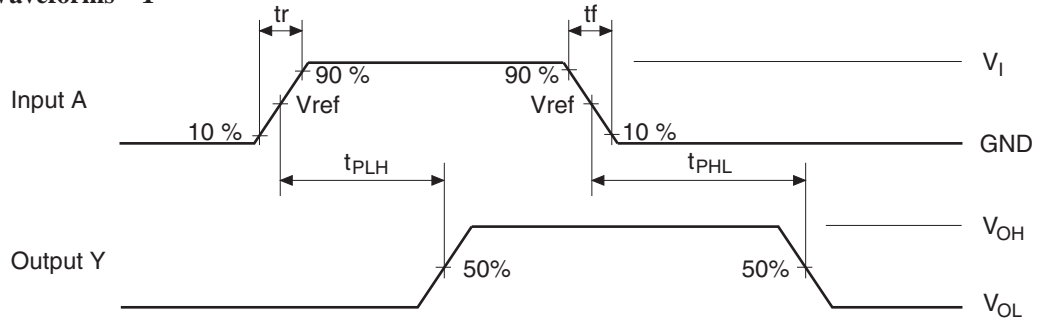
Item	Symbol	V <sub>CC</sub> (V)	T <sub>a</sub> = 25°C			Unit	Test Conditions
			Min	Typ	Max		
Power dissipation capacitance	C <sub>PD</sub>	5.0	—	11.5	—	pF	f = 10 MHz

Test Circuit

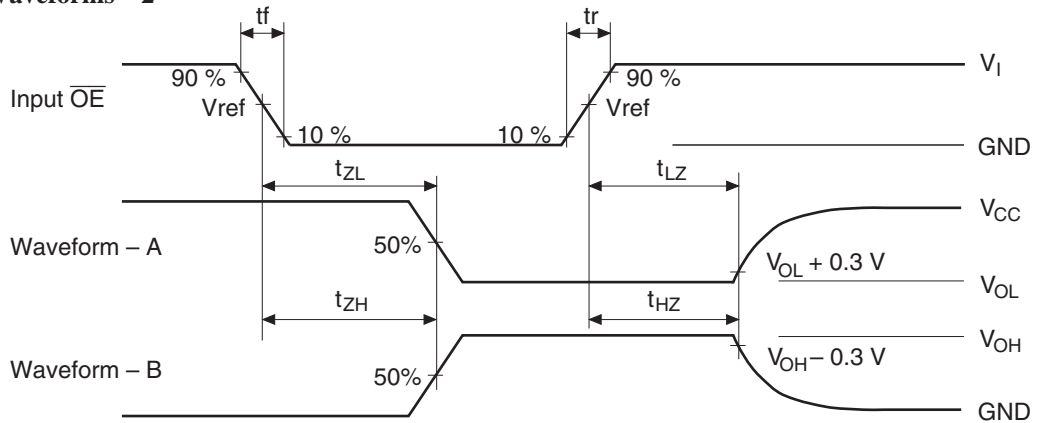




• Waveforms – 1



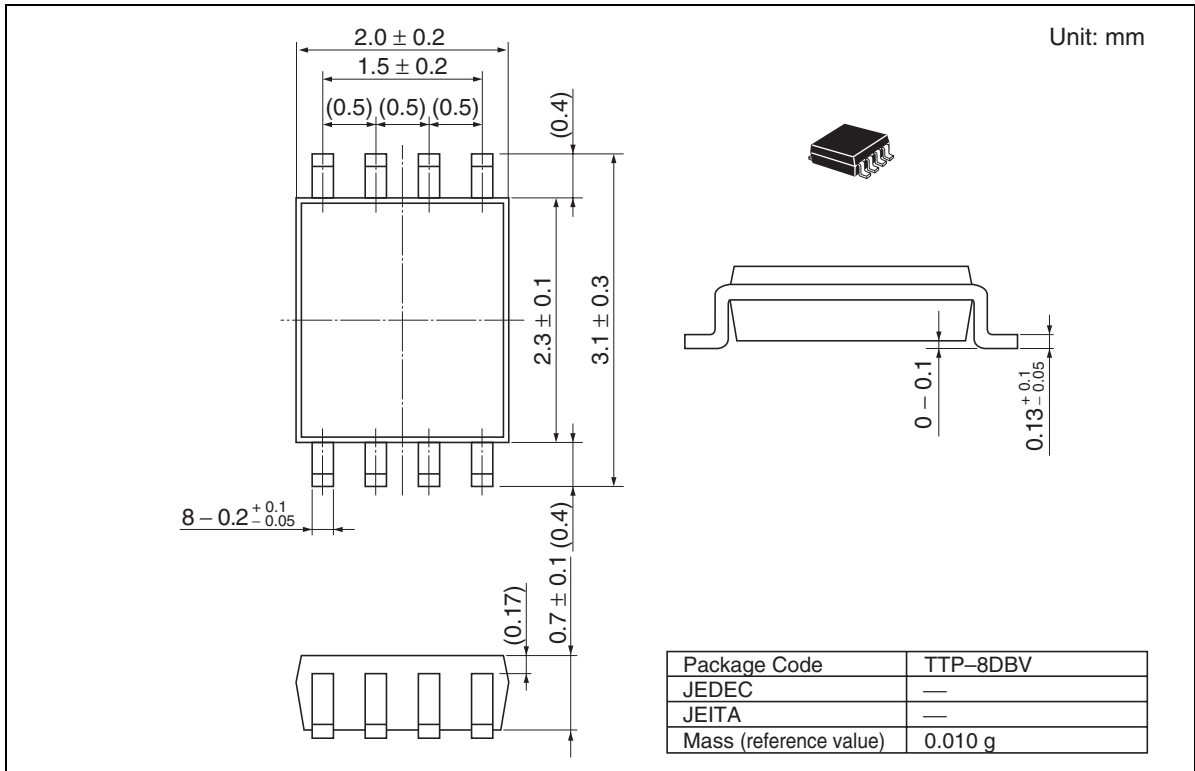
• Waveforms – 2



$V_{CC}$ (V)	INPUTS		Vref
	$V_I$	$t_r / t_f$	
3.3±0.3	2.5 V	≤ 3.0 ns	50%
5.0±0.5	3 V	≤ 3.0 ns	1.5 V

- Notes:
1. Input waveform : PRR ≤ 1 MHz,  $Z_o = 50 \Omega$ .
  2. Waveform – A is for an output with internal conditions such that the output is low except when disabled by the output control.
  3. Waveform – B is for an output with internal conditions such that the output is high except when disabled by the output control.

Package Dimensions



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