

## General Description

The 83904I-02 is a low skew, high performance 1-to-4 Crystal-to-LVCMOS Fanout Buffer. The 83904I-02 has selectable single-ended clock or two crystal-oscillator inputs. There is an output enable to disable the outputs by placing them into a high-impedance state.

Guaranteed output and part-to-part skew characteristics make the 83904I-02 ideal for those applications demanding well defined performance and repeatability.

## Features

- Four LVCMOS / LVTTL outputs, 19Ω output impedance at  $V_{DD} = V_{DDO} = 3.3V$
- Two crystal oscillator input pairs LVCMOS / LVTTL clock input
- Crystal input frequency range: 12MHz – 38.88MHz
- Output frequency: 200MHz (maximum)
- Output skew: 40ps (maximum) at  $V_{DD} = V_{DDO} = 3.3V$
- RMS phase jitter @ 25MHz output, using a 25MHz crystal, (100Hz – 1MHz): 0.16ps (typical) at  $V_{DD} = V_{DDO} = 3.3V$
- RMS phase noise at 25MHz

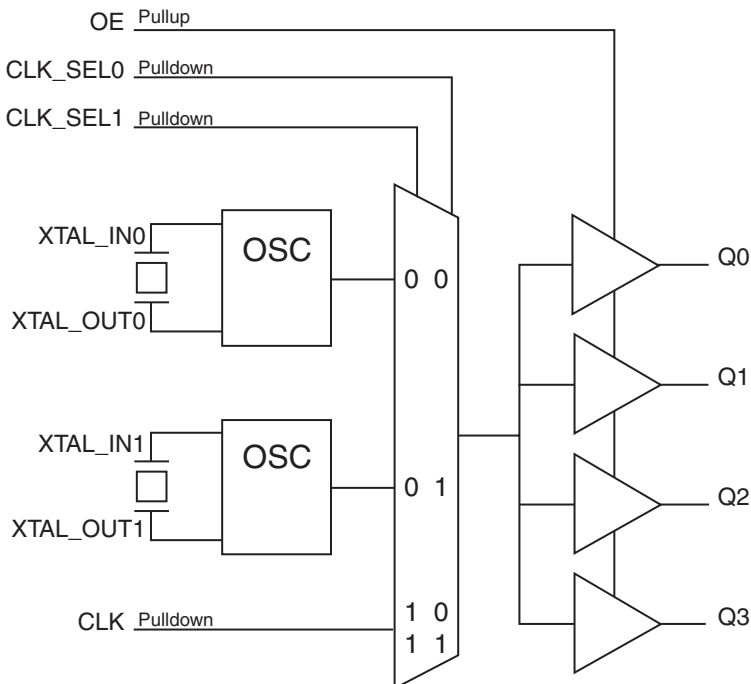
Offset	Noise Power
100Hz .....	-118.4 dBc/Hz
1kHz.....	-141.5 dBc/Hz
10kHz.....	-157.2 dBc/Hz
100kHz.....	-157.2 dBc/Hz

•Power Supply Voltage Modes:

Core / Output
3.3V / 3.3V
3.3V / 2.5V
3.3V / 1.8V
2.5V / 2.5V
2.5V / 1.8V

- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) packaging

## Block Diagram



## Pin Assignment

CLK_SEL0	1	16	VDDO
XTAL_OUT0	2	15	Q0
XTAL_IN0	3	14	Q1
VDD	4	13	GND
XTAL_IN1	5	12	Q2
XTAL_OUT1	6	11	Q3
CLK_SEL1	7	10	VDDO
CLK	8	9	OE

**83904I-02**

**16-Lead TSSOP**

**4.4mm x 5.0mm x 0.92mm package body**

**G Package**

**Top View**

## Pin Descriptions and Pin Characteristics

**Table 1. Pin Descriptions**

Number	Name	Type		Description
1, 7	CLK_SEL0, CLK_SEL1	Input	Pulldown	Clock select inputs. See Table 3, <i>Input Reference Function Table</i> . LVCMOS/LVTTL interface levels.
2, 3	XTAL_OUT0, XTAL_IN0	Input		Crystal oscillator interface. XTAL_IN0 is the input. XTAL_OUT0 is the output.
4	V <sub>DD</sub>	Power		Power supply pin.
5, 6	XTAL_IN1, XTAL_OUT1	Input		Crystal oscillator interface. XTAL_IN1 is the input. XTAL_OUT1 is the output.
8	CLK	Input	Pulldown	Single-ended clock input. LVCMOS/LVTTL interface levels.
9	OE	Input	Pullup	Output enable pin. When LOW, outputs are in high-impedance state. When HIGH, outputs are active. LVCMOS/LVTTL interface levels.
10, 16	V <sub>DDO</sub>	Power		Output supply pins.
11, 12, 14, 15	Q3, Q2, Q1, Q0	Output		Single-ended clock outputs. LVCMOS/LVTTL interface levels.
13	GND	Power		Power supply ground.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

**Table 2. Pin Characteristics**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
R <sub>PULLUP</sub>	Input Pullup Resistor			51		kΩ
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			51		kΩ
C <sub>PD</sub>	Power Dissipation Capacitance (per output)	V <sub>DDO</sub> = 3.465V		8		pF
		V <sub>DDO</sub> = 2.625V		7		pF
		V <sub>DDO</sub> = 2.0V		7		pF
R <sub>OUT</sub>	Output Impedance	V <sub>DDO</sub> = 3.3V		19		Ω
		V <sub>DDO</sub> = 2.5V		21		Ω
		V <sub>DDO</sub> = 1.8V		32		Ω

## Function Table

**Table 3. Input Reference Function Table**

Control Inputs		Reference
CLK_SEL1	CLK_SEL0	
0	0	XTAL0 (default)
0	1	XTAL1
1	0	CLK
1	1	CLK

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, $V_{DD}$	4.6V
Inputs, $V_I$	-0.5V to $V_{DD} + 0.5V$
Outputs, $V_O$	-0.5V to $V_{DDO} + 0.5V$
Package Thermal Impedance, $\theta_{JA}$	100.3°C/W (0 mps)
Storage Temperature, $T_{STG}$	-65°C to 150°C

## DC Electrical Characteristics

**Table 4A. Power Supply DC Characteristics,  $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Power Supply Voltage		3.135	3.3	3.465	V
$V_{DDO}$	Output Supply Voltage		3.135	3.3	3.465	V
$I_{DD}$	Power Supply Current	No Load & XTALx selected @ 12MHz			7	mA
		No Load & CLK selected			1	mA
$I_{DDO}$	Output Supply Current	No Load & CLK selected			1	mA

**Table 4B. Power Supply DC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Power Supply Voltage		3.135	3.3	3.465	V
$V_{DDO}$	Output Supply Voltage		2.375	2.5	2.625	V
$I_{DD}$	Power Supply Current	No Load & XTALx selected @ 12MHz			7	mA
		No Load & CLK selected			1	mA
$I_{DDO}$	Output Supply Current	No Load & CLK selected			1	mA

**Table 4C. Power Supply DC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Power Supply Voltage		3.135	3.3	3.465	V
$V_{DDO}$	Output Supply Voltage		1.6	1.8	2.0	V
$I_{DD}$	Power Supply Current	No Load & XTALx selected @ 12MHz			7	mA
		No Load & CLK selected			1	mA
$I_{DDO}$	Output Supply Current	No Load & CLK selected			1	mA

**Table 4D. Power Supply DC Characteristics,  $V_{DD} = V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Power Supply Voltage		2.375	2.5	2.625	V
$V_{DDO}$	Output Supply Voltage		2.375	2.5	2.625	V
$I_{DD}$	Power Supply Current	No Load & XTALx selected @ 12MHz			3	mA
		No Load & CLK selected			1	mA
$I_{DDO}$	Output Supply Current	No Load & CLK selected			1	mA

**Table 4E. Power Supply DC Characteristics,  $V_{DD} = 2.5V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Power Supply Voltage		2.375	2.5	2.625	V
$V_{DDO}$	Output Supply Voltage		1.6	1.8	2.0	V
$I_{DD}$	Power Supply Current	No Load & XTALx selected @ 12MHz			3	mA
		No Load & CLK selected			1	mA
$I_{DDO}$	Output Supply Current	No Load & CLK selected			1	mA

**Table 4F. LVCMOS/LVTTL DC Characteristics,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage	$V_{DD} = 3.3V \pm 5\%$	2.2		$V_{DD} + 0.3$	V
		$V_{DD} = 2.5V \pm 5\%$	1.6		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage	$V_{DD} = 3.3V \pm 5\%$	-0.3		1.3	V
		$V_{DD} = 2.5V \pm 5\%$	-0.3		0.9	V
$I_{IH}$	Input High Current	CLK, CLK_SEL[0:1] $V_{DD} = V_{IN} = 3.3V$ or $2.5V \pm 5\%$			150	$\mu\text{A}$
		OE $V_{DD} = V_{IN} = 3.3V$ or $2.5V \pm 5\%$			5	$\mu\text{A}$
$I_{IL}$	Input Low Current	CLK, CLK_SEL[0:1] $V_{DD} = 3.3V$ or $2.5V \pm 5\%$ , $V_{IN} = 0V$	-5			$\mu\text{A}$
		OE $V_{DD} = 3.3V$ or $2.5V \pm 5\%$ , $V_{IN} = 0V$	-150			$\mu\text{A}$
$V_{OH}$	Output High Voltage; NOTE 1	$V_{DDO} = 3.3V \pm 5\%$	2.6			V
		$V_{DDO} = 2.5V \pm 5\%$	1.8			V
		$V_{DDO} = 1.8V \pm 0.2V$	1.2			V
$V_{OL}$	Output Low Voltage; NOTE 1	$V_{DDO} = 3.3V \pm 5\%$			0.6	V
		$V_{DDO} = 2.5V \pm 5\%$			0.5	V
		$V_{DDO} = 1.8V \pm 0.2V$			0.4	V

 NOTE: Outputs terminated with  $50\Omega$  to  $V_{DDO}/2$ . See Parameter Measurement section, *Load Test Circuit diagram*.

**Table 5. Crystal Characteristics**

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		12		38.88	MHz
Equivalent Series Resistance (ESR)				50	$\Omega$
Shunt Capacitance				7	pF
Drive Level				1	mW

## AC Electrical Characteristics

**Table 6A. AC Characteristics,  $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$** 

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency	w/external XTAL	12		38.88	MHz
		w/external CLK			200	MHz
$t_{PLH}$	Propagation Delay, Low to High; NOTE 1		1.4	1.9	2.4	ns
$t_{sk(o)}$	Output Skew; NOTE 2, 5				40	ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 3, 5				700	ps
$f_{jit(\theta)}$	RMS Phase Jitter, Random; 4, 5		25MHz, Integration Range: 100MHz – 1MHz		0.16	ps
$t_R / t_F$	Output Rise/Fall Time		20% to 80%		100	ps
odc	Output Duty Cycle	w/external XTAL	45		55	%
		w/external CLK	$f < 150\text{MHz}$		46	54
$t_{EN}$	Output Enable Time; NOTE 6				10	ns
$t_{DIS}$	Output Disable Time; NOTE 6				10	ns

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: Measured from the  $V_{DD}/2$  of the input to  $V_{DDO}/2$  of the output.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at  $V_{DDO}/2$ .

NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltage, same frequency, same temperature and with equal load conditions. Using the same type of input on each device, the output is measured at  $V_{DDO}/2$ .

NOTE 4: Phase jitter is dependent on the input source used.

NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 6: These parameters are guaranteed by characterization. Not tested in production.

**Table 6B. AC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency	w/external XTAL	12		38.88	MHz
		w/external CLK			200	MHz
$t_{PLH}$	Propagation Delay, Low to High; NOTE 1		1.5	2.0	2.5	ns
$t_{sk(o)}$	Output Skew; NOTE 2, 5				40	ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 3, 5				700	ps
$f_{jit(\theta)}$	RMS Phase Jitter, Random; 4, 5	25MHz, Integration Range: 100MHz – 1MHz		0.16		ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	100		800	ps
odc	Output Duty Cycle	w/external XTAL	45		55	%
		w/external CLK	$f < 150MHz$	46		54
$t_{EN}$	Output Enable Time; NOTE 6				10	ns
$t_{DIS}$	Output Disable Time; NOTE 6				10	ns

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: Measured from the  $V_{DD}/2$  of the input to  $V_{DDO}/2$  of the output.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at  $V_{DDO}/2$ .

NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltage, same frequency, same temperature and with equal load conditions. Using the same type of input on each device, the output is measured at  $V_{DDO}/2$ .

NOTE 4: Phase jitter is dependent on the input source used.

NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 6: These parameters are guaranteed by characterization. Not tested in production.

**Table 6C. AC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency	w/external XTAL	12		38.88	MHz
		w/external CLK			200	MHz
$t_{PLH}$	Propagation Delay, Low to High; NOTE 1		1.7	2.2	2.7	ns
$t_{sk(o)}$	Output Skew; NOTE 2, 5				40	ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 3, 5				700	ps
$f_{jit(\theta)}$	RMS Phase Jitter, Random; 4, 5	25MHz, Integration Range: 100MHz – 1MHz		0.16		ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	100		1000	ps
odc	Output Duty Cycle	w/external XTAL	45		55	%
		w/external CLK	$f < 150MHz$	46		54
$t_{EN}$	Output Enable Time; NOTE 6				10	ns
$t_{DIS}$	Output Disable Time; NOTE 6				10	ns

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: Measured from the  $V_{DD}/2$  of the input to  $V_{DDO}/2$  of the output.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at  $V_{DDO}/2$ .

NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltage, same frequency, same temperature and with equal load conditions. Using the same type of input on each device, the output is measured at  $V_{DDO}/2$ .

NOTE 4: Phase jitter is dependent on the input source used.

NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 6: These parameters are guaranteed by characterization. Not tested in production.

**Table 6D. AC Characteristics,  $V_{DD} = V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency	w/external XTAL	12		38.88	MHz
		w/external CLK			200	MHz
$t_{PLH}$	Propagation Delay, Low to High; NOTE 1		1.5	2.2	3.0	ns
$t_{sk(o)}$	Output Skew; NOTE 2, 5				40	ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 3, 5				700	ps
$f_{jit(\theta)}$	RMS Phase Jitter, Random; 4, 5	25MHz, Integration Range: 100MHz – 1MHz		0.20		ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	100		800	ps
odc	Output Duty Cycle	w/external XTAL	45		55	%
		w/external CLK	46		54	%
$t_{EN}$	Output Enable Time; NOTE 6				10	ns
$t_{DIS}$	Output Disable Time; NOTE 6				10	ns

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: Measured from the  $V_{DD}/2$  of the input to  $V_{DDO}/2$  of the output.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at  $V_{DDO}/2$ .

NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltage, same frequency, same temperature and with equal load conditions. Using the same type of input on each device, the output is measured at  $V_{DDO}/2$ .

NOTE 4: Phase jitter is dependent on the input source used.

NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 6: These parameters are guaranteed by characterization. Not tested in production.

**Table 6E. AC Characteristics,  $V_{DD} = 2.5V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency	w/external XTAL	12		38.88	MHz
		w/external CLK			200	MHz
$t_{PLH}$	Propagation Delay, Low to High; NOTE 1		1.7	2.5	3.3	ns
$t_{sk(o)}$	Output Skew; NOTE 2, 5				40	ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 3, 5				700	ps
$f_{jit(\theta)}$	RMS Phase Jitter, Random; 4, 5	25MHz, Integration Range: 100MHz – 1MHz		0.19		ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	100		1000	ps
odc	Output Duty Cycle	w/external XTAL	45		55	%
		w/external CLK	46		54	%
$t_{EN}$	Output Enable Time; NOTE 6				10	ns
$t_{DIS}$	Output Disable Time; NOTE 6				10	ns

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: Measured from the  $V_{DD}/2$  of the input to  $V_{DDO}/2$  of the output.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at  $V_{DDO}/2$ .

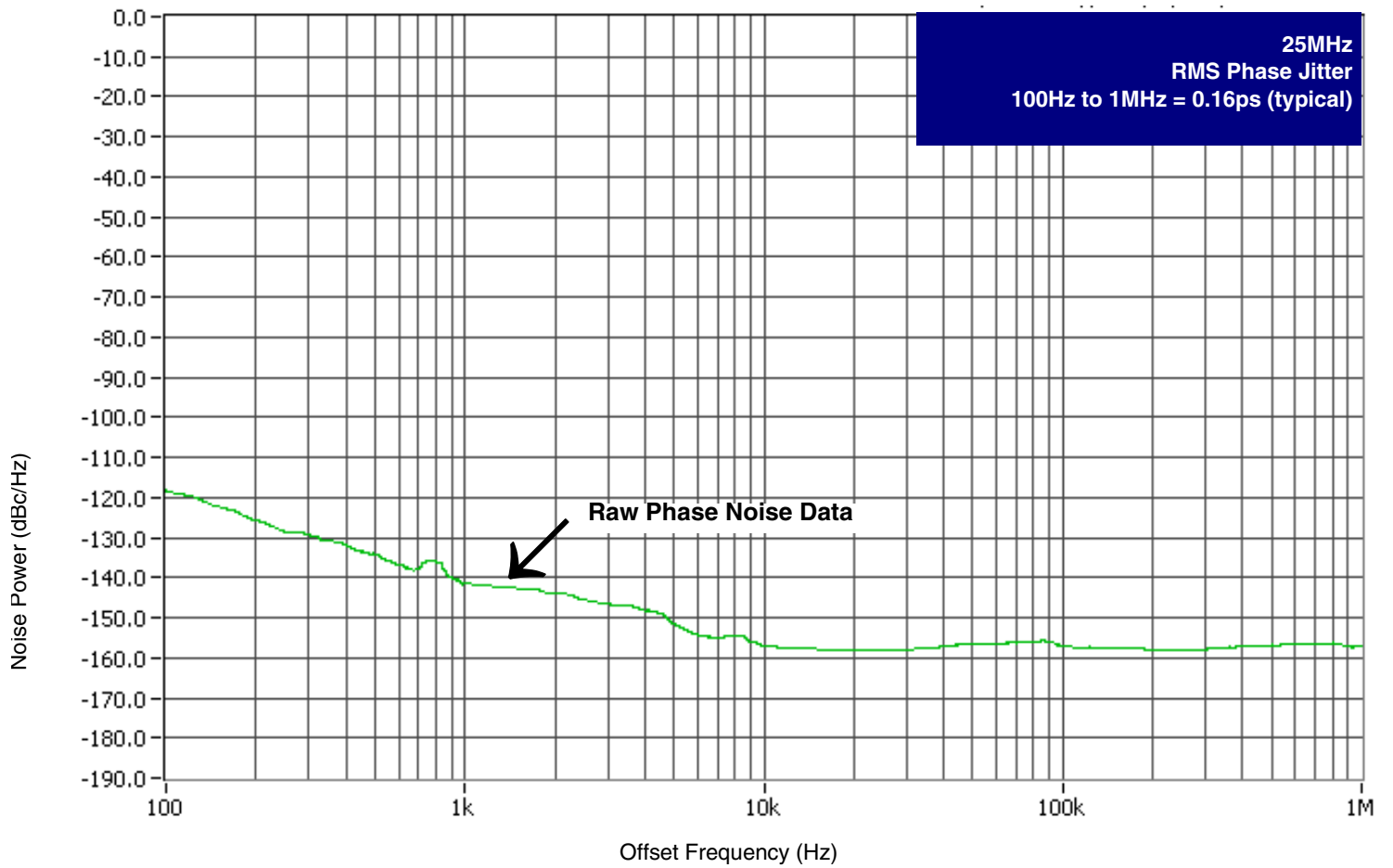
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltage, same frequency, same temperature and with equal load conditions. Using the same type of input on each device, the output is measured at  $V_{DDO}/2$ .

NOTE 4: Phase jitter is dependent on the input source used.

NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

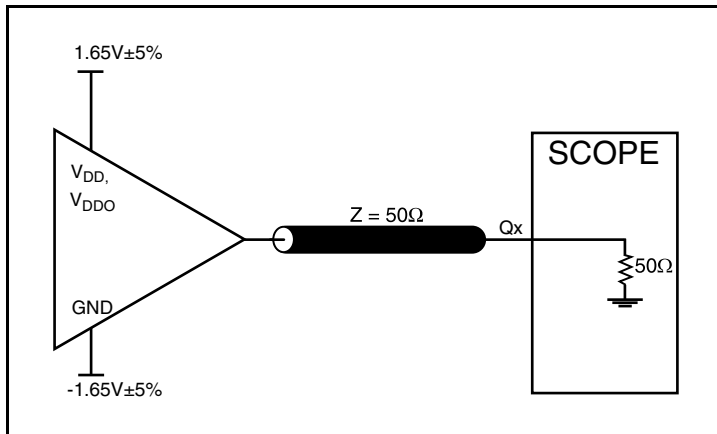
NOTE 6: These parameters are guaranteed by characterization. Not tested in production.

### Typical Phase Noise at 25MHz, 100Hz - 1MHz

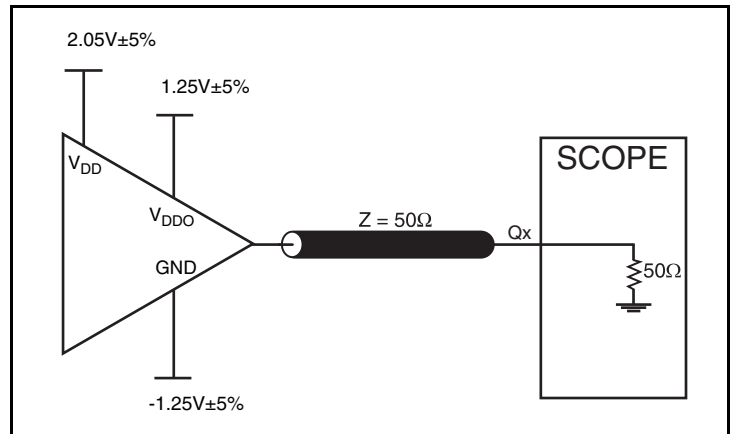




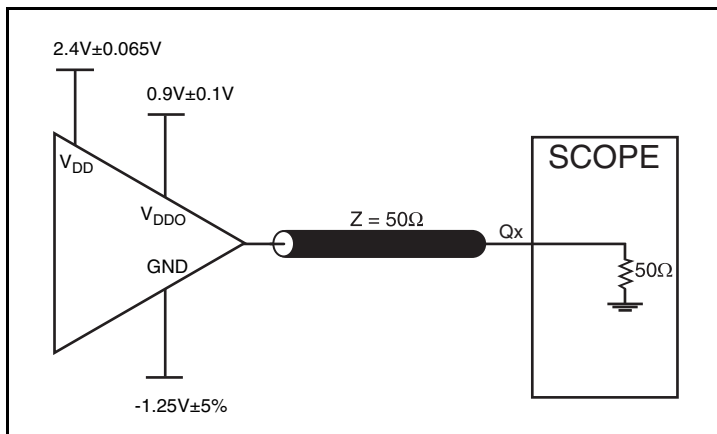
### Parameter Measurement Information



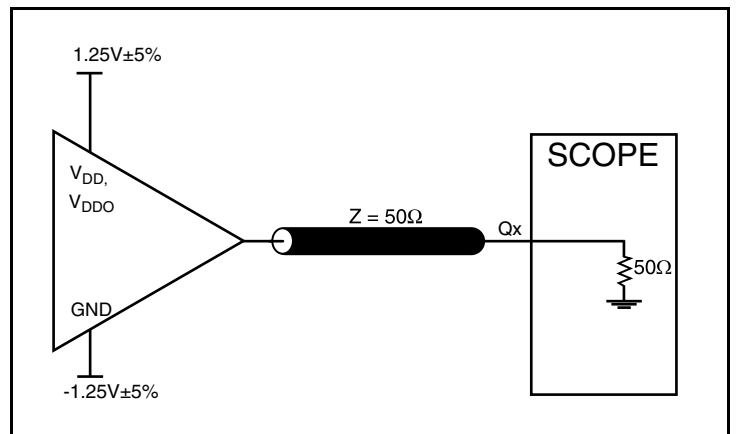
**3.3V Core/3.3V LVCMOS Output Load Test Circuit**



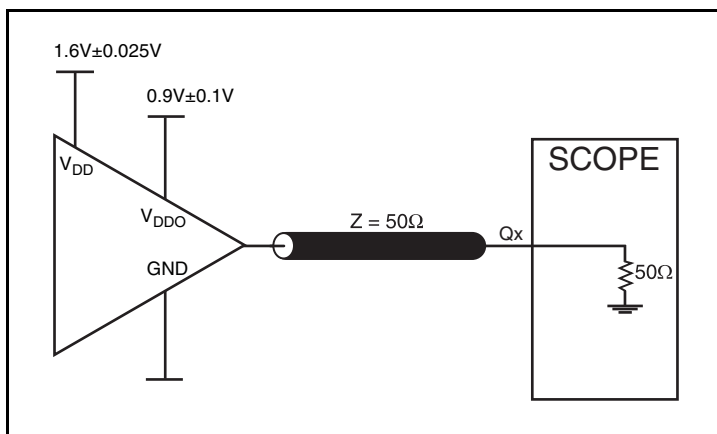
**3.3V Core/2.5V LVCMOS Output Load Test Circuit**



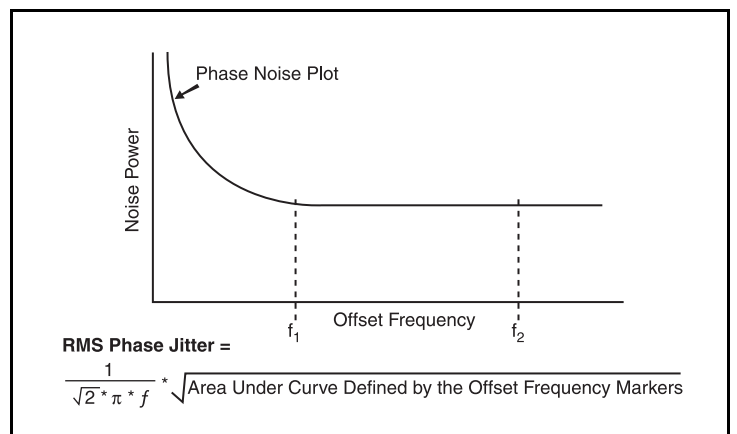
**3.3V Core/1.8V LVCMOS Output Load Test Circuit**



**2.5V Core/2.5V LVCMOS Output Load Test Circuit**

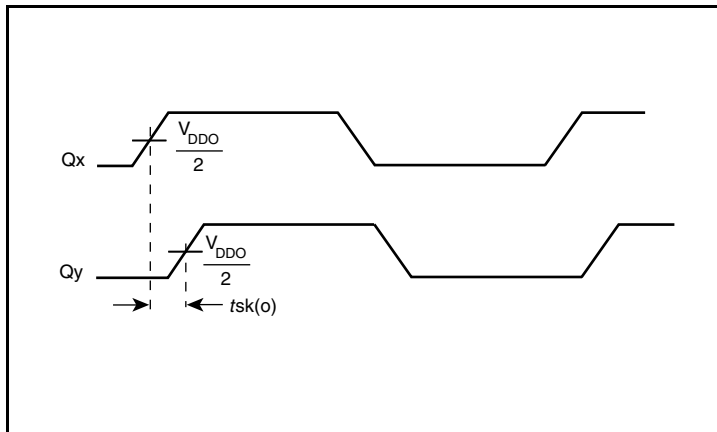


**2.5V Core/1.8V LVCMOS Output Load Test Circuit**

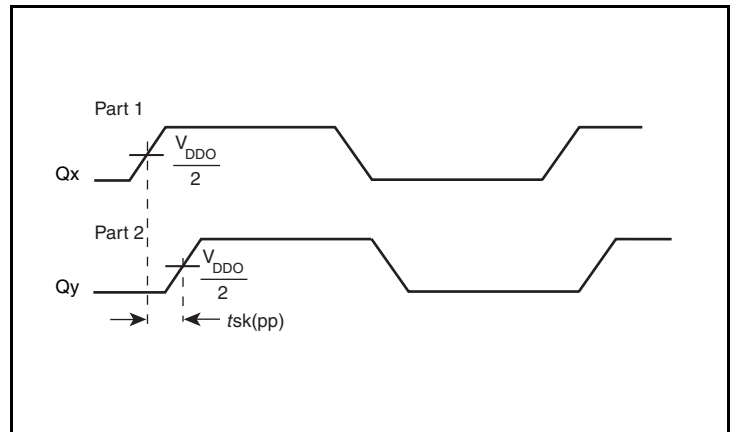


**RMS Phase Jitter**

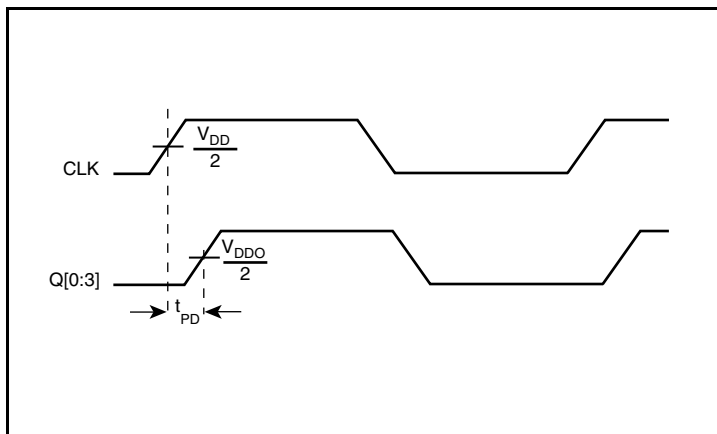
## Parameter Measurement Information, continued



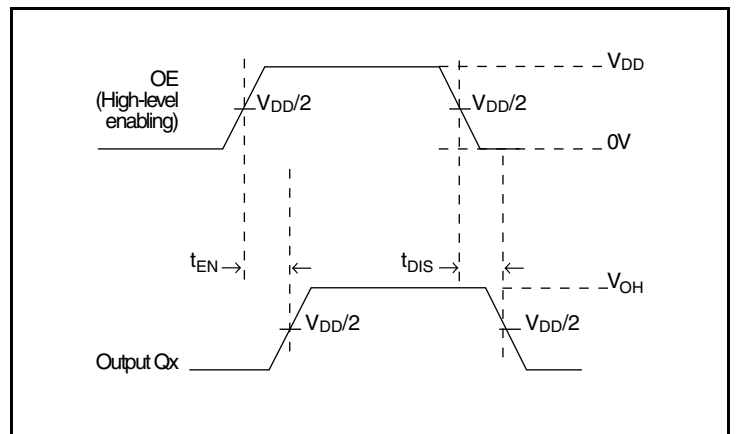
**Output Skew**



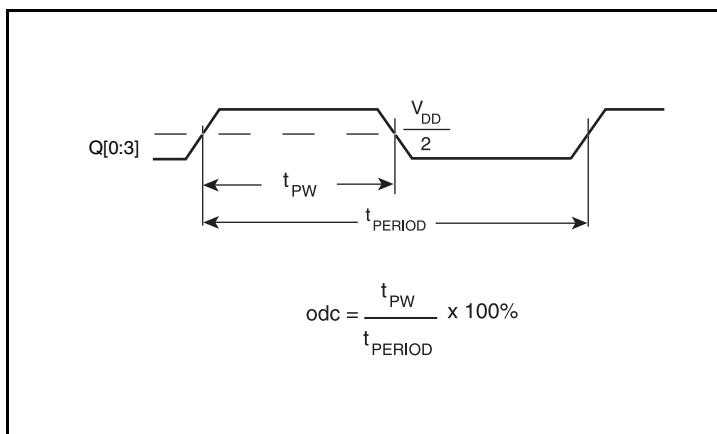
**Part-to-Part Skew**



**Propagation Delay**



**Output Enable/Disable Time**



**Output Duty Cycle/Pulse Width/Period**



**Output Rise/Fall Time**

## Applications Information

### Recommendations for Unused Input and Output Pins

#### Inputs:

##### Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL\_IN and XTAL\_OUT can be left floating. Though not required, but for additional protection, a  $1\text{k}\Omega$  resistor can be tied from XTAL\_IN to ground.

##### CLK Input

For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a  $1\text{k}\Omega$  resistor can be tied from the CLK input to ground.

##### LVC MOS Control Pins

All control pins have internal pullup and pulldown resistors; additional resistance is not required but can be added for additional protection. A  $1\text{k}\Omega$  resistor can be used.

#### Outputs:

##### LVC MOS Outputs

All unused LVC MOS outputs can be left floating. There should be no trace attached.

### Crystal Input Interface

Figure 1 shows an example of 83904I-02 crystal interface with a parallel resonant crystal. The frequency accuracy can be fine tuned by adjusting the C1 and C2 values. For a parallel crystal with loading capacitance  $C_L = 18\text{pF}$ , we suggest  $C_1 = 15\text{pF}$  and  $C_2 = 15\text{pF}$  to start with. These values may be slightly fine tuned further to optimize the frequency accuracy for different board layouts. Slightly increasing the C1 and C2 values will slightly reduce the frequency. Slightly decreasing the C1 and C2 values will slightly increase the frequency. For the oscillator circuit below, R1 can be used, but is not required. For new designs, it is recommended that R1 not be used.

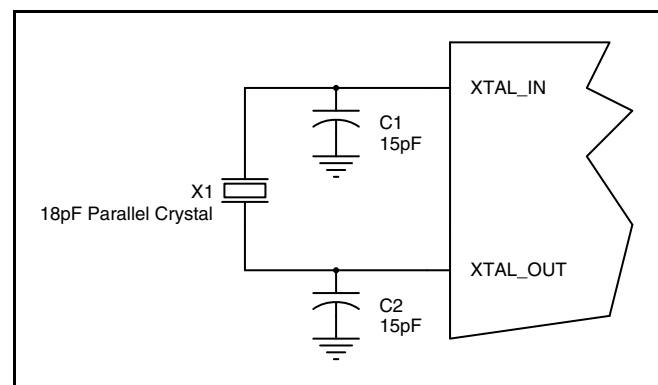


Figure 1. Crystal Input Interface

## Overdriving the XTAL Interface

The XTAL\_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL\_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/nS. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. *Figure 2A* shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver ( $R_o$ ) and the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This

can be done in one of two ways. First,  $R_1$  and  $R_2$  in parallel should equal the transmission line impedance. For most 50Ω applications,  $R_1$  and  $R_2$  can be 100Ω. This can also be accomplished by removing  $R_1$  and changing  $R_2$  to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. *Figure 2B* shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL\_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

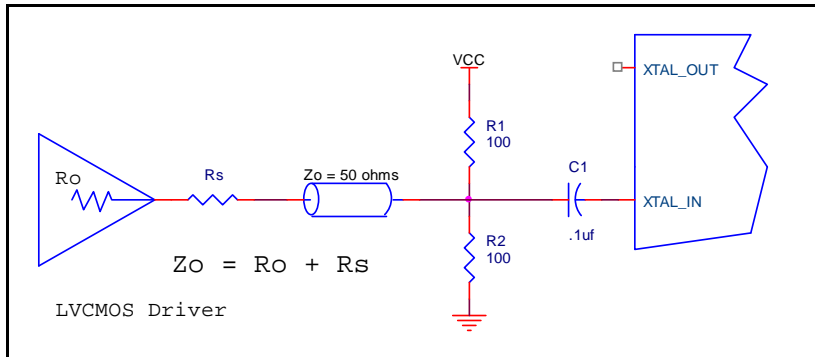


Figure 2A. General Diagram for LVCMOS Driver to XTAL Input Interface

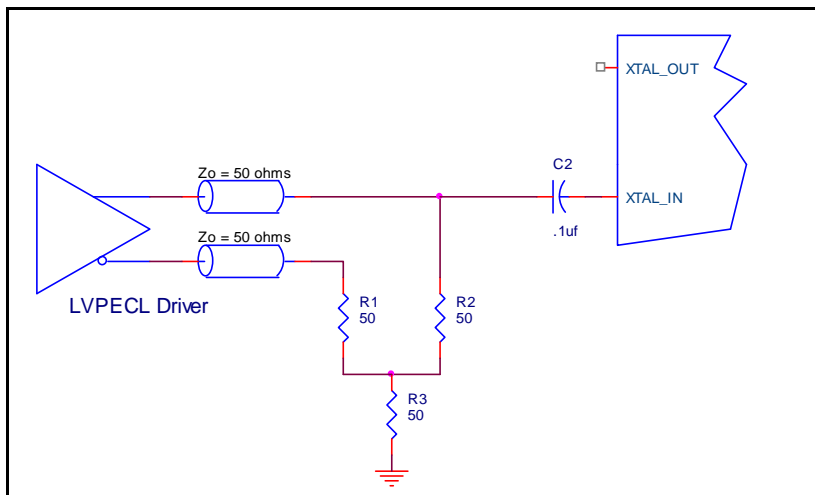


Figure 2B. General Diagram for LVPECL Driver to XTAL Input Interface

## Reliability Information

Table 7.  $\theta_{JA}$  vs. Air Flow Table for a 16 Lead TSSOP

$\theta_{JA}$ vs. Air Flow			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	100.3°C/W	96.0°C/W	93.9°C/W

## Transistor Count

The transistor count for 839041-02: 205

## Package Outline and Package Dimensions

Package Outline - G Suffix for 16 Lead TSSOP

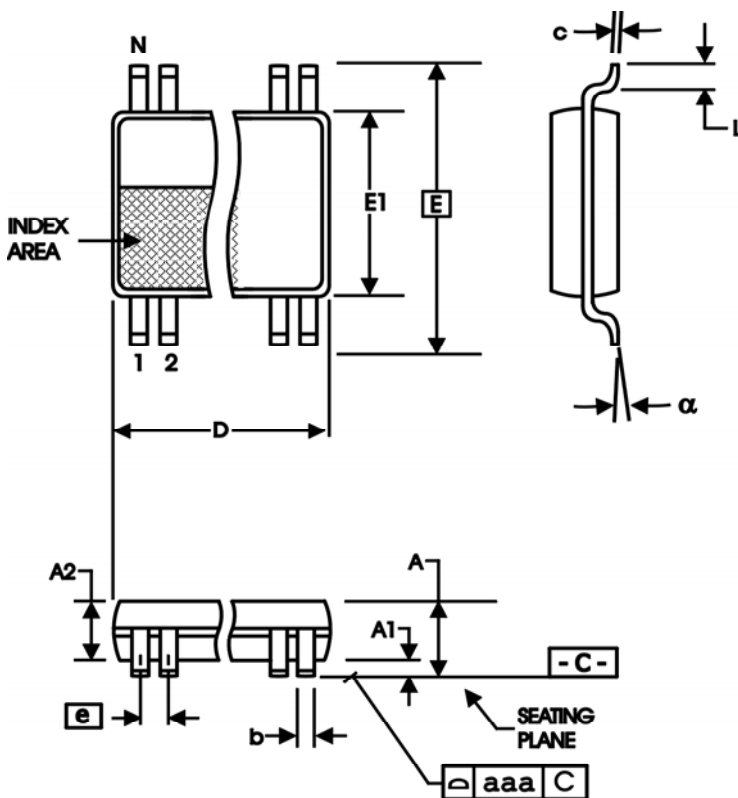


Table 8. Package Dimensions for 16 Lead TSSOP

All Dimensions in Millimeters		
Symbol	Minimum	Maximum
N	16	
A		1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
$\alpha$	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

## Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
83904AGI-02LF	904AI02L	"Lead-Free" 16 Lead TSSOP	Tube	-40°C to 85°C
83904AGI-02LFT	904AI02L	"Lead-Free" 16 Lead TSSOP	Tape & Reel	-40°C to 85°C

## Revision History Sheet

Rev	Table	Page	Description of Change	Date
B			Deleted "ICS" prefix from part number throughout the datasheet. Updated datasheet header/footer.	4/8/16



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