FemtoClock™ Crystal-to-LVCMOS/LVTTL Clock Generator

ICS840021I

DATA SHEET

General Description

The ICS840021I is a Gigabit Ethernet Clock Generator. The ICS840021I uses a 25MHz crystal to synthesize 125MHz. The ICS840021I has excellent phase jitter performance, over the 1.875MHz – 20MHz integration range. The ICS840021I is packaged in a small 8-pin TSSOP and 16-pin VFQFN, making it ideal for use in systems with limited board space.

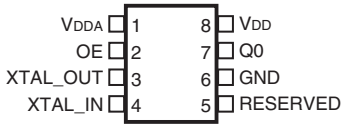
Features

- One LVCMOS/LVTTL output, 15Ω output impedance
- Crystal oscillator interface designed for 25MHz, 18pF parallel resonant crystal
- Output frequency: 125MHz
- VCO range: 560MHz to 680MHz
- RMS phase jitter @ 125MHz, using a 25MHz crystal (1.875MHz - 20MHz): 0.48ps (typical) 3.3V
- RMS phase noise at 125MHz (typical)
- Phase noise:

Offset	Noise Power
100Hz	-97.8 dBc/Hz
1kHz	-124.6 dBc/Hz
10kHz	-132.5 dBc/Hz
100Hz	-131.1 dBc/Hz

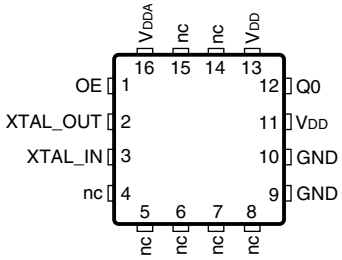
- Voltage Supply Modes:
  V_{DD}/V_{DDA} = 3.3V
  V_{DD}/V_{DDA} = 2.5V
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Pin Assignments



ICS840021I

8-Lead TSSOP
4.40mm x 3.0mm x 0.925mm package body
G Package
Top View



ICS840021I

16-Lead VFQFN
3.0mm x 3.0mm x 0.925mm package body
K Package
Top View

Block Diagram

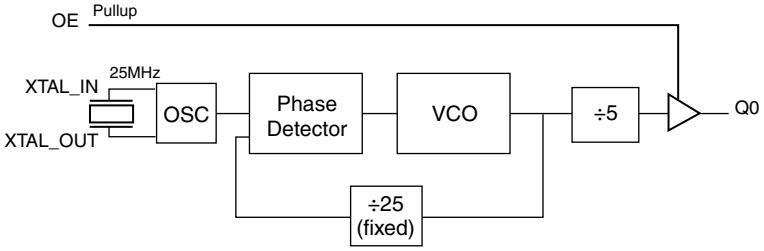


Table 1. Pin Descriptions

Name	Type		Description
V_{DDA}	Power		Analog supply pin.
OE	Input	Pullup	Output enable pin. When HIGH, Q0 output is enabled. When LOW, forces Q0 to high-impedance state. LVCMOS/LVTTL interface levels.
XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
nc	Unused		No connect.
RESERVED	Reserved		Reserved pin.
GND	Power		Power supply ground.
Q0	Output		Single-ended clock output. LVCMOS/LVTTL interface levels. 15Ω output impedance.
V_{DD}	Power		Core supply pin.

NOTE: *Pullup* refers to internal input resistors. See Table 1, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
C_{PD}	Power Dissipation Capacitance	V_{DD} = 3.465V		7		pF
		V_{DD} = 2.625V		7		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
R_{OUT}	Output Impedance			15		Ω

Function Table

Table 3. Control Function Table

Control Input	Output
OE	**Q0**
0	High-Impedance
1	Active

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA} 8 TSSOP 16 VFQFN	 101.7°C/W (0 mps) 74.9°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				65	mA
I_{DDA}	Analog Supply Current				10	mA

Table 4B. Power Supply DC Characteristics, V_{DD} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDA}	Analog Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				60	mA
I_{DDA}	Analog Supply Current				10	mA

Table 4C. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V ± 5% OR 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.3V	2		V_{DD} + 0.3	V
			V_{DD} = 2.5V	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.3V	-0.3		0.8	V
			V_{DD} = 2.5V	-0.3		0.7	V
I_{IH}	Input High Current	OE	V_{DD} = V_{IN} = 3.465V OR 2.625V			5	µA
I_{IL}	Input Low Current	OE	V_{DD} =3.465V OR 2.625V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage; NOTE 1		V_{DD} = 3.465V	2.6			V
			V_{DD} = 2.625V	1.8			V
V_{OL}	Output High Voltage; NOTE 1		V_{DD} = 3.465V OR 2.625V			0.5	V

NOTE 1: Outputs terminated with 50Ω to V_{DD}/2. See Parameter Measurement Information Section, "3.3V Output Load Test Circuit" diagrams.

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

AC Electrical Characteristics

Table 6A. AC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency			125		MHz
$t_{jit}(Ø)$	RMS Phase Jitter, Random; NOTE 1	Integration Range: 1.875MHz – 20MHz		0.48		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		500	ps
odc	Output Duty Cycle		48		52	%

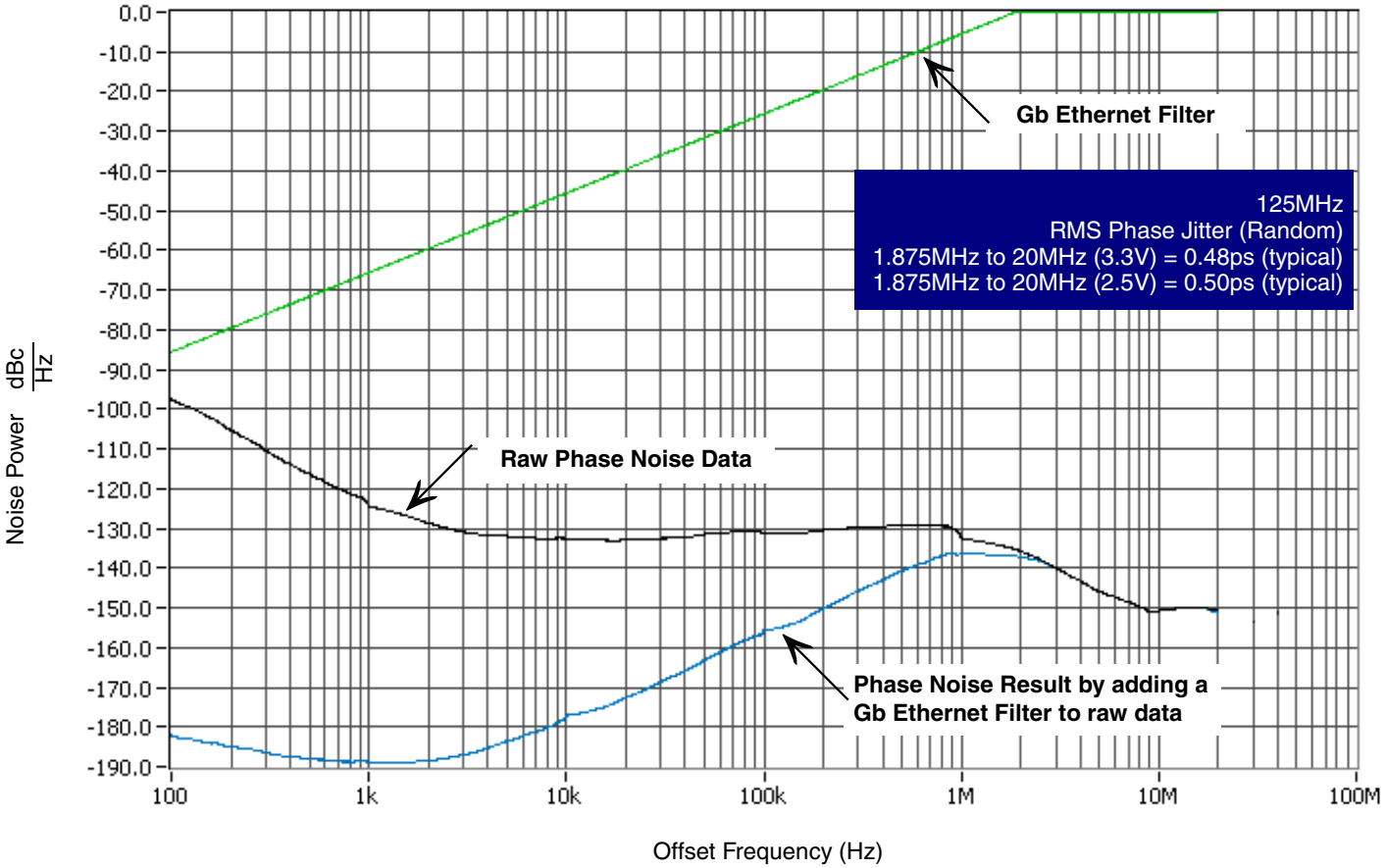
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Please refer to Phase Noise Plots.

Table 6B. AC Characteristics, V_{DD} = 2.5V ± 5%, T_A = -40°C to 85°C

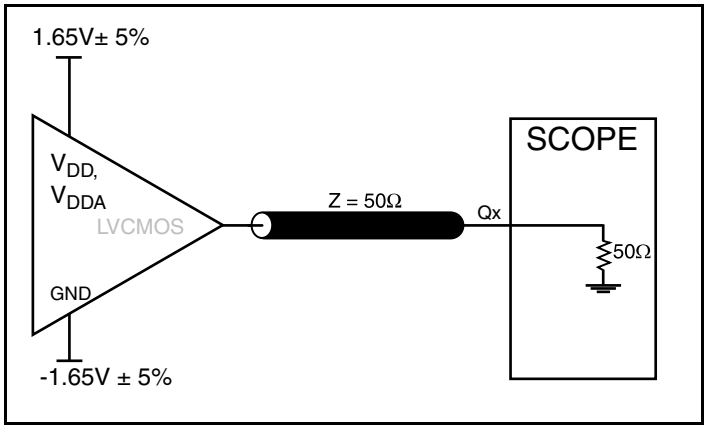
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency			125		MHz
$t_{jit}(Ø)$	RMS Phase Jitter, Random; NOTE 1	Integration Range: 1.875MHz – 20MHz		0.50		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	250		550	ps
odc	Output Duty Cycle		48		52	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Please refer to Phase Noise Plots.

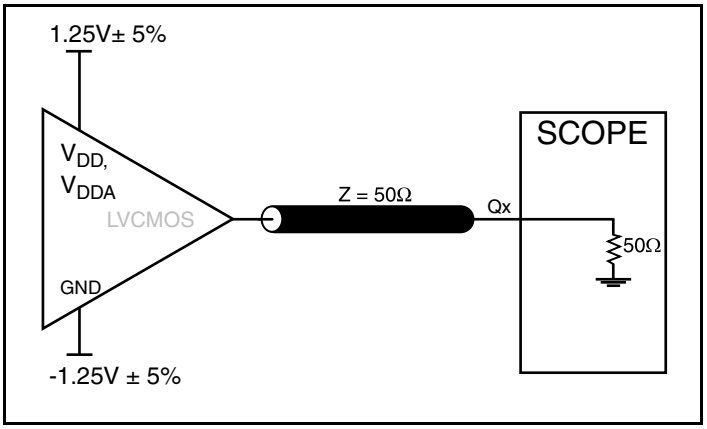
Typical Phase Noise at 125MHz (3.3V OR 2.5V)



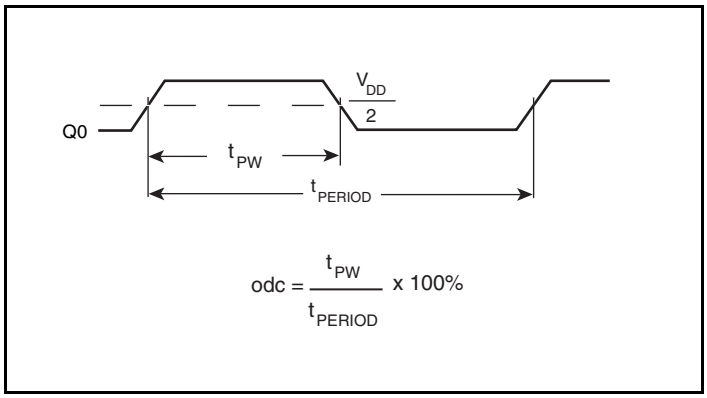
Parameter Measurement Information



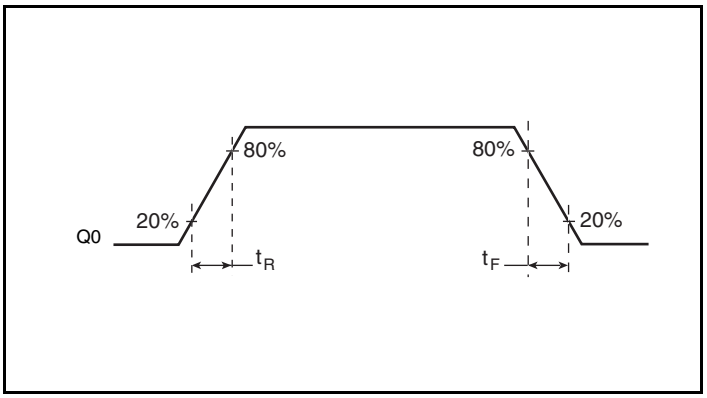
3.3V Output Load AC Test Circuit



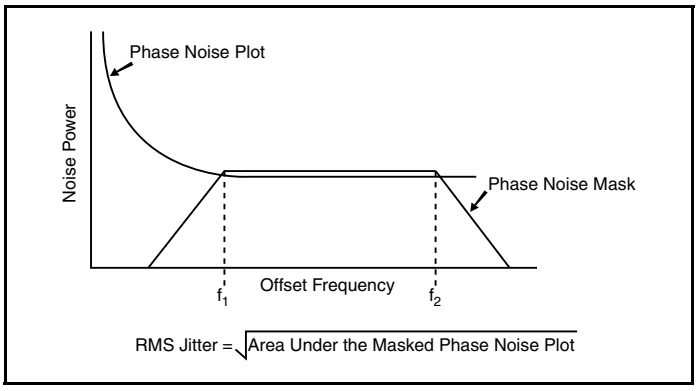
2.5V Output Load AC Test Circuit



Output Duty Cycle/Pulse Width/Period



Output Rise/Fall Time



RMS Phase Jitter

Application Information

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. ICS840021I provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} and V_{DDA} should be individ- ually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{DDA} pin.

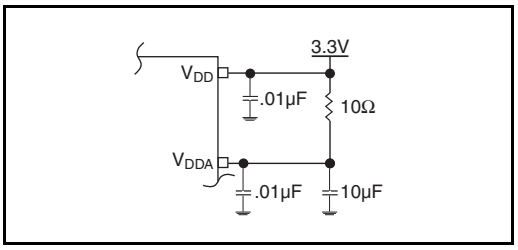


Figure 1. Power Supply Filtering

Crystal Input Interface

The ICS840021I has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 2* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

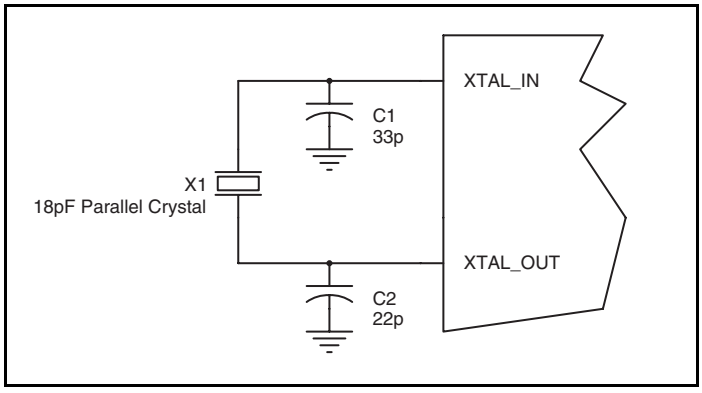


Figure 2. Crystal Input Interface

LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS signals, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

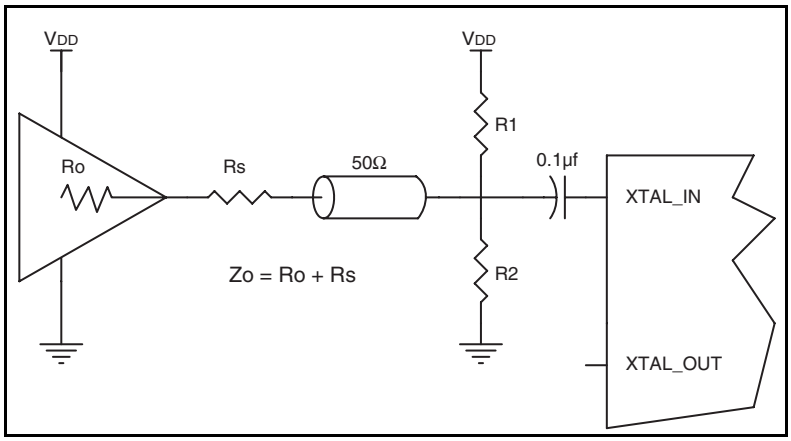


Figure 3. General Diagram for LVCMOS Driver to XTAL Input Interface

Application Schematic

Figure 4A shows a schematic example of the ICS840021I. An example of LVCMOS termination is shown in this schematic. Additional LVCMOS termination approaches are shown in the LVCMOS Termination Application Note. In this example, an 18pF parallel resonant 25MHz crystal is used for generating 125MHz output frequency. The C1 = 22pF and C2 = 33pF are recommended for frequency accuracy. For different board layout, the C1 and C2 values may be slightly adjusted for optimizing frequency accuracy.

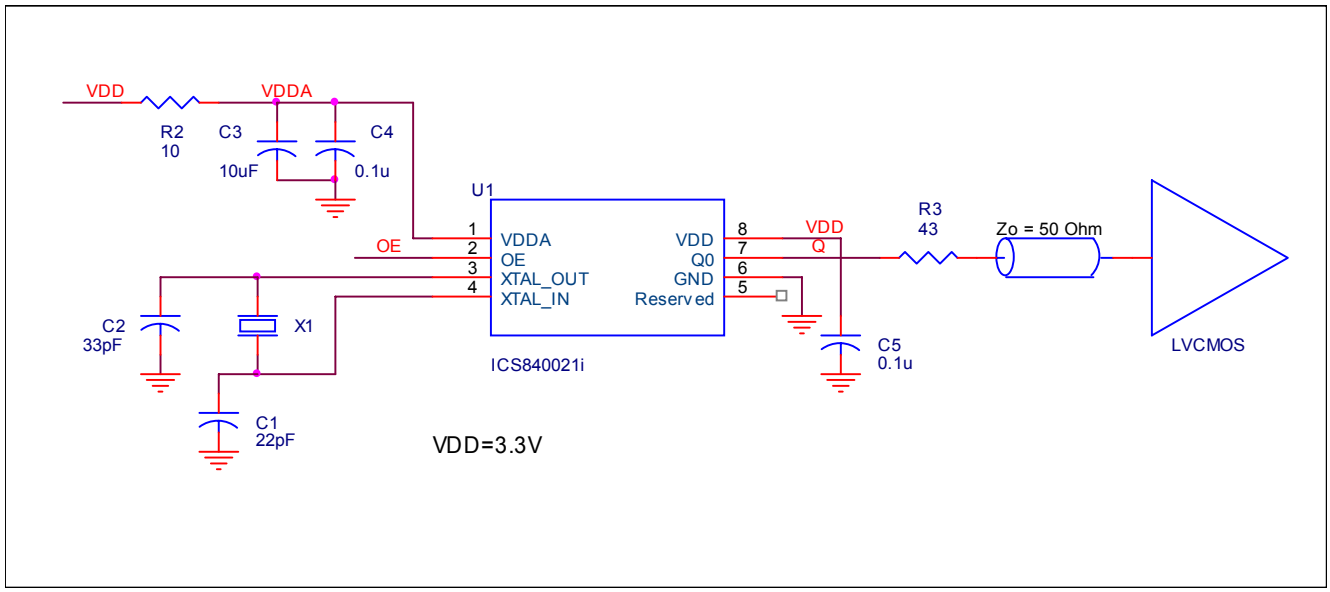


Figure 4A. ICS840021I Schematic Example

PC Board Layout Example

Figure 4B shows an example of ICS840021I P.C. board layout. The crystal X1 footprint shown in this example allows installation of either surface mount HC49S or through-hole HC49 package. The footprints of other components in this example are listed in the *Table 7.* There should be at least one decoupling capacitor per power pin. The decoupling capacitors should be located as close as possible to the power pins. The layout assumes that the board has clean analog power ground plane.

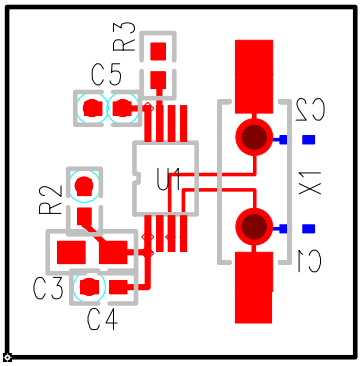


Figure 4B. ICS840021I PC Board Layout Example

Table 7. Footprint Table

Reference	Size
C1, C2	0402
C3	0805
C4, C5	0603
R2, R3	0603

NOTE: Table 7, lists component sizes shown in this layout example.

Reliability Information

Table 8A. θ_{JA} vs. Air Flow Table for a 8 Lead TSSOP

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	101.7°C/W	90.5°C/W	89.8°C/W

Table 8B. θ_{JA} vs. Air Flow Table for a 16 Lead VFQFN

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	74.97°C/W	65.5°C/W	58.8°C/W

Transistor Count

The transistor count for ICS840021I is: 1961

Package Outline and Package Dimensions

Package Outline - G Suffix for 8 Lead TSSOP

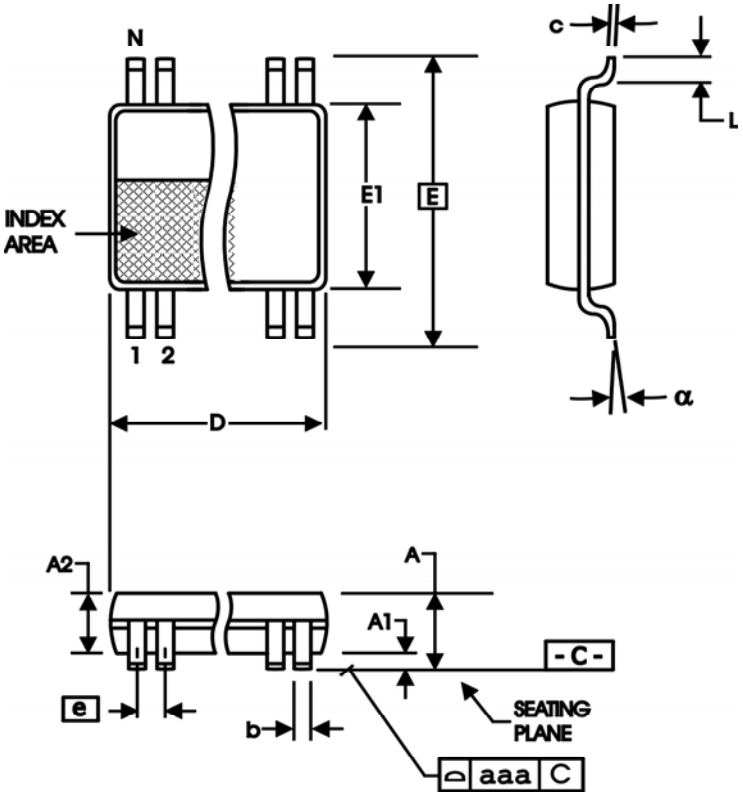
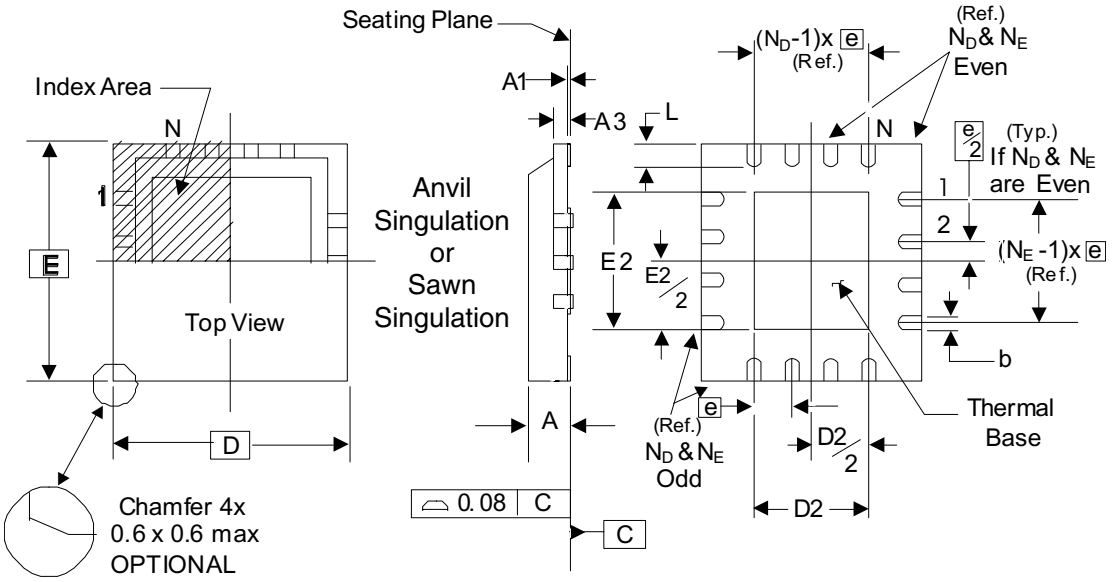


Table 9A. Package Dimensions

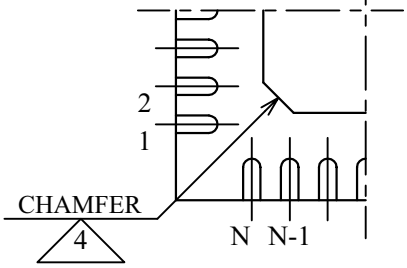
All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	8	
A		1.20
A1	0.5	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	2.90	3.10
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

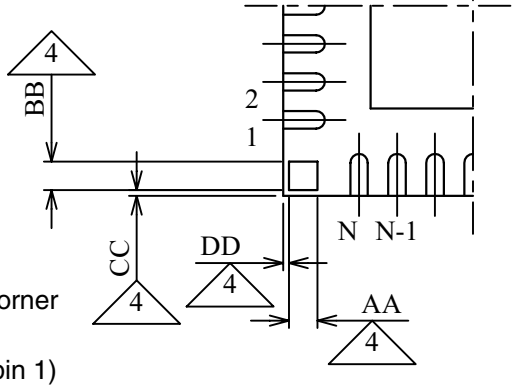
Package Outline - K Suffix for 16 Lead VFQFN



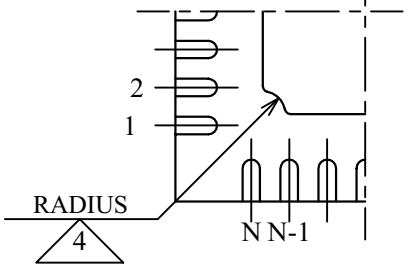
Bottom View w/Type A ID



Bottom View w/Type B ID



Bottom View w/Type C ID



There are 3 methods of indicating pin 1 corner at the back of the VFQFN package are:

1. Type A: Chamfer on the paddle (near pin 1)
2. Type B: Dummy pad between pin 1 and N.
3. Type C: Mouse bite on the paddle (near pin 1)

Table 9B. Package Dimensions

JEDEC Variation: VEED-2/-4 All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	16	
A	0.80	1.00
A1	0	0.05
A3	0.25 Ref.	
b	0.18	0.30
N_D & N_E	4	
D & E	3.00 Basic	
D2 & E2	1.00	1.80
e	0.50 Basic	
L	0.30	0.50

Reference Document: JEDEC Publication 95, MO-220

Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
840021AGI	021AI	8 Lead TSSOP	Tube	-40°C to 85°C
840021AGIT	021AI	8 Lead TSSOP	2500 Tape & Reel	-40°C to 85°C
840021AGILF	21AIL	“Lead-Free” 8 Lead TSSOP	Tube	-40°C to 85°C
840021AGILFT	21AIL	“Lead-Free” 8 Lead TSSOP	2500 Tape & Reel	-40°C to 85°C
840021AKILF	1AIL	“Lead-Free” 16 Lead VFQFN	Tray	-40°C to 85°C
840021AKILFT	1AIL	“Lead-Free” 16 Lead VFQFN	2500 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	T10	11	Ordering Information Table - Added Lead-Free Marking.	7-30-07
A		9	Added *LVCMOS to XTAL Interface* section. Changed formatting throughout data sheet	1-20-09
B	T1	1 2	Pin Assignment - changed pin 5 from nc to Reserved. Pin Description Table - changed pin 5 from nc to Reserved.	5/4/09
C	T8B T9B 10	1 3 11 13 14	Add 16 VFQFN Pin Assignment. Absolute Maximum Ratings - added 16 VFQFN Package Thermal Impedance information. Added 16 VFQFN Air Flow Table. Added 16 VFQFN Package Drawing and Dimensions. Ordering Information Table - added 16 VFQFN ordering information.	6/25/09
C			Deleted “Proposed” label throughout the datasheet.	7/14/09
C		1 13	Feature Section corrected temperature bullet from 40°C to -40°C. Added new VFQFN bottom view package drawing.	1/27/10

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