General Description

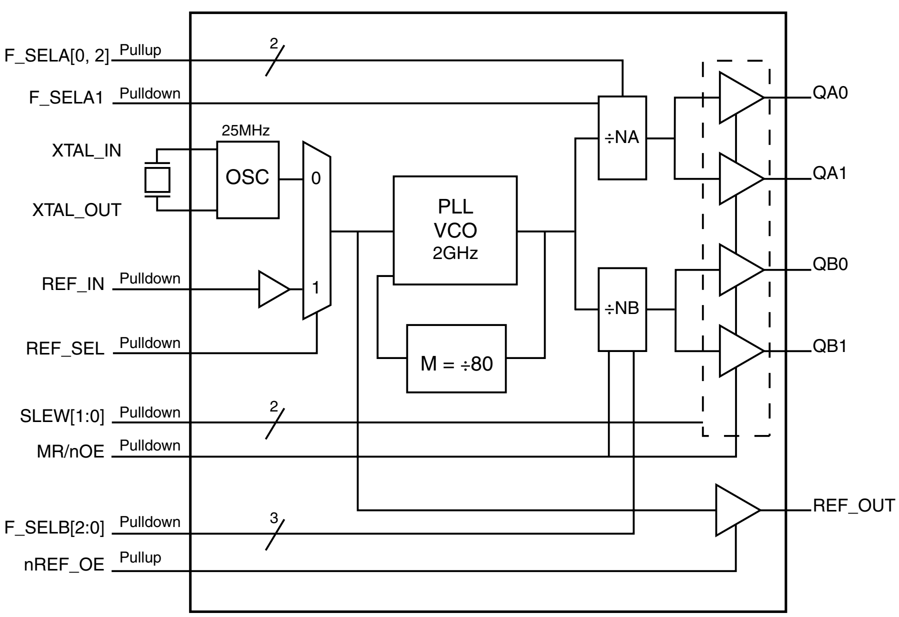
The 840S05I is a five output LVCMOS/LVTTL Frequency Synthesizer accepting crystal or single-ended reference clock inputs. The 840S05I uses a 25MHz parallel resonant crystal to generate 33.33MHz – 166.67MHz clock signals, replacing solutions requiring multiple oscillator and fan-out buffer solution. The device supports output slew rate control with two slew select pins (SLEW[1:0]). The VCO operates at a frequency of 2GHz. The device has 2 output banks, Bank A with two 33.33MHz – 166.67MHz LVCMOS/LVTTL outputs and Bank B with two 33.33MHz – 166.67MHz LVCMOS/LVTTL outputs.

The two banks have their own dedicated frequency select pins and can be independently set for frequencies in the ranges mentioned above. Designed for networking and industrial applications, the 840S05I can also drive the high-speed clock inputs of communication processors, DSPs, switches and bridges.

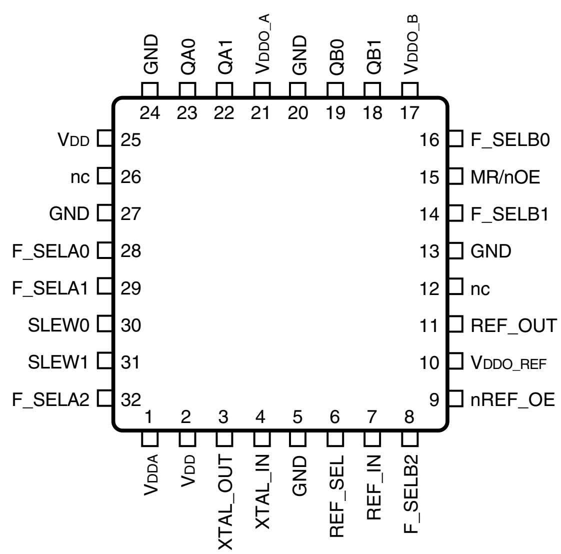
Features

- Four single-ended LVCMOS/LVTTL clock outputs
- One REF_OUT LVCMOS/LVTTL clock output
- Selectable crystal oscillator interface, 25MHz, 18pF parallel resonant crystal or LVCMOS/LVTTL single-ended reference input
- Supports the following output frequencies on either bank: 33.33MHz, 50MHz, 66.67MHz, 83.33MHz, 100MHz, 125MHz, 133.33MHz, and 166.67MHz
- VCO: 2GHz
- Slew rate control
- Output supply modes:
  Core/Output
  3.3V/3.3V
  3.3V/2.5V
- -40°C to 85°C ambient operating temperature
- Lead-free (RoHS 6) packaging

Block Diagram



Pin Assignment



840S05I

32-Lead TQFP, E-Pad
7mm x 7mm x 1mm package body
Y Package
Top View

Pin Description and Pin Characteristic Tables

Table 1. Pin Descriptions

Number	Name	Type		Description
1	V_{DDA}	Power		Analog supply pin.
2, 25	V_{DD}	Power		Core supply pin.
3, 4	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input. XTAL_OUT is the output.
5, 13, 20, 24, 27	GND	Power		Power supply ground.
6	REF_SEL	Input	Pulldown	Reference select pin. See Table 3C. LVCMOS/LVTTL interface levels.
7	REF_IN	Input	Pulldown	Single-ended 25MHz reference clock input. LVCMOS/LVTTL interface levels.
8, 14, 16	F_SELB2, F_SELB1, F_SELB0	Input	Pulldown	Frequency select pins for Bank B outputs. See Table 3A. LVCMOS/LVTTL interface levels.
9	nREF_OE	Input	Pullup	Active low REF_OUT enable/disable pin. See Table 3D. LVCMOS/LVTTL interface levels.
10	V_{DDO_REF}	Power		Output supply pin for REF_OUT clock output.
11	REF_OUT	Output		Single-ended LVCMOS/LVTTL reference clock output.
12, 26	nc	Unused		No connect.
15	MR/nOE	Input	Pulldown	Active HIGH Master Reset. Active LOW output enable. See Table 3E. LVCMOS/LVTTL interface levels.
17	V_{DDO_B}	Power		Output supply pin for QBx outputs.
18, 19	QB1, QB0	Output		Single-ended Bank B clock outputs. LVCMOS/LVTTL interface levels.
21	V_{DDO_A}	Power		Output supply pin for QAx outputs.
22, 23	QA1, QA0	Output		Single-ended Bank A clock outputs. LVCMOS/LVTTL interface levels.
28, 32	F_SELA0, F_SELA2	Input	Pullup	Frequency select pins for Bank A outputs. See Table 3A. LVCMOS/LVTTL interface levels.
29	F_SELA1	Input	Pulldown	Frequency select pin for Bank A outputs. See Table 3A. LVCMOS/LVTTL interface levels.
30, 31	SLEW0, SLEW1	Input	Pulldown	Slew rate select pins for LVCMOS/LVTTL clock output. See Table 3B. LVCMOS/LVTTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				2		pF
C_{PD}	Power Dissipation Capacitance	QA[1:0], QB[1:0]	SLEW[1:0] = 00 V_{DD}, V_{DDA}, V_{DDO_REF}, V_{DDO_A}, V_{DDO_B} = 3.465V		6.5		pF
		QA[1:0], QB[1:0]	SLEW[1:0] = 01 V_{DD}, V_{DDA}, V_{DDO_REF}, V_{DDO_A}, V_{DDO_B} = 3.465V		10.5		pF
		QA[1:0], QB[1:0]	SLEW[1:0] = 10 V_{DD}, V_{DDA}, V_{DDO_REF}, V_{DDO_A}, V_{DDO_B} = 3.465V		13		pF
		QA[1:0], QB[1:0]	SLEW[1:0] = 11 V_{DD}, V_{DDA}, V_{DDO_REF}, V_{DDO_A}, V_{DDO_B} = 3.465V		16		pF
		QA[1:0], QB[1:0]	V_{DD}, V_{DDA} = 3.465V V_{DDO_REF}, V_{DDO_A}, V_{DDO_B} = 2.625V		5		pF
		REF_OUT	V_{DD}, V_{DDA} = 3.465V V_{DDO_REF}, V_{DDO_A}, V_{DDO_B} = 3.465V or 2.625V		4		pF
R_{PULLUP}	Input Pullup Resistor				51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor				51		kΩ
R_{OUT}; NOTE 1	Output Impedance	QA[1:0], QB[1:0]	V_{DDO_A}, V_{DDO_B} = 3.3V		18		Ω
		QA[1:0], QB[1:0]	V_{DDO_A}, V_{DDO_B} = 2.5V		21		Ω
		REF_OUT	V_{DDO_REF} = 3.3V		22		Ω
		REF_OUT	V_{DDO_REF} = 2.5V		25		Ω

NOTE 1: Characterized with SLEW[1:0] = 00.

Function Tables

Table 3A. Frequency Select Function Table

Inputs					Output Frequency	
F_SELA2, F_SELB2	F_SELA1, F_SELB1	F_SELA0, F_SELB0	M Divider Value	NA, NB Divider Value	QA[1:0] (MHz)	QB[1:0] (MHz)
L	L	L	80	60	33.33	33.33 (default)
L	L	H	80	40	50	50
L	H	L	80	30	66.67	66.67
L	H	H	80	24	83.33	83.33
H	L	L	80	20	100	100
H	L	H	80	16	125 (default)	125
H	H	L	80	15	133.33	133.33
H	H	H	80	12	166.67	166.67

NOTE: Using 25MHz reference.

Table 3B. Slew Rate Function Table

Setting		Slew Rate (v/ns)
SLEW1	SLEW0	
0	0	3.5 (Default)
0	1	2.6
1	0	1.8
1	1	1.0

NOTE: Typical values for V_{DDO_A}, V_{DDO_B} = 3.3V. Refer to the AC Characteristics Table for more details.

Table 3C. REF_SEL Function Table

REF_SEL	Input Reference
0 (Default)	XTAL_IN
1	REF_IN

Table 3D. nREF_OE Function Table

nREF_OE	REF_OUT State
0	REF_OUT enabled
1 (Default)	REF_OUT disabled (Logic LOW)

Table 3E. MR/nOE Function Table

MR/nOE	Function
0 (Default)	QA and QB outputs enabled.
1	Device reset, QA and QB outputs disabled (Logic LOW).

NOTE: A MR/OE pulse is required after device power-up to guarantee functionality.

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I XTAL_IN Other Inputs	 0V to V_{DD} -0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA}	36.2°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDO\_REF} = V_{DDO\_A} = V_{DDO\_B}$ = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.20	3.3	V_{DD}	V
V_{DDO_A}, V_{DDO_B}, V_{DDO_REF}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				160	mA
I_{DDA}	Analog Supply Current				20	mA
I_{DDO_A}, I_{DDO_B}	Output Supply Current	SLEW[1:0] = 11, QA[1:0], QB[1:0] = 166.67MHz; REF_OUT = 25MHz, Outputs Not Loaded			30	mA
I_{DDO_REF}	Output Supply Current	Outputs Not Loaded			2	mA

NOTE: All parameters specified for inputs and outputs under static conditions, unless otherwise noted.

Table 4B. Power Supply DC Characteristics, V_{DD} = 3.3V ± 5%, $V_{DDO\_REF} = V_{DDO\_A} = V_{DDO\_B}$ = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.20	3.3	V_{DD}	V
V_{DDO_A}, V_{DDO_B}, V_{DDO_REF}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				160	mA
I_{DDA}	Analog Supply Current				20	mA
I_{DDO_A}, I_{DDO_B}	Output Supply Current	SLEW[1:0] = 11, QA[1:0], QB[1:0] = 166.67MHz; REF_OUT = 25MHz, Outputs Not Loaded			10	mA
I_{DDO_REF}	Output Supply Current	Outputs Not Loaded			1	mA

NOTE: All parameters specified for inputs and outputs under static conditions, unless otherwise noted.

Table 4C. LVCMOS DC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDO_REF} = V_{DDO_A} = V_{DDO_B} = 3.3V ± 5% or 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.465V	2.2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.465V	-0.3		0.8	V
I_{IH}	Input High Current	nREF_OE, F_SELA0, FSELA2	V_{DD} = V_{IN} = 3.465V			10	µA
		F_SELB[2:0], SLEW0, SLEW1, F_SELA1, MR/nOE, REF_IN, REF_SEL	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	nREF_OE, F_SELA0, FSELA2	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
		F_SELB[2:0], SLEW0, SLEW1, F_SELA1, MR/nOE, REF_IN, REF_SEL	V_{DD} = 3.465V, V_{IN} = 0V	-10			µA
V_{OH}	Output High Voltage; NOTE 1, 2		V_{DDO_X} = 3.3V±5%	2.45			V
			V_{DDO_X} = 2.5V±5%	1.75			V
V_{OL}	Output Low Voltage; NOTE 1, 2		V_{DDO_X} = 3.3V±5%			0.85	V
			V_{DDO_X} = 2.5V±5%			0.65	V

NOTE: V_{DDO_X} denotes V_{DDO_A}, V_{DDO_B}, V_{DDO_REF}.
NOTE 1: Outputs terminated with 50Ω to $V_{DDO\_A,\ \_B,\ \_REF}$/2. See Parameter Measurement Information, *Output Load Test Circuit diagram.*
NOTE 2: Characterized with QA[1:0], QB[1:0] = 33.33MHz and REF_OUT = 25MHz.

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

NOTE: Characterized using an 18pF parallel resonant crystal.

AC Electrical Characteristics

Table 6A. AC Characteristics, $V_{DD} = V_{DDO\_REF} = V_{DDO\_A} = V_{DDO\_B}$ = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	QA[1:0]		33.33		166.67	MHz
		QB[1:0]		33.33		166.67	MHz
*t*sk(o)	Output Skew; NOTE 1, 2	QA[1:0] or QB[1:0]	f_{OUT} ≤ 125MHz, 25MHz Crystal Input			180	ps
*t*sk(b)	Bank Skew; NOTE 2, 3	QA[1:0] or QB[1:0]	SLEW[1:0] = 00			35	ps
tjit(per)	Period Jitter, RMS; NOTE 4		f_{OUT} = 125MHz, SLEW[1:0] = 00		3.4		ps
			f_{OUT} = 125MHz, SLEW[1:0] = 01		3.4		ps
			f_{OUT} = 125MHz, SLEW[1:0] = 10		3.5		ps
			f_{OUT} = 125MHz, SLEW[1:0] = 11		4.6		ps
t_{SLEW}	Slew Rate; NOTE 5	QA[1:0] or QB[1:0]	SLEW[1:0] = 00, Rise/Fall Time: 20% to 80%		3.5	5.0	V/ns
		QA[1:0] or QB[1:0]	SLEW[1:0] = 01, Rise/Fall Time: 20% to 80%		2.6	3.8	V/ns
		QA[1:0] or QB[1:0]	SLEW[1:0] = 10, Rise/Fall Time: 20% to 80%		1.8	2.7	V/ns
		QA[1:0] or QB[1:0]	SLEW[1:0] = 11, Rise/Fall Time: 20% to 80%		1.0	1.7	V/ns
t_L	PLL Lock Time		SLEW[1:0] = 00			20	ms
odc	Output Duty Cycle	QA[1:0] or QB[1:0]	25MHz Crystal Input, SLEW[1:0] = 00	45		55	%

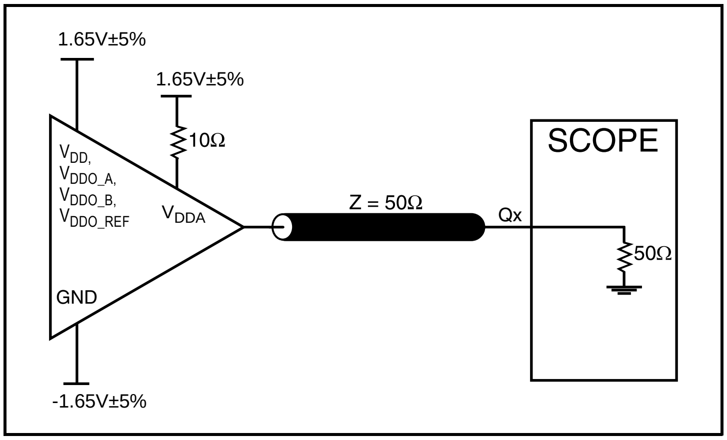
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. Device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO\_A,\ \_B,\ \_REF}/2$.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Defined as skew within a bank of outputs at the same supply voltage and with equal load conditions.
NOTE 4: Characterized using a 25MHz Crystal input. REF_OUT is disabled.
NOTE 5: A slew rate of 2V/ns or greater should be selected for output frequencies of 100MHz and higher.

Table 6B. AC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDO_REF} = V_{DDO_A} = V_{DDO_B} = 2.5V ± 5%, T_A = -40°C to 85°C

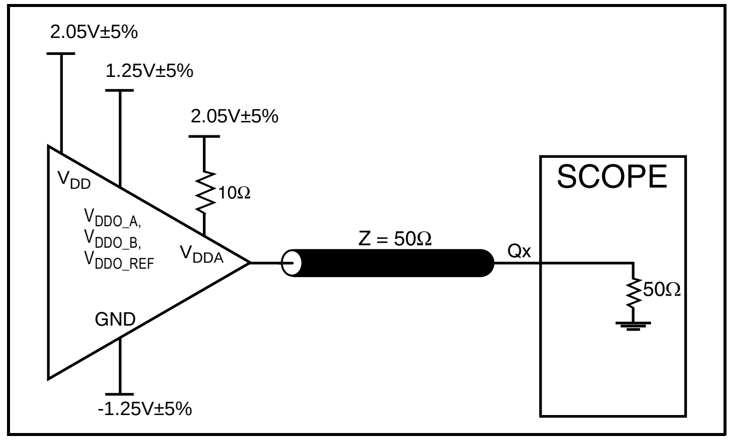
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	QA[1:0]		33.33		166.67	MHz
		QB[1:0]		33.33		166.67	MHz
*t*sk(o)	Output Skew; NOTE 1, 2	QA[1:0] or QB[1:0]	f_{OUT} ≤ 125MHz, 25MHz Crystal Input			210	ps
*t*sk(b)	Bank Skew; NOTE 2, 3	QA[1:0] or QB[1:0]	SLEW[1:0] = 00			45	ps
tjit(per)	Period Jitter, RMS; NOTE 4		f_{OUT} = 125MHz, SLEW[1:0] = 00		3.5		ps
			f_{OUT} = 125MHz, SLEW[1:0] = 01		3.6		ps
			f_{OUT} = 125MHz, SLEW[1:0] = 10		4.1		ps
			f_{OUT} = 125MHz, SLEW[1:0] = 11		6.3		ps
t_{SLEW}	Slew Rate; NOTE 5	QA[1:0] or QB[1:0]	SLEW[1:0] = 00, Rise/Fall Time: 20% to 80%		3.0	4.5	V/ns
		QA[1:0] or QB[1:0]	SLEW[1:0] = 01, Rise/Fall Time: 20% to 80%		2.2	3.4	V/ns
		QA[1:0] or QB[1:0]	SLEW[1:0] = 10, Rise/Fall Time: 20% to 80%		1.6	2.6	V/ns
		QA[1:0] or QB[1:0]	SLEW[1:0] = 11, Rise/Fall Time: 20% to 80%		0.9	1.7	V/ns
t_L	PLL Lock Time		SLEW[1:0] = 00			25	ms
odc	Output Duty Cycle	QA[1:0] or QB[1:0]	25MHz Crystal Input, SLEW[1:0] = 00	45		55	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. Device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO\_A,\ \_B,\ \_REF}/2$.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Defined as skew within a bank of outputs at the same supply voltage and with equal load conditions.
NOTE 4: Characterized using a 25MHz Crystal input. REF_OUT is disabled.
NOTE 5: A slew rate of 2V/ns or greater should be selected for output frequencies of 100MHz and higher.

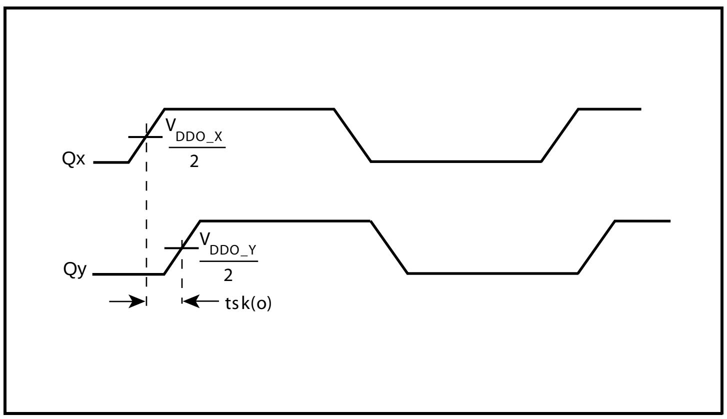
Parameter Measurement Information



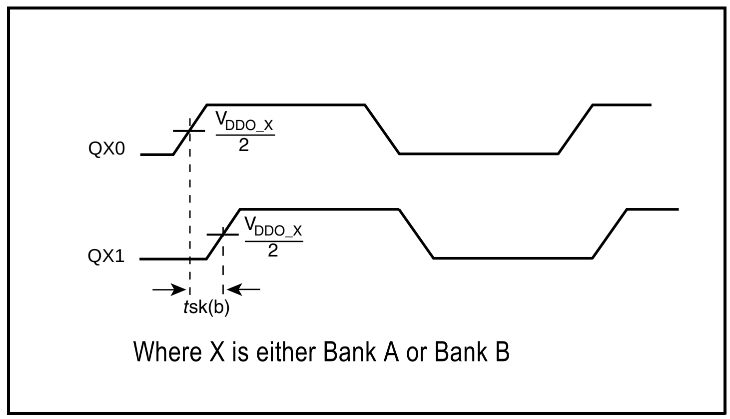
3.3V Core/3.3V LVCMOS Output Load Test Circuit



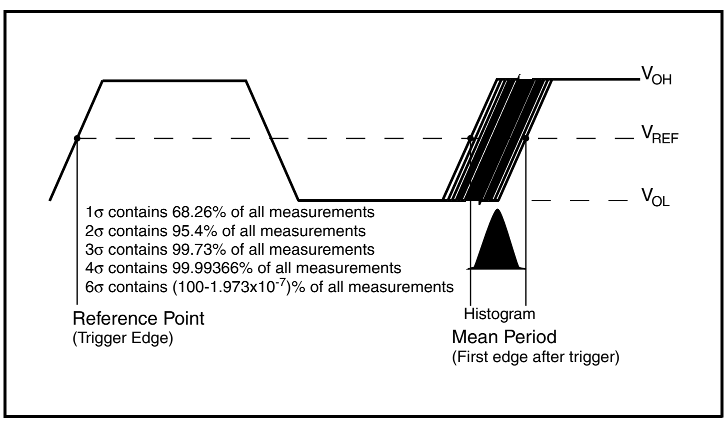
3.3V Core/2.5V LVCMOS Output Load Test Circuit



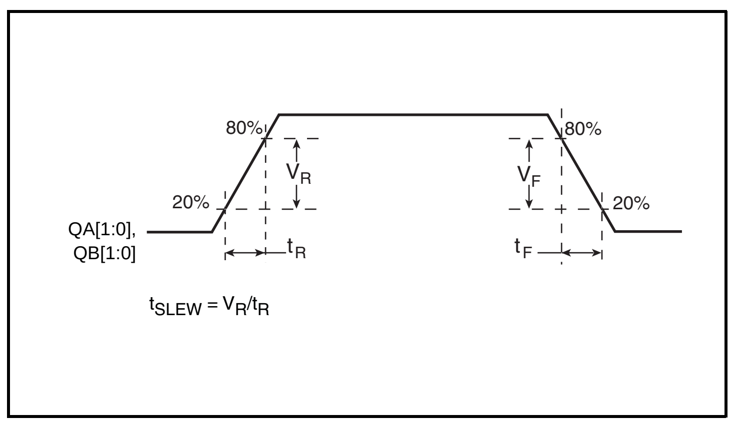
Output Skew



Bank Skew

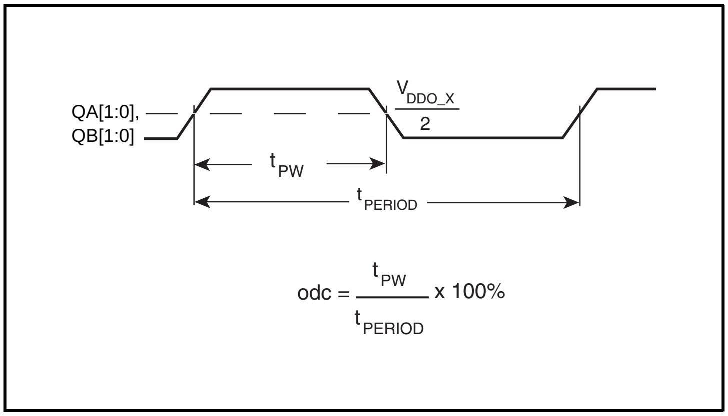


RMS Period Jitter



Output Slew Rate

Parameter Measurement Information, continued



Output Duty Cycle/Pulse Width/Period

Applications Information

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

REF_IN Input

For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the REF_IN to ground.

Outputs:

LVCMOS Outputs

All unused LVCMOS outputs can be left floating. There should be no trace attached.

Overdriving the XTAL Interface

The XTAL_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/ns. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. *Figure 1A* shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and changing R2 to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. *Figure 1B* shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

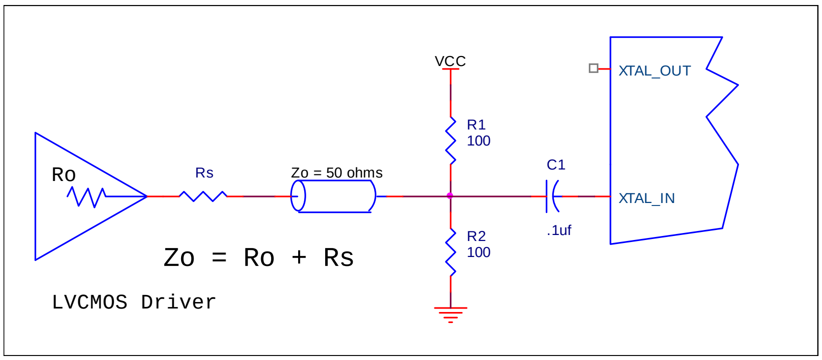


Figure 1A. General Diagram for LVCMOS Driver to XTAL Input Interface

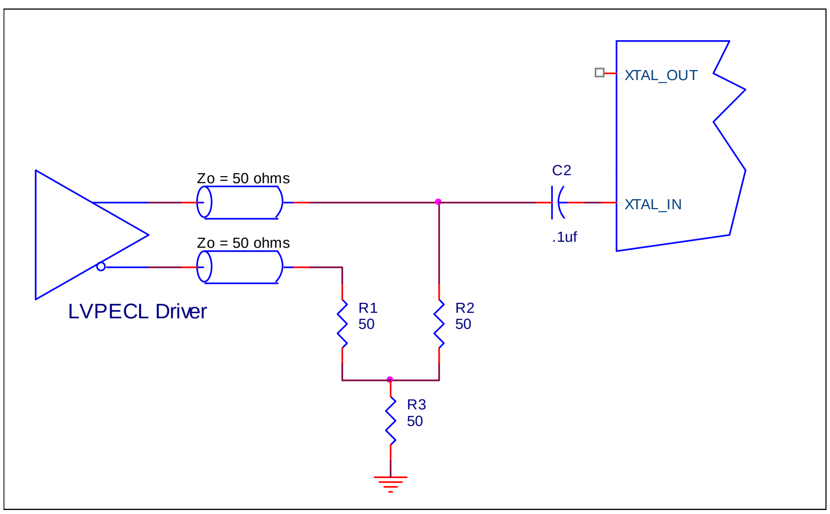


Figure 1B. General Diagram for LVPECL Driver to XTAL Input Interface

EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 2.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.

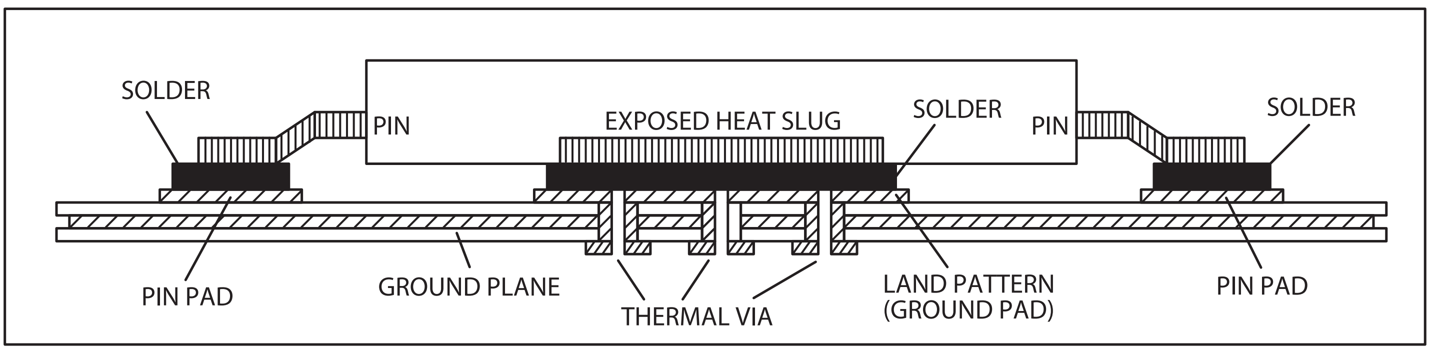


Figure 2. Assembly for Exposed Pad Thermal Release Path - Side View (drawing not to scale)

Schematic Layout

Figure 3 shows an example 840S05I application schematic. This schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure that the logic control inputs are properly set.

In this schematic, the device is operated at VDD=VDDA = 3.3V and VDDO_A, VDDO_B and VDDO_REF=2.5V. An 18pF parallel resonant 25MHz crystal is used with the recommended load capacitors C1 = 33pF and C2 = 27pF for frequency accuracy. Depending on the parasitic capacity on the crystal terminals of the printed circuit board layout, these values might require a slight adjustment to optimize the frequency accuracy. Crystals with other load capacitance specifications can be used. This will require adjusting C1 and C2. For this device, the crystal load capacitors are required for proper operation.

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 840S05I provides separate power supply pins to isolate any high switching noise from coupling into the internal PLL.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1µf capacitor in each power pin filter should be placed on the device side. The other components can be on the opposite side of the PCB.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

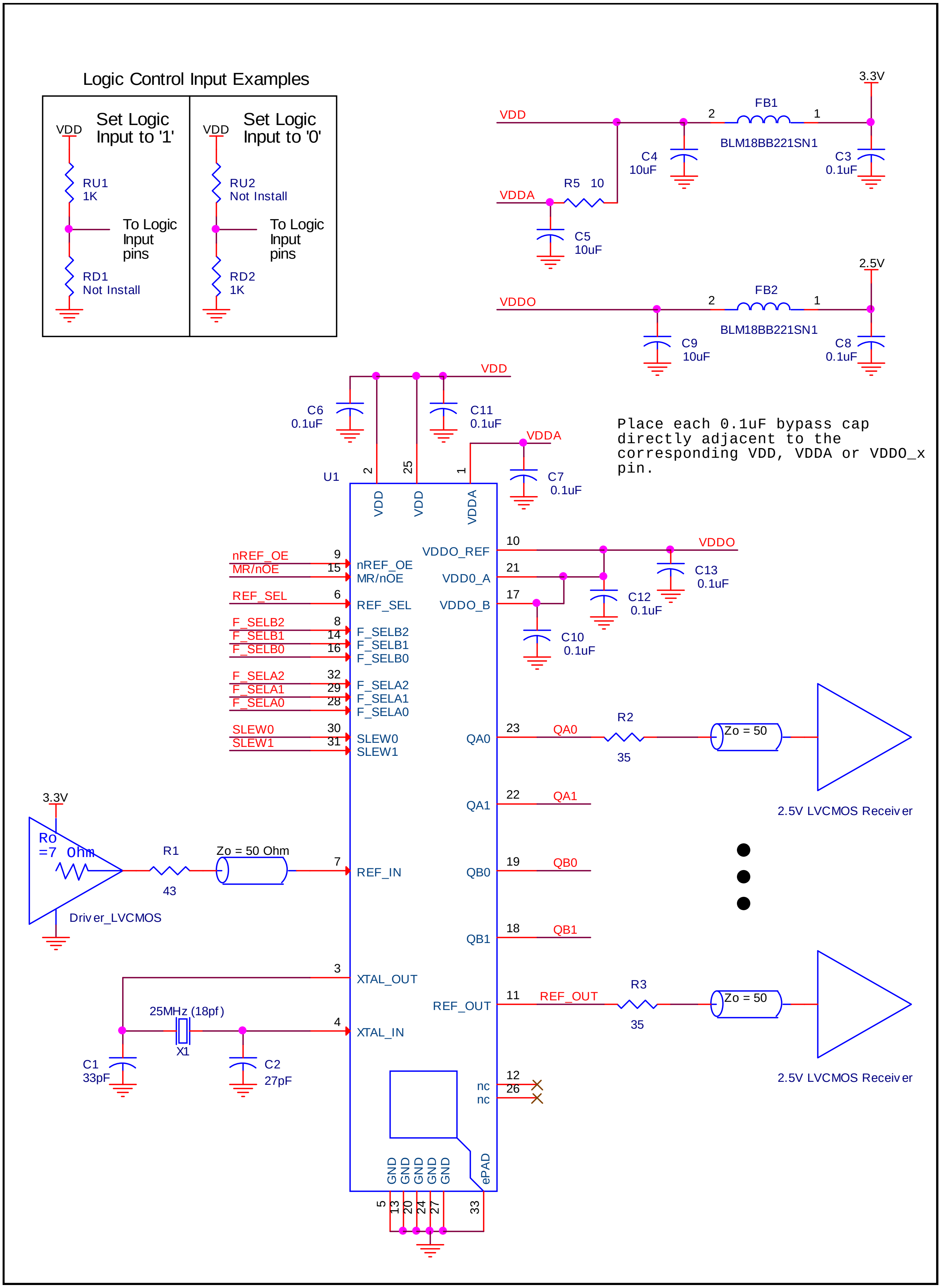


Figure 3. 840S05I Application Schematic

Power Considerations

This section provides information on power dissipation and junction temperature for the 840S05I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 840S05I is the sum of the core power plus the analog power plus the power dissipation in the load(s). The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

The maximum current at 85°C is as follows:
I_{DD_MAX} = 160mA

I_{DDA_MAX} = 20mA

Core Power Dissipation

- Power $(core)_{MAX}$ = V_{DD_MAX} * (I_{DD} + I_{DDA}) = 3.465V *(160mA + 20mA) = **623.7mW**

LVCMOS Output Power Dissipation

- Output Impedance R_{OUT} Power Dissipation due to Loading 50Ω to V_{DD}/2
  Output Current I_{OUT} = V_{DD_MAX} / [2 * (50Ω + R_{OUT})] = 3.465V / [2 * (50Ω + 22Ω)] = **24.06mA**
- Power Dissipation on the R_{OUT} per LVCMOS output
  Power (R_{OUT}) = R_{OUT} * $(I_{OUT})^2$ = 22Ω * $(24.06mA)^2$ = **12.74mW per output**
- Total Power Dissipation on the R_{OUT}
  Total Power (R_{OUT}) = 12.74mW * 5 = **63.7mW**

- Dynamic Power Dissipation at 25MHz (REF_OUT)
  Power (25MHz) = C_{PD} * Frequency * $(V_{DDO})^2$ = 4pF * 25MHz * $(3.465V)^2$ = **1.2mW per output**
  Total Power (25MHz) = 1.2mW * 1 = **1.2mW**
- Dynamic Power Dissipation at 166.67MHz (QA[1:0], QB[1:0])
  Power (166.67MHz) = C_{PD} * Frequency * $(V_{DDO})^2$ = 16pF * 166.67MHz * $(3.465V)^2$ = **32.02mW per output**
  Total Power (166.67MHz) = 32.02mW * 4 = **128.08mW**

Total Power Dissipation

- **Total Power**
  = Power (core) + Power (output) + Total Power (25MHz) + Total Power (166.67MHz)
  = 623.7mW + 63.7mW + 1.2mW + 128.08mW
  = 816.68mW

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 36.2°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.817W * 36.2°C/W = 114.6°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance θ_{JA} for 32 Lead TQFP, E-Pad, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	36.2°C/W	30.6°C/W	29.2°C/W

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for a 32 Lead TQFP, E-Pad

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	36.2°C/W	30.6°C/W	29.2°C/W

Transistor Count

The transistor count for 840S05I is: 2395

Package Outline and Package Dimensions

Package Outline - Y Suffix for 32 Lead TQFP, E-Pad

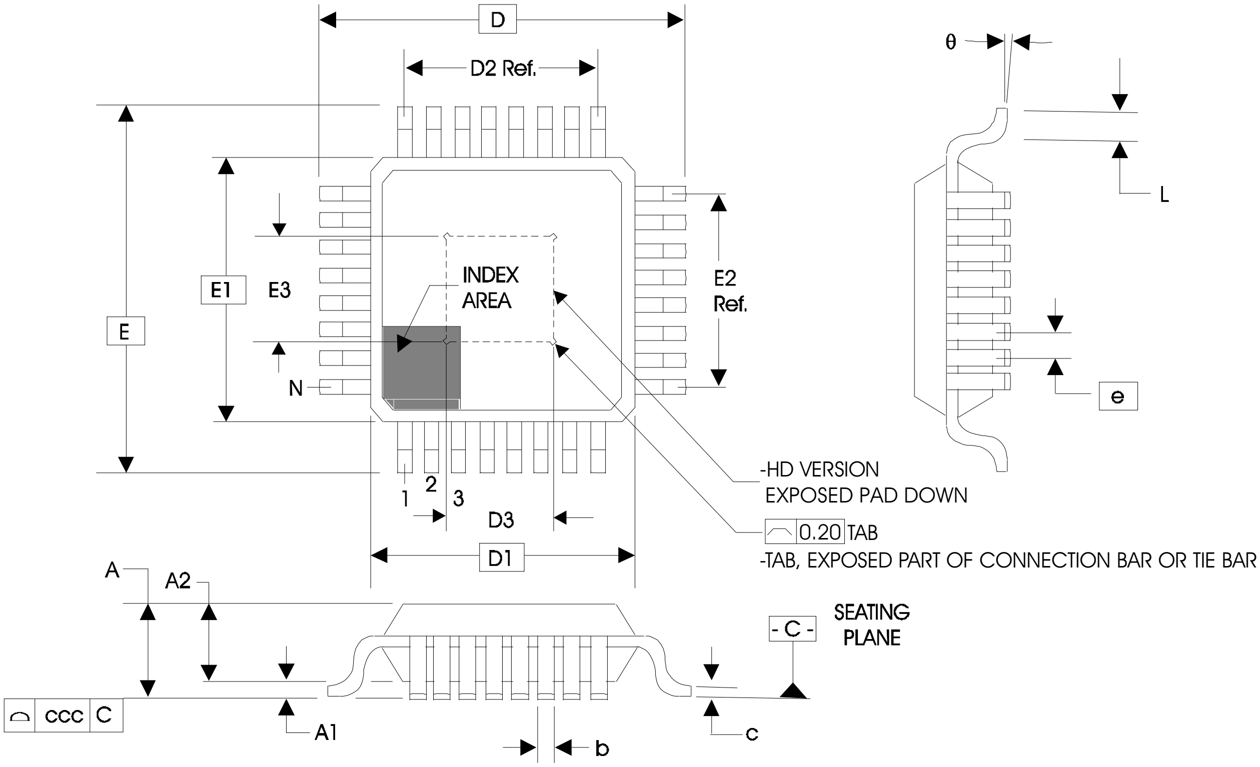


Table 9. Package Dimensions 32 Lead TQFP, E-Pad

JEDEC Variation: ABA - HD All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		32	
A			1.20
A1	0.05	0.10	0.15
A2	0.95	1.00	1.05
b	0.30	0.35	0.40
c	0.09		0.20
D, E		9.00 Basic	
D1, E1		7.00 Basic	
D2, E2		5.60 Ref.	
D3, E3	3.0	3.5	4.0
e		0.80 Basic	
L	0.45		0.75
θ	0°		7°
ccc			0.10

Reference Document: JEDEC Publication 95, MS-026

Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
840S05AYILF	840S05AIL	Lead-Free, 32 Lead TQFP, E-Pad	Tray	-40°C to 85°C
840S05AYILFT	840S05AIL	Lead-Free, 32 Lead TQFP, E-Pad	Tape & Reel	-40°C to 85°C

Revision History

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Revision Date	Description of Change
April 11, 2016	▪ Removed ICS from part number where needed. ▪ Updated data sheet header and footer.

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