FemtoClock® NG Crystal-to-HCSL Clock Generator

841654

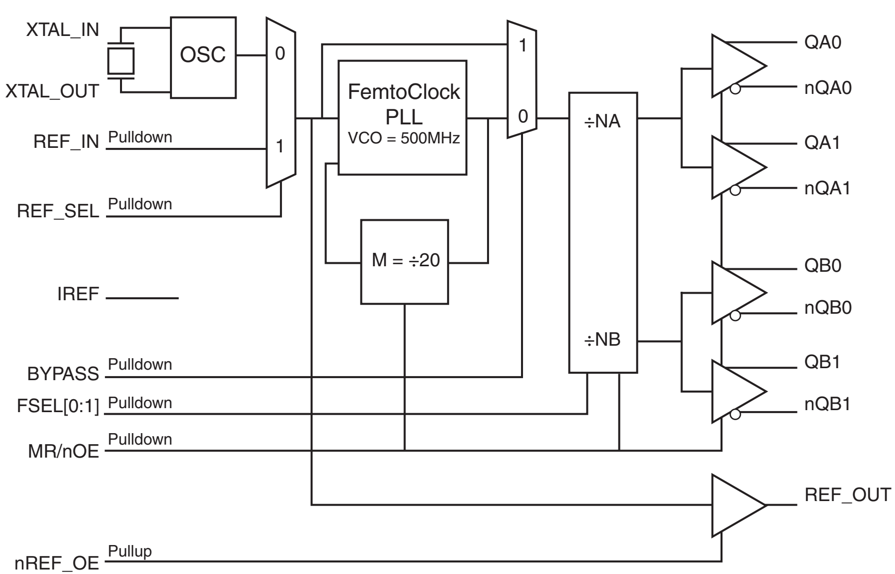
General Description

The 841654 is an optimized PCIe and sRIO clock generator. The device uses a 25MHz parallel crystal to generate 100MHz and 125MHz clock signals, replacing solutions requiring multiple oscillator and fanout buffer solutions. The device has excellent phase jitter (< 1ps rms) suitable to clock components requiring precise and low-jitter PCIe or sRIO or both clock signals. Designed for telecom, networking and industrial applications, the 841654 can also drive the high-speed sRIO and PCIe SerDes clock inputs of communication processors, DSPs, switches and bridges.

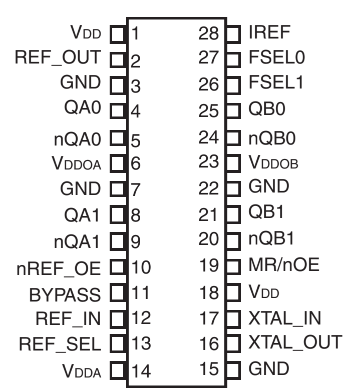
Features

- Four differential HCSL clock outputs: configurable for PCIe (100MHz) and sRIO (100MHz or 125MHz) clock signals
  One REF_OUT LVCMOS/LVTTL clock output
- Selectable crystal oscillator interface, 25MHz, 18pF parallel resonant crystal or LVCMOS/LVTTL single-ended reference clock input
- Supports the following output frequencies: 100MHz or 125MHz
- VCO: 500MHz
- PLL bypass and output enable
- RMS phase jitter at 100MHz, using a 25MHz crystal (1.875MHz - 20MHz): 0.44ps (typical)
- Full 3.3V power supply mode
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Block Diagram



Pin Assignment



841654
28-Lead TSSOP
6.1mm x 9.7mm x 0.925mm package body
G Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 18	V_{DD}	Power		Core supply pins.
2	REF_OUT	Output		Single-ended reference frequency clock output. LVCMOS/LVTTL interface levels.
3, 7, 15, 22	GND	Power		Power supply ground.
4, 5, 8, 9	QA0, nQA0, QA1, nQA1	Ouput		Differential Bank A output pairs. HCSL interface levels.
6	V_{DDOA}	Power		Output supply pin for Bank A outputs.
10	nREF_OE	Input	Pullup	Active low REF_OUT enable/disable. See Table 3E. LVCMOS/LVTTL interface levels.
11	BYPASS	Input	Pulldown	Selects PLL operation/PLL bypass operation. See Table 3C. LVCMOS/LVTTL interface levels.
12	REF_IN	Input	Pulldown	Single-ended PLL reference clock input. LVCMOS/LVTTL interface levels.
13	REF_SEL	Input	Pulldown	Reference select. Selects the input reference source. See Table 3B. LVCMOS/LVTTL interface levels.
14	V_{DDA}	Power		Analog supply pin.
16, 17	XTAL_OUT, XTAL_IN	Input		Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input. (PLL reference.)
19	MR/nOE	Input	Pulldown	Active HIGH master reset. Active LOW output enable. When logic HIGH, the internal dividers are reset and the differential outputs are in high impedance (HiZ). When logic LOW, the internal dividers and the differential outputs are enabled. See Table 3D. LVCMOS/LVTTL interface levels.
20, 21 24, 25	nQB1, QB1 nQB0, QB0	Output		Differential Bank B output pairs. HCSL interface levels.
23	V_{DDOB}	Power		Output supply pin for Bank B outputs.
26, 27	FSEL1, FSEL0	Input	Pulldown	Output frequency select pins. LVCMOS/LVTTL interface levels.
28	IREF	Output		HCSL current reference external resistor output. A fixed precision resistor (RREF = 475Ω) from this pin to ground provides a reference current used for differential current-mode QA[0:1]/nQA[0:1] and QB[0:1]/nQB[0:1] clock outputs.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input PullupResistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Table 3A. FSELx Function Table (f_{ref} = 25MHz)

Inputs			Outputs Frequency Settings	
FSEL1	FSEL0	M	QA0:1/nQA0:1	QB0:1/nQB0:1
0	0	20	VCO/5 (100MHz)	VCO/5 (100MHz) (default)
0	1	20	VCO/5 (100MHz)	VCO/4 (125MHz)
1	0	20	VCO/5 (100MHz)	QB0:1 = L, nQB0:1 = H
1	1	20	VCO/4 (125MHz)	VCO/4 (125MHz)

Table 3B. REF_SEL Function Table

Input	
REF_SEL	Input Reference
0	XTAL (default)
1	REF_IN

Table 3C. BYPASS Function Table

Input	
BYPASS	PLL Configuration NOTE 1
0	PLL on (default)
1	PLL bypassed (QA, QB = fref/N)

NOTE 1: Asynchronous function.

Table 3D. MR/nOE Function Table

Input	
MR/nOE	Function NOTE 1
0	Outputs enabled (default)
1	Device reset, outputs disabled (High Impedance)

NOTE 1: Asynchronous function.

Table 3E. nREF_OE Function Table

Input	
nREF_OE	Function NOTE 1
0	REF_OUT enabled
1	REF_OUT disabled (High Impedance) (default)

NOTE 1: Asynchronous function.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DDOX} + 0.5V
Package Thermal Impedance, θ_{JA}	64.4°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY CHARACTERISTICS, $V_{DD} = V_{DDOA} = V_{DDOB}$ = 3.3V±5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.20	3.3	3.465	V
V_{DDOA}, V_{DDOB}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current	Unterminated			85	mA
I_{DDA}	Analog Supply Current	Unterminated			20	mA
I_{DDOA} and I_{DDOB}	Output Supply Current	Unterminated, RREF = 475 ± 1%			5	mA

TABLE 4B. LVCMOS / LVTTL DC CHARACTERISTICS, V_{DD} = 3.3V±5%, TA = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	REF_IN, REF_SEL, BYPASS, MR/nOE, FSEL0, FSEL1	$V_{DD} = V_{IN}$ = 3.465 V			150	µA
		nREF_OE	$V_{DD} = V_{IN}$ = 3.465V			5	µA
I_{IL}	Input Low Current	REF_IN, REF_SEL, BYPASS, MR/nOE, FSEL0, FSEL1	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		nREF_OE	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{OH}	Ouput High Voltage; NOTE 1	REF_OUT	V_{DD} = 3.465V	2.6			V
V_{OL}	Ouput Low Voltage; NOTE 1	REF_OUT	V_{DD} = 3.465V			0.5	V
Z_{OUT}	Output Impedance	REF_OUT	V_{DD} = 3.465V		20		Ω

NOTE 1: Outputs terminated with 50Ω to V_{DD}/2. See Parameter Measurement Information Section, Output Load Test Circuit diagram.

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

NOTE: Characterized using an 18pF parallel resonant crystal.

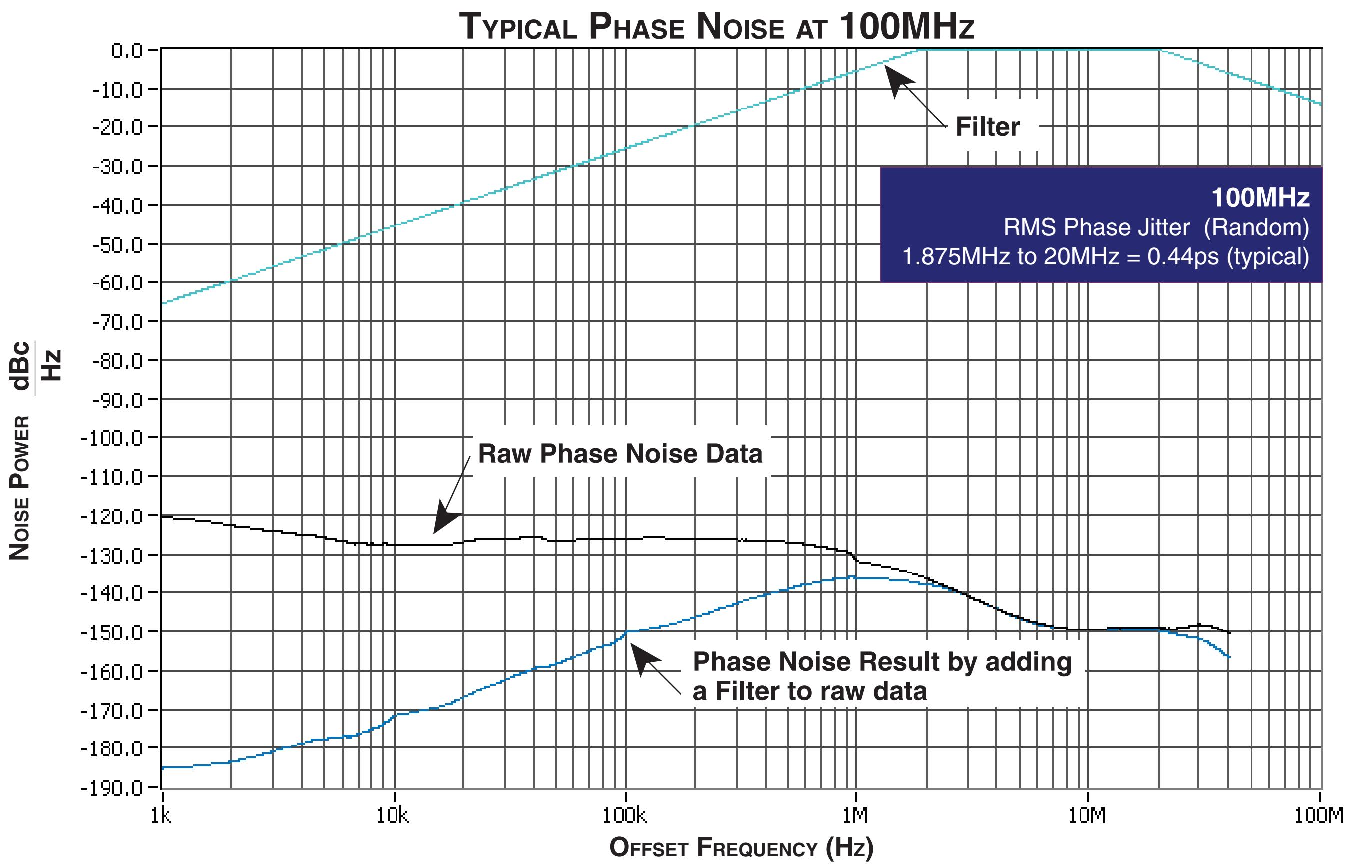
Table 6A. LVCMOS AC Characteristics, V_{DD} = 3.3V±5%, TA = -40°C to 85°C

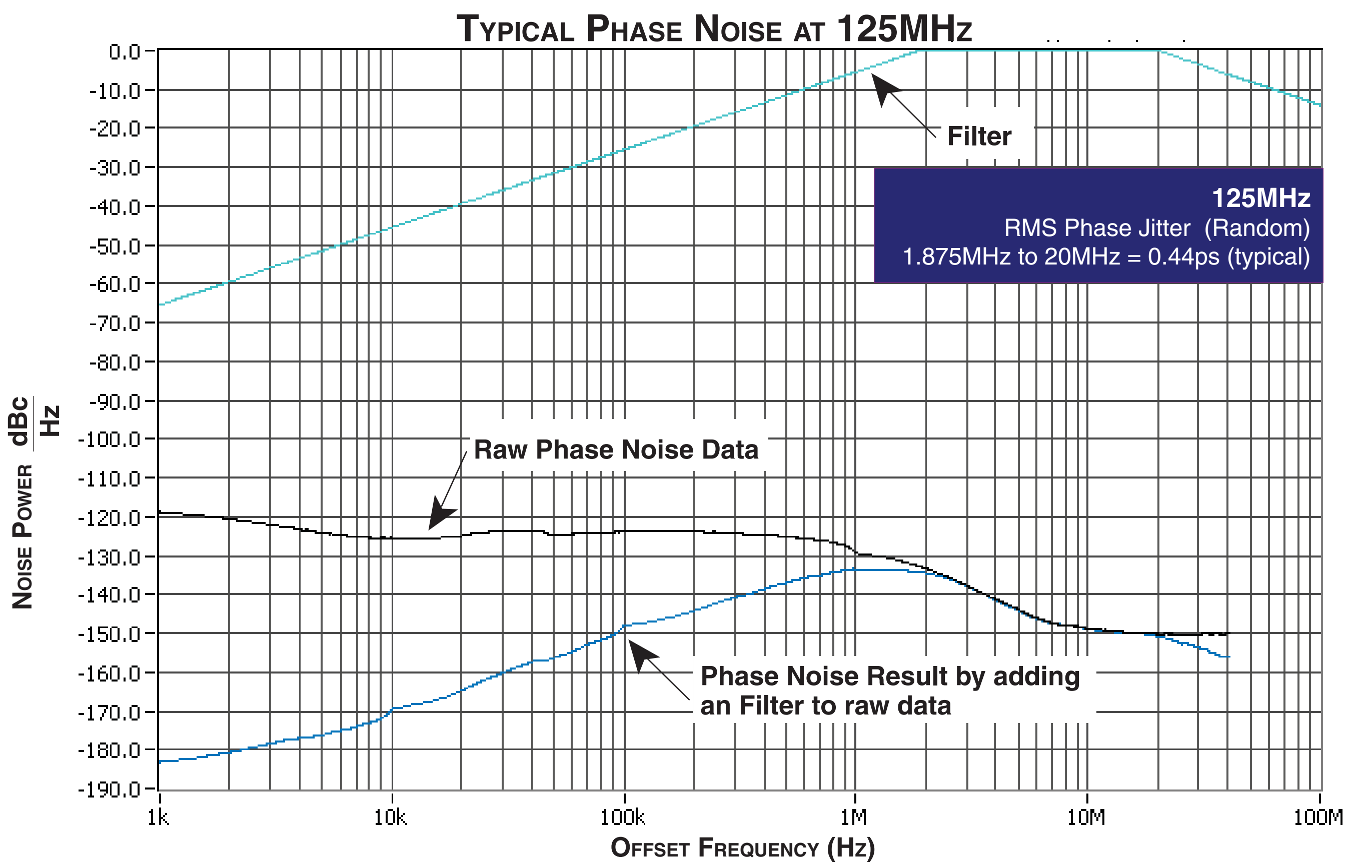
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency	REF_OUT			25		MHz
t_R / t_F	Output Rise/Fall Time		20% to 80%	0.60		1.80	ns
odc	Output Duty Cycle			49		51	%

Table 6B. HCSL AC Characteristics, $V_{DD} = V_{DDOA} = V_{DDOB}$ = 3.3V±5%, TA = -40°C to 85°C

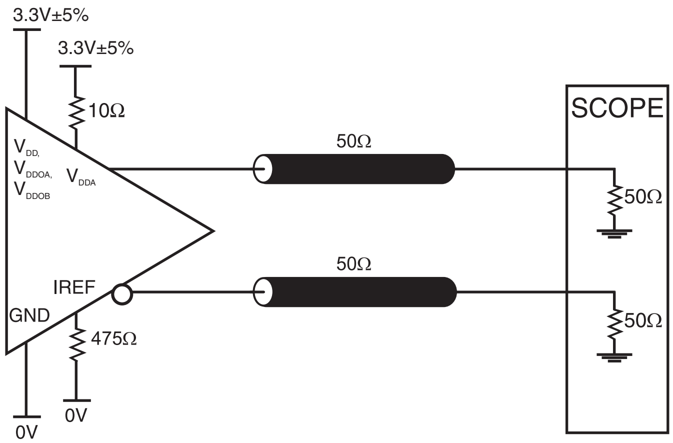
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency		VCO/5		100		MHz
			VCO/4		125		MHz
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 1		100MHz, (1.875MHz - 20MHz)		0.44		ps
			125MHz, (1.875MHz - 20MHz)		0.44		ps
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 3					35	ps
*t*sk(o)	Output Skew; NOTE 2, 3	QAx/nQAx, QBx/nQBx				100	ps
t_L	PLL Lock Time					100	ms
V_{HIGH}	Voltage High		125MHz	650	700	950	mV
V_{LOW}	Voltage Low			-150		150	mV
V_{OVS}	Max. Voltage, Overshoot					0.3	V
V_{UDS}	Min. Voltage, Undershoot			-0.3			V
V_{rb}	Ringback Voltage					0.2	V
V_{CROSS}	Absolute Crossing Voltage			200		550	mV
ΔV_{CROSS}	Total Variation of V_{CROSS} over all edges					160	mV
t_R / t_F	Output Rise/Fall Time	QAx/nQAx, QBx/nQBx	measured between 0.175V to 0.525V	100		700	ps
$\Delta t_R / \Delta t_F$	Rise/Fall Time Variation					125	ps
odc	Output Duty Cycle	QAx/nQAx, QBx/nQBx		48		52	%

NOTE: All specifications are taken at 100MHz and 125MHz.
NOTE 1: Please refer to the Phase Noise Plot.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

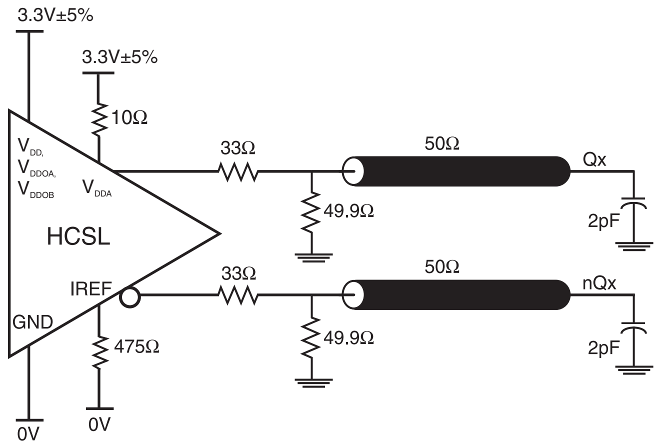

Typical Phase Noise at 100MHz
0.0
-10.0
-20.0
-30.0
-40.0
-50.0
-60.0
-70.0
-80.0
-90.0
-100.0
-110.0
-120.0
-130.0
-140.0
-150.0
-160.0
-170.0
-180.0
-190.0
Noise Power dBc/Hz
Filter
100MHz
RMS Phase Jitter (Random)
1.875MHz to 20MHz = 0.44ps (typical)
Raw Phase Noise Data
Phase Noise Result by adding
a Filter to raw data
1k
10k
100k
1M
10M
100M
Offset Frequency (Hz)


Typical Phase Noise at 125MHz
0.0
-10.0
-20.0
-30.0
-40.0
-50.0
-60.0
-70.0
-80.0
-90.0
-100.0
-110.0
-120.0
-130.0
-140.0
-150.0
-160.0
-170.0
-180.0
-190.0
Noise Power dBc/Hz
Filter
125MHz
RMS Phase Jitter (Random)
1.875MHz to 20MHz = 0.44ps (typical)
Raw Phase Noise Data
Phase Noise Result by adding
an Filter to raw data
1k
10k
100k
1M
10M
100M
Offset Frequency (Hz)

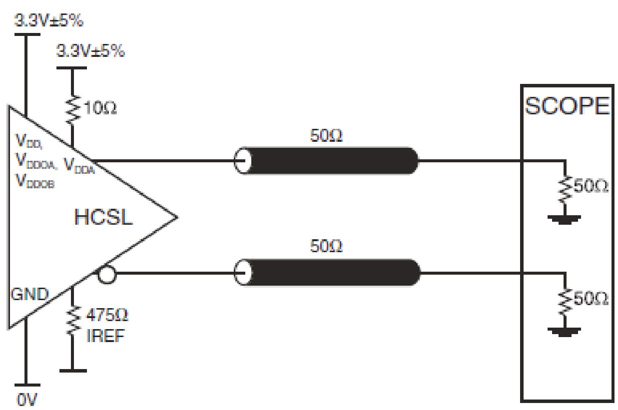
Parameter Measurement Information



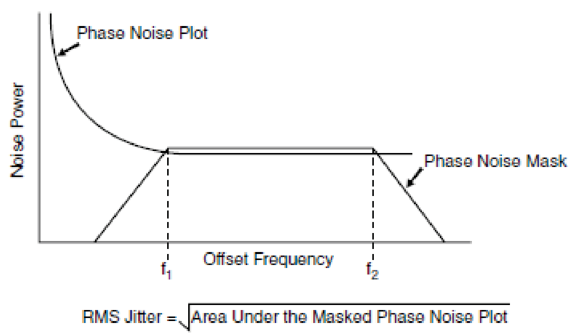
HCSL Output Load AC Test Circuit



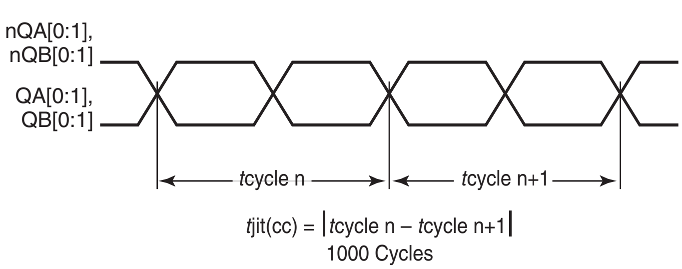
HCSL Output Load AC Test Circuit



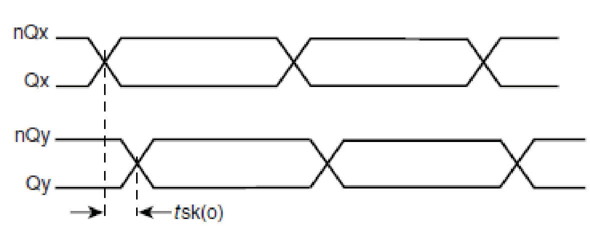
3.3V LVCMOS Output Load AC Test Circuit



RMS Phase Jitter

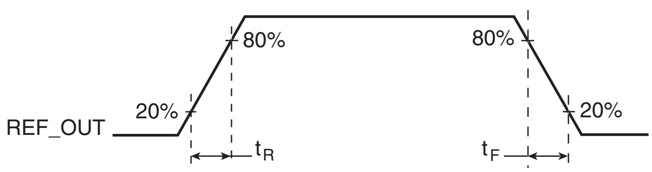


Cycle-to-Cycle Jitter

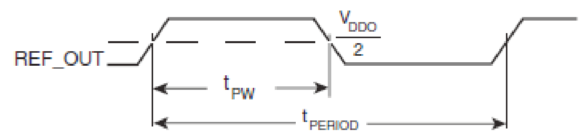


HCSL Output Skew

Parameter Measurement Information, continued

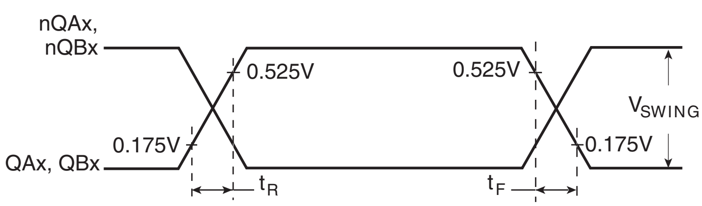


LVCMOS Output Rise/Fall Time

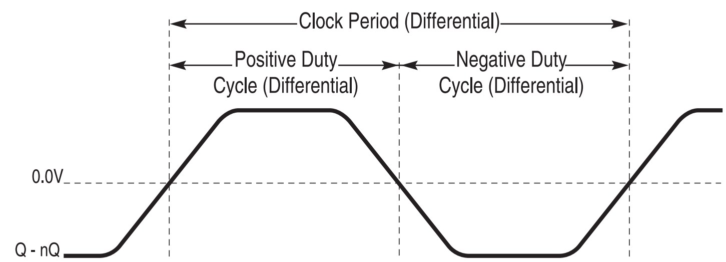


$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

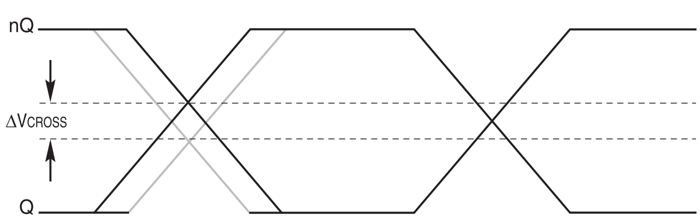
LVCMOS Output Duty Cycle/Pulse Width/Period



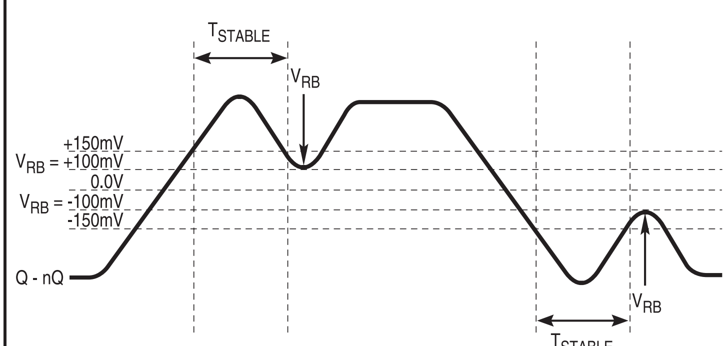
Differential Measurement Points for Rise/Fall Time



Differential Measurement Points for Duty Cycle/Period

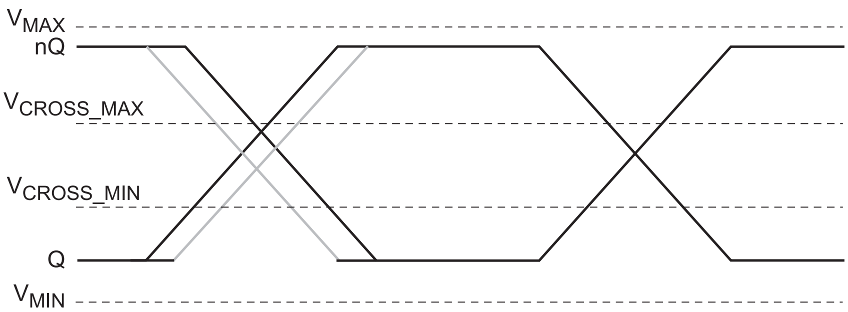


SE Measurement Points for Delta Cross Point



Differential Measurement Points for Ringback

Parameter Measurement Information, continued



SE Measurement Points for Absolute Cross Point/Swing

Application Information

Power Supply Filtering Techniques

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 841654 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA}, V_{DDOA} and V_{DDOB} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional10Ω resistor along with a 10µF bypass capacitor be connected to the V_{DDA} pin.

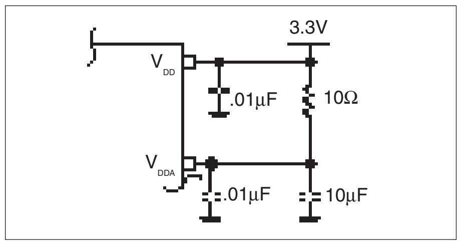


Figure 1. Power Supply Filtering

Recommendations for Unused Input and Output Pins

Inputs:

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

REF_IN Input

For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the REF_IN to ground.

LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

HCSL Outputs

All unused HCSL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

LVCMOS Output

The unused LVCMOS output can be left floating. We recommend that there is no trace attached.

Crystal Input Interface

The 841654 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.

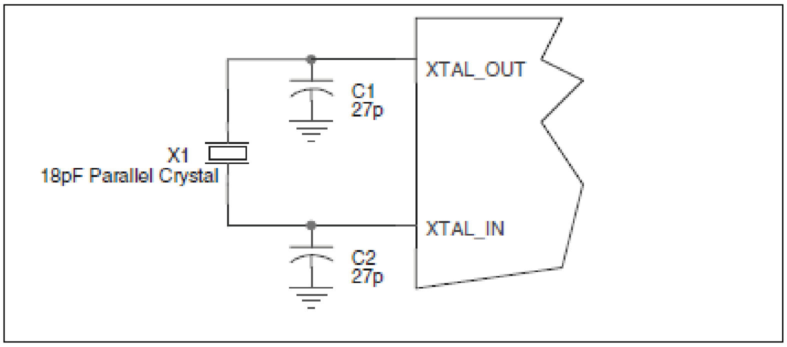


Figure 2. Crystal Input Interface

LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC couple capacitor. A general interface diagram is shown in *Figure 3.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

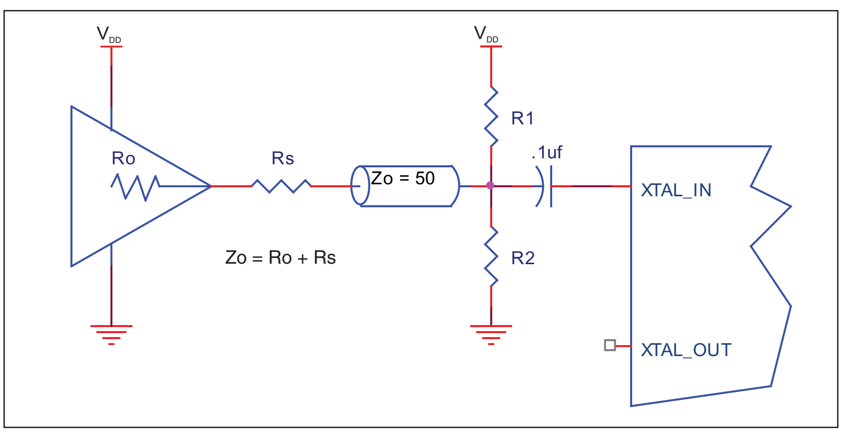


Figure 3. General Diagram for LVCMOS Driver to XTAL Input Interface

Schematic Layout

Figure 4 shows an example of 841654 application schematic. In this example, the device is operated at V_{CC} = 3.3V. The 18pF parallel resonant 25MHz crystal is used. The C1 = 27pF and C2 = 27pF are recommended for frequency accuracy. For different board layout, the C1 and C2 may be slightly adjusted for optimizing frequency accuracy. One example of HCSL and one example of LVCMOS terminations are shown in this schematic. The decoupling capacitors should be located as close as possible to the power pin.

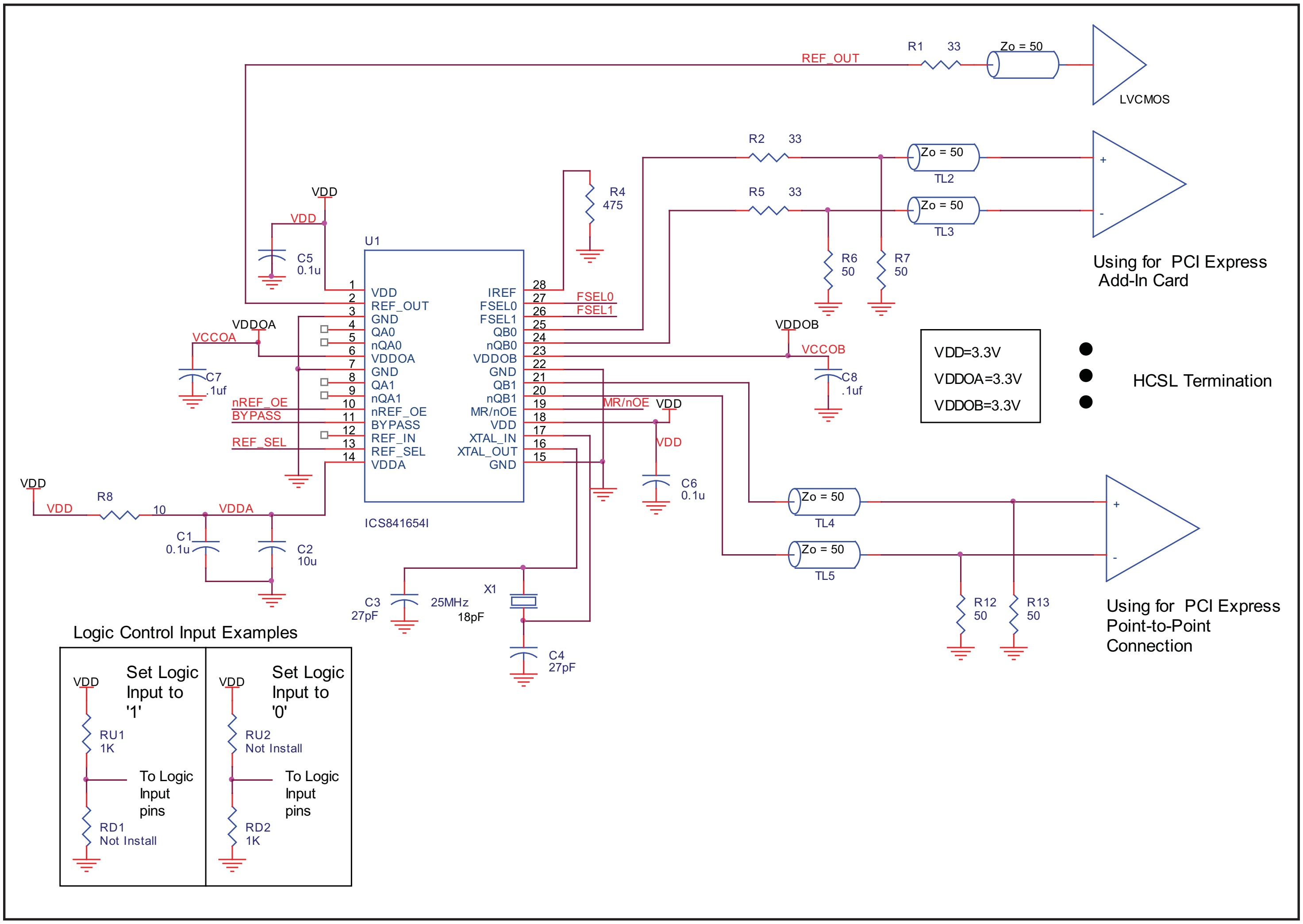


Figure 4. 841654 Schematic Layout

Power Considerations

This section provides information on power dissipation and junction temperature for the 841654.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 841654 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{DD_MAX} * I_{DD_MAX} = 3.465V * 85mA = **294.5mW**
- Power (outputs)$_{MAX}$ = **50.06mW/Loaded Output pair**
  If all outputs are loaded, the total power is 4 * 50.06mW = **200.24mW**

Total Power $_{\_MAX}$ (3.465V, with all outputs switching) = 294.5mW + 200.24mW = 494.74mW

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in Section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 64.5°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 0.495W * 64.5°C/W = 116.9°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

Table 7. Thermal Resistance θ_{JA} for 28-Lead TSSOP, Forced Convection

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	64.5°C/W	60.4°C/W	58.5°C/W

3. Calculations and Equations.

The purpose of this section is to calculate power dissipation on the IC per HCSL output pair.

HCSL output driver circuit and termination are shown in *Figure 4.*

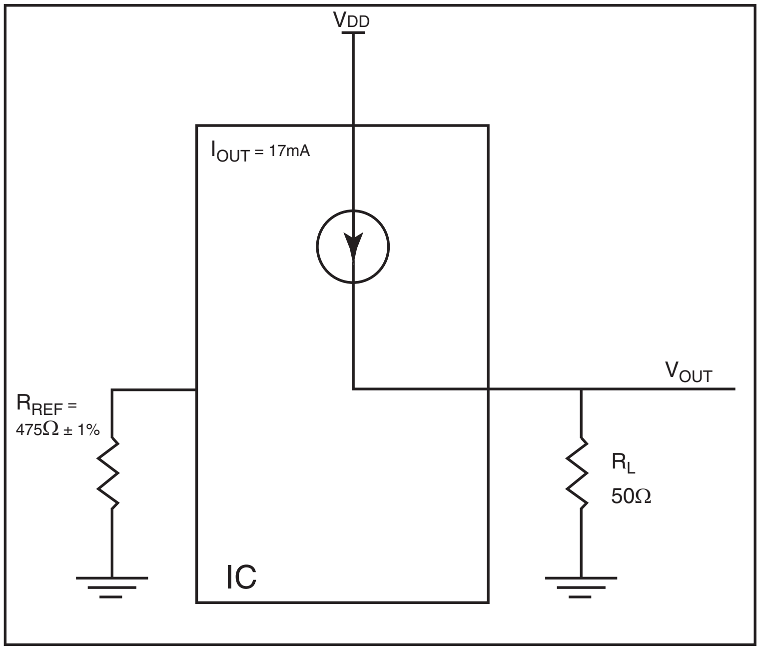


FIGURE 4. HCSL DRIVER CIRCUIT AND TERMINATION

HCSL is a current steering output which sources a maximum of 17mA of current per output. To calculate worst case on-chip power dissipation, use the following equations which assume a 50Ω load to ground.

The highest power dissipation occurs when V_{DD} is HIGH.

Power = $(V_{DD\_HIGH} - V_{OUT}) * I_{OUT}$, since $V_{OUT} = I_{OUT} * R_L$

$= (V_{DD\_HIGH} - I_{OUT} * R_L) * I_{OUT}$

$= (3.465V - 17mA * 50\Omega) * 17mA$

Total Power Dissipation per output pair = **50.06mW**

Recommended Termination

Figure 5A is the recommended termination for applications which require the receiver and driver to be on a separate PCB. All traces should be 50Ω impedance.

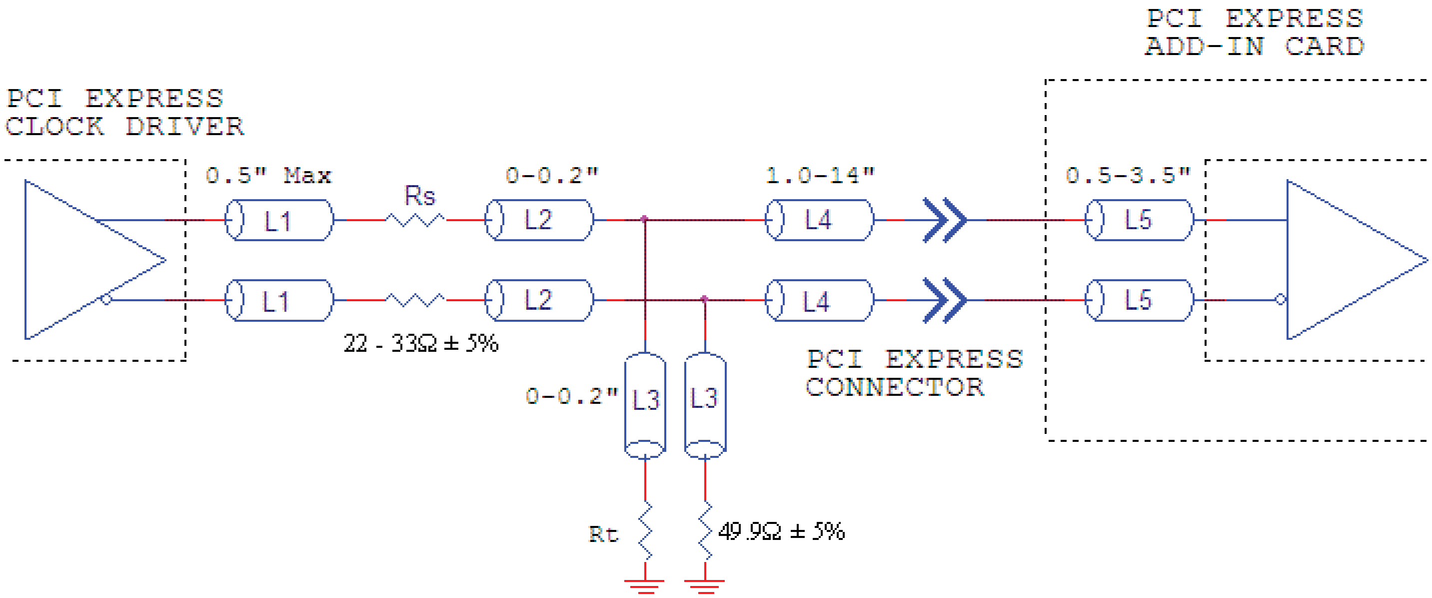


Figure 5A. Recommended Termination

Figure 5B is the recommended termination for applications which require a point to point connection and contain the driver and receiver on the same PCB. All traces should all be 50Ω impedance.

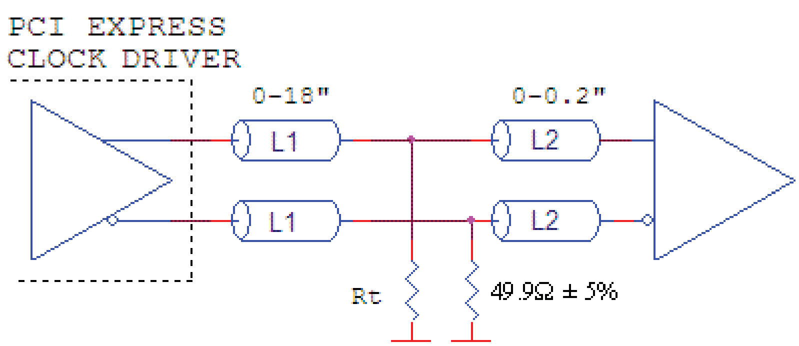


Figure 5B. Recommended Termination

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for 28 Lead TSSOP

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	64.5°C/W	60.4°C/W	58.5°C/W

Transistor Count

The transistor count for 841654 is: 2954

Package Outline and Package Dimensions

Package Outline - G Suffix for 28 Lead TSSOP

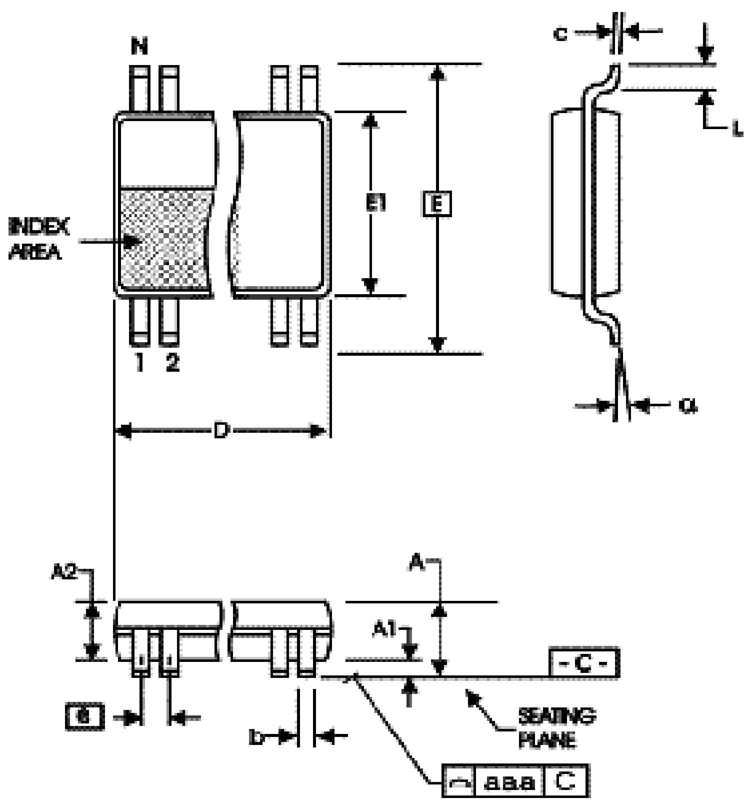


Table 9. Package Dimensions

SYMBOL	Millimeters	
	Minimum	Maximum
N	28	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	9.60	9.80
E	8.10 BASIC	
E1	6.00	6.20
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 10. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS841654AGILF	ICS841654AGILF	28 Lead “Lead-Free” TSSOP	tube	-40°C to 85°C
ICS841654AGILFT	ICS841654AGILF	28 Lead “Lead-Free” TSSOP	tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an “LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	T10	16	Ordering Information - removed leaded devices. Updated data sheet format.	4/20/15

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/