RENESAS

FemtoClock® Crystal-to-3.3V LVPECL Frequency Synthesizer

8430252I-45

DATASHEET

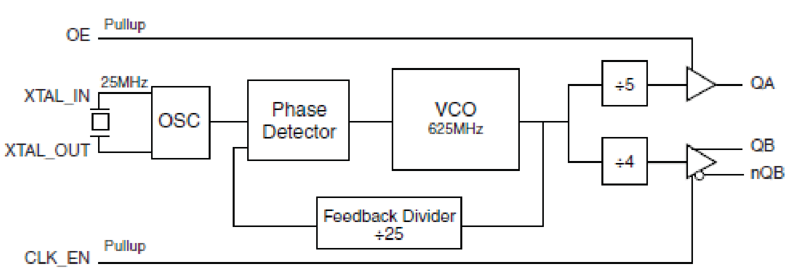
General Description

The 8430252I-45 is a 2 output LVPECL and LVCMOS/LVTTL Synthesizer optimized to generate Ethernet reference clock frequencies. Using a 25MHz, 18pF parallel resonant crystal, the following fre-quencies can be generated: 156.25MHz LVPECL output and, 125MHz LVCMOS output. The 8430252I-45 uses IDT's 3[RD] generation low phase noise VCO technology and can achieve 1ps or lower typical rms phase jitter, easily meeting Ethernet jitter requirements. The 8430252I-45 is packaged in a small 16-pin TSSOP package.

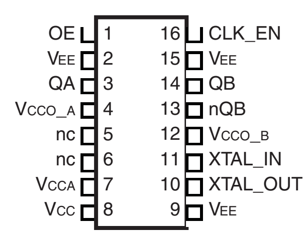
Features

- One differential 3.3V LVPECL output and One LVCMOS/LVTTL output
- Crystal oscillator interface designed for a 25MHz, 18pF parallel resonant crystal
- A 25MHz crystal generates both an output frequency of 156.25MHz (LVPECL) and 125MHz (LVCMOS)
- VCO frequency: 625MHz
- RMS phase jitter @ 156.25MHz (1.875MHz - 20MHz) using a 25MHz crystal: 0.39ps (typical)
- Full 3.3V supply mode
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Block Diagram



Pin Assignment



8430252I-45
16-Lead TSSOP
4.4mm x 5.0mm x 0.92mm package body
G Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	OE	Input	Pullup	Output enable pin. LVCMOS/LVTTL interface levels. See Table 3A Function Table.
2, 9, 15	V_{EE}	Power		Negative supply pins.
3	QA	Output		LVCMOS/LVTTL clock output.
4	V_{CCO_A}	Power		Output supply pin for QA output.
5, 6	nc	Unused		No connect.
7	V_{CCA}	Power		Analog supply pin.
8	V_{CC}	Power		Core supply pin.
10, 11	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
12	V_{CCO_B}	Power		Output supply pin for QB, nQB outputs.
13, 14	nQB, QB	Output		Differential clock outputs. LVPECL interface levels.
16	CLK_EN	Input	Pullup	Clock enable pin. LVCMOS/LVTTL interface levels. See Table 3B Function Table.

NOTE: Pullup refers to internal input resistors. See Table 2, Pin Characterisitcs, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				4		pF
C_{PD}	Power Dissipation Capacitance		V_{CC}, V_{CCA}, $V_{CCO\_A,}$ V_{CCO_B} = 3.465V		18		pF
R_{PULLUP}	Input Pullup Resistor				51		kΩ
R_{OUT}	Output Impedance	QA	V_{CCO_A} = 3.3V		20		Ω

TABLE 3A. OE SELECT FUNCTION TABLE

Input	Output
OE	**QA**
0	Hi-Z
1	Active

TABLE 3B. CLK_EN SELECT FUNCTION TABLE

Input	Outputs	
CLK_EN	**QB**	**nQB**
0	Low	High
1	Active	Active

Absolute Maximum Ratings

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	89°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{CC} = V_{CCA} = V_{CCO\_A,}\ V_{CCO\_B}$ = 3.3V±5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		V_{CC} – 0.10	3.3	V_{CC}	V
$V_{CCO\_A,}\ V_{CCO\_B}$	Output Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				95	mA
I_{CCA}	Analog Supply Current				10	mA

Table 4B. LVCMOS / LVTTL DC Characteristics, $V_{CC} = V_{CCA} = V_{CCO\_A}$ = 3.3V±5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	OE, CLK_EN	$V_{CC} = V_{IN}$ = 3.465V			5	
I_{IL}	Input Low Current	OE, CLK_EN	V_{CC} = 3.465V, V_{IN} = 0V	-150			
V_{OH}	Output High Voltage; NOTE 1			2.6			V
V_{OL}	Output Low Voltage; NOTE 1					0.5	V

NOTE 1: Outputs terminated with 50Ω to V_{CCO_A}/2. See Parameter Measurement Information Section, "3.3V Output Load Test Circuit".

Table 4C. LVPECL DC Characteristics, $V_{CC} = V_{CCA} = V_{CCO\_B}$ = 3.3V±5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CCO_B} - 1.4		V_{CCO_B} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CCO_B} - 2.0		V_{CCO_B} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CCO_B} - 2V.

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

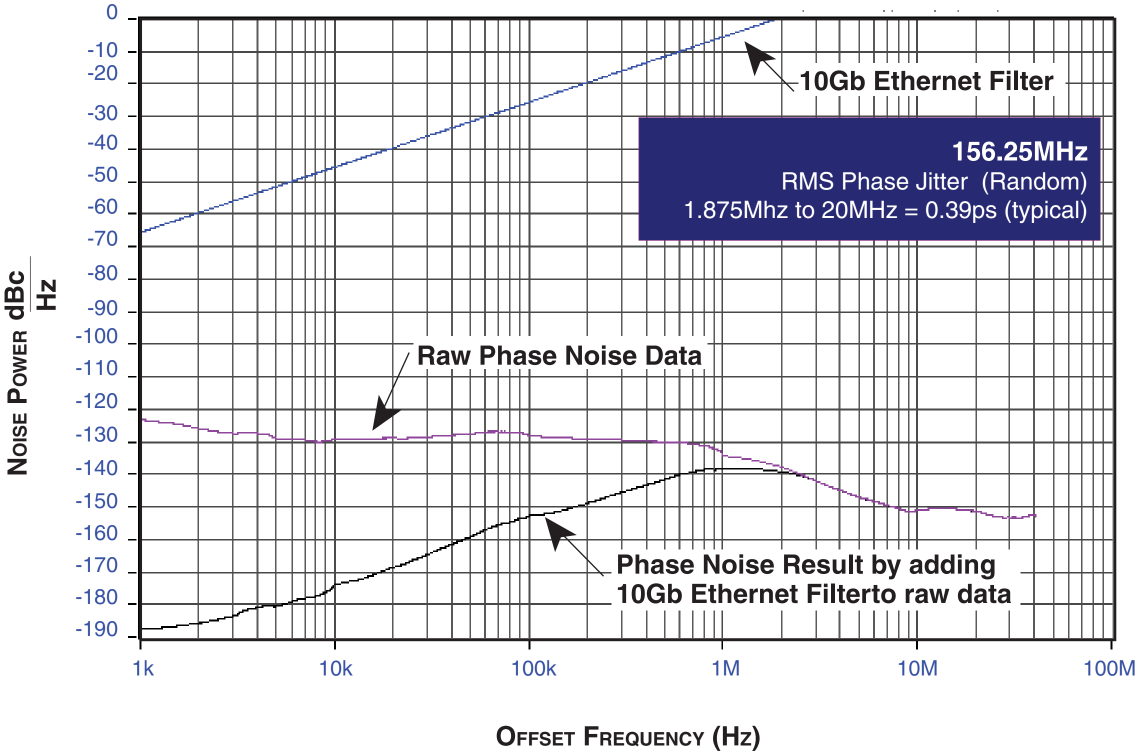
NOTE: Characterized using an 18pF parallel resonant crystal.

Table 6. AC Characteristics, $V_{CC} = V_{CCA} = V_{CCO\_A,}\ V_{CCO\_B} = 3.3V \pm 5\%$, $T_A = -40°C$ to $85°C$

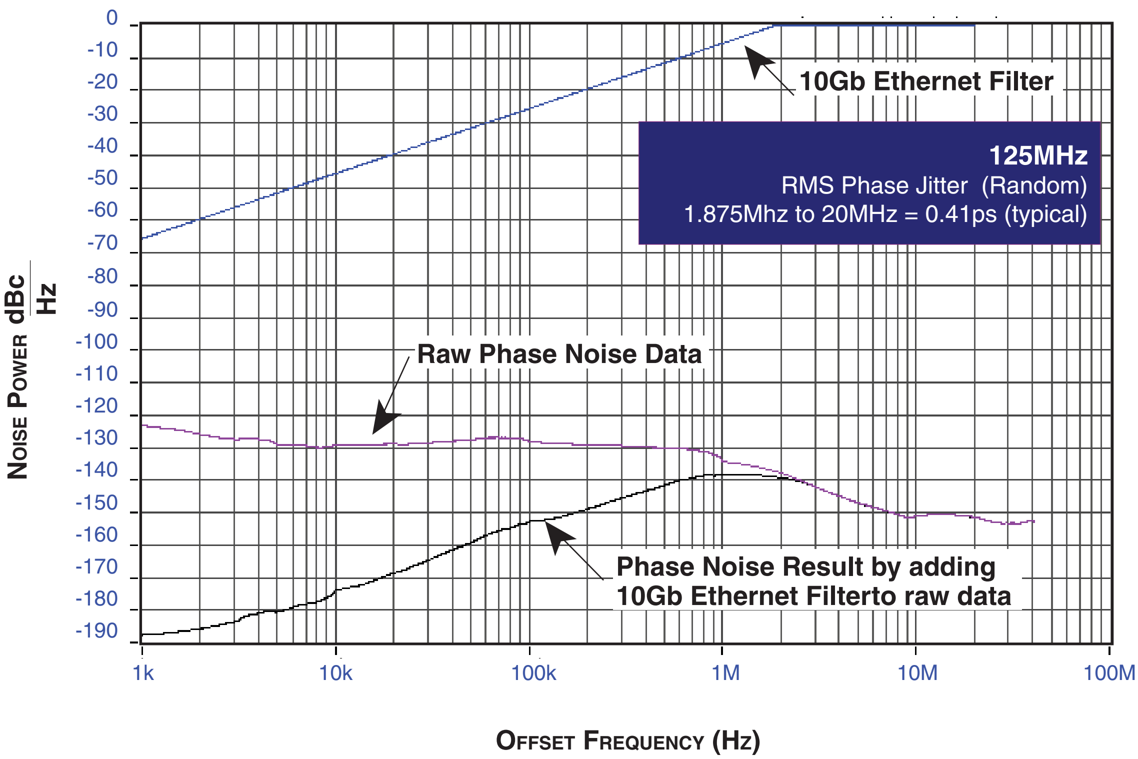
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency Range				156.25		MHz
					125		MHz
tjit(Ø)	RMS Phase Jitter (Random); NOTE 1	QA	125MHz (1.875MHz - 20MHz)		0.41		ps
		QB, nQB	156.25MHz (1.875MHz - 20MHz)		0.39		ps
t_R / t_F	Output Rise/Fall Time	QA	20% to 80%	500		1200	ps
		QB, nQB		300		700	ps
odc	Output Duty Cycle	QA		47		53	%
		QB, nQB		48		52	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Please refer to the Phase Noise Plots.

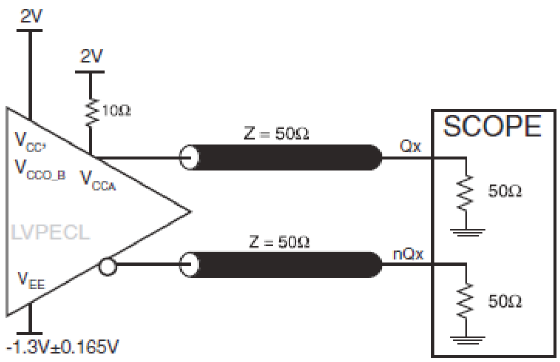
Typical Phase Noise at 156.25MHz



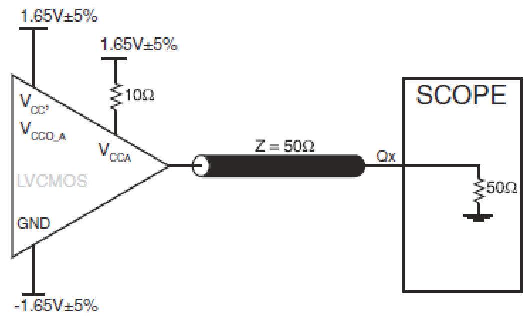
Typical Phase Noise at 125MHz



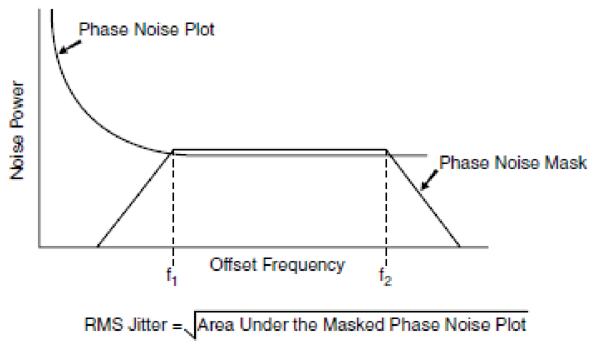
Parameter Measurement Information



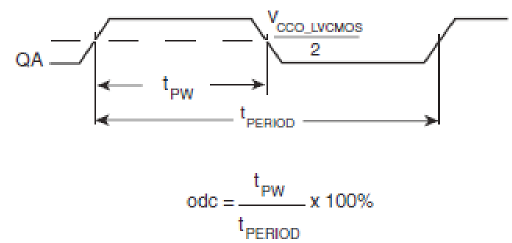
3.3V Core/3.3V LVPECL Output Load AC Test Circuit



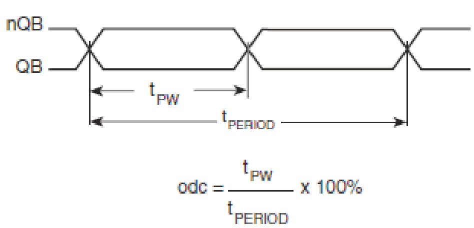
3.3V Core/3.3V LVCMOS Output Load AC Test Circuit



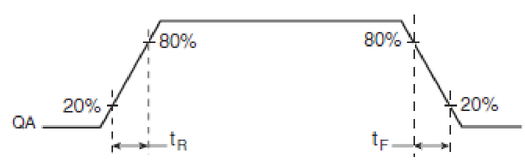
RMS Phase Jitter



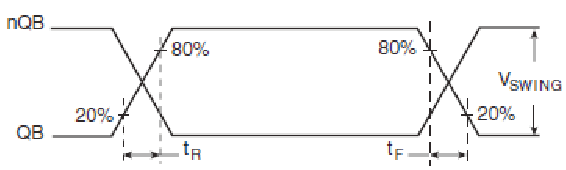
LVCMOS Output Duty Cycle/Pulse Width/Period



LVPECL Output Duty Cycle/Pulse Width/Period



LVCMOS Output Rise/Fall Time



LVPECL Output Rise/Fall Time

Application Information

Power Supply Filtering Techniques

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 8430252I-45 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC}, V_{CCA}, and V_{CCO_X} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{CC} pin and also shows that V_{CCA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{CCA} pin.

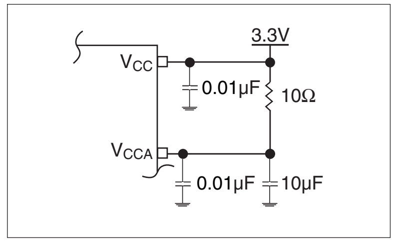


Figure 1. Power Supply Filtering

Recommendations for Unused Input and Output Pins

Inputs:

Select Pins:

All select pins have internal pullups; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVCMOS Output:

All unused LVCMOS output can be left floating. We recommend that there is no trace attached.

LVPECL Output:

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Crystal Input Interface

The 8430252I-45 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.

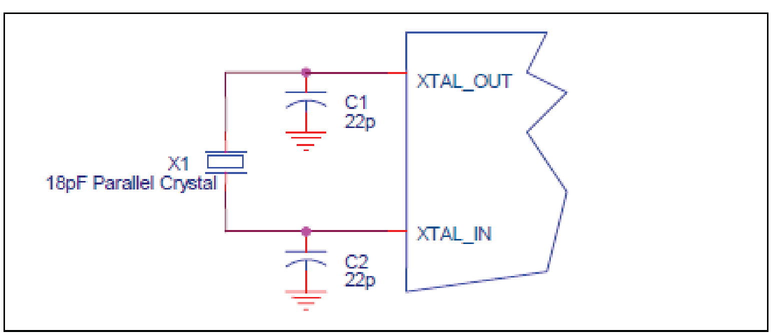


Figure 2. Crystal Input Interface

Over-Driving the Crystal Interface

The XTAL_IN input can a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3A.* The XTAL_OUT pin can be left floating. The maximum amplitude of the input signal should not exceed 2V and the input edge rate can be as slow as 10ns. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω. By overdring the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.

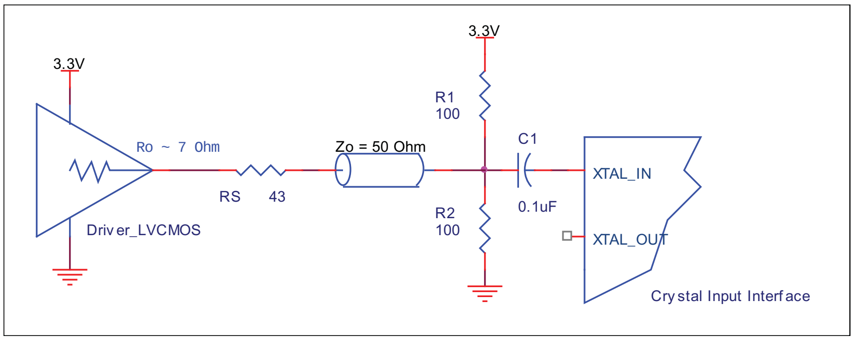


Figure 3A. General Diagram for LVCMOS Driver to XTAL Input Interface

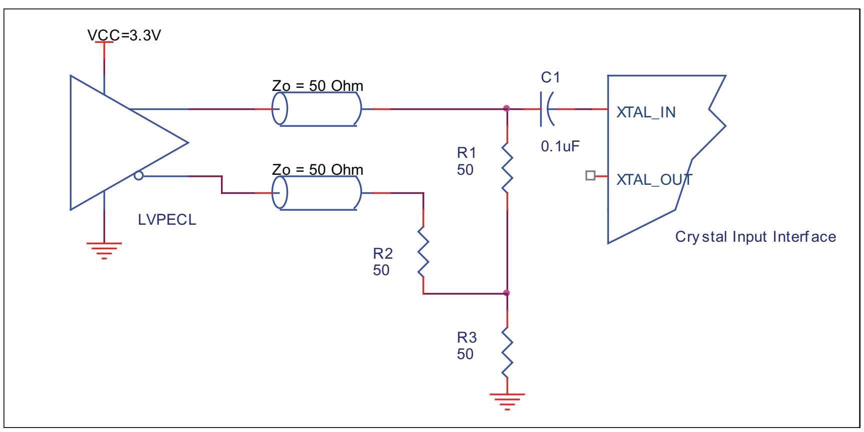


Figure 3B. General Diagram for LVPECL Driver to XTAL Input Interface

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

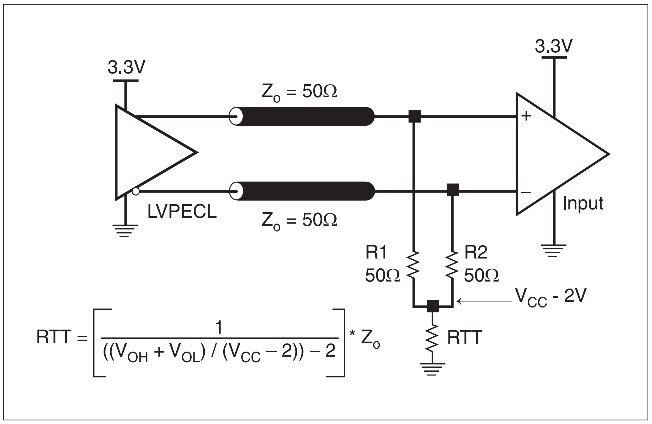


Figure 4A. LVPECL Output Termination

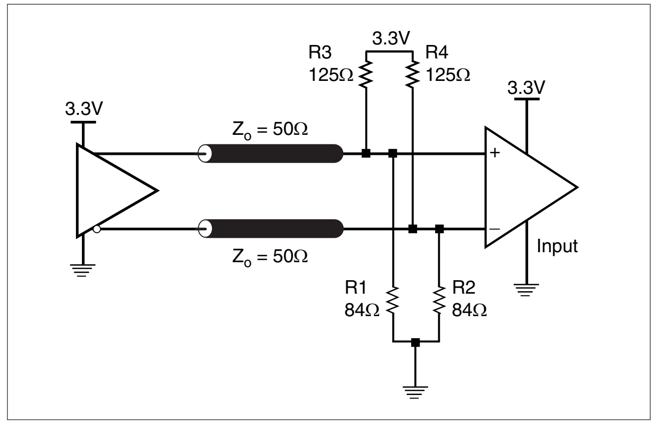


Figure 4B. LVPECL Output Termination

Layout Guideline

Figure 5 shows an example of 8430252I-45 application schematic. In this example, the device is operated at V_{CC} = 3.3V. The 18pF parallel resonant 25MHz crystal is used. The C1 = 22pF and C2 = 22pF are recommended for frequency accuracy. For different board layout, the C1 and C2 may be slightly adjusted for optimizing frequency accuracy. Two examples of LVPECL and one example of LVCMOS terminations are shown in this schematic. Additional termination approaches are shown in the LVPECL Termination Application Note.

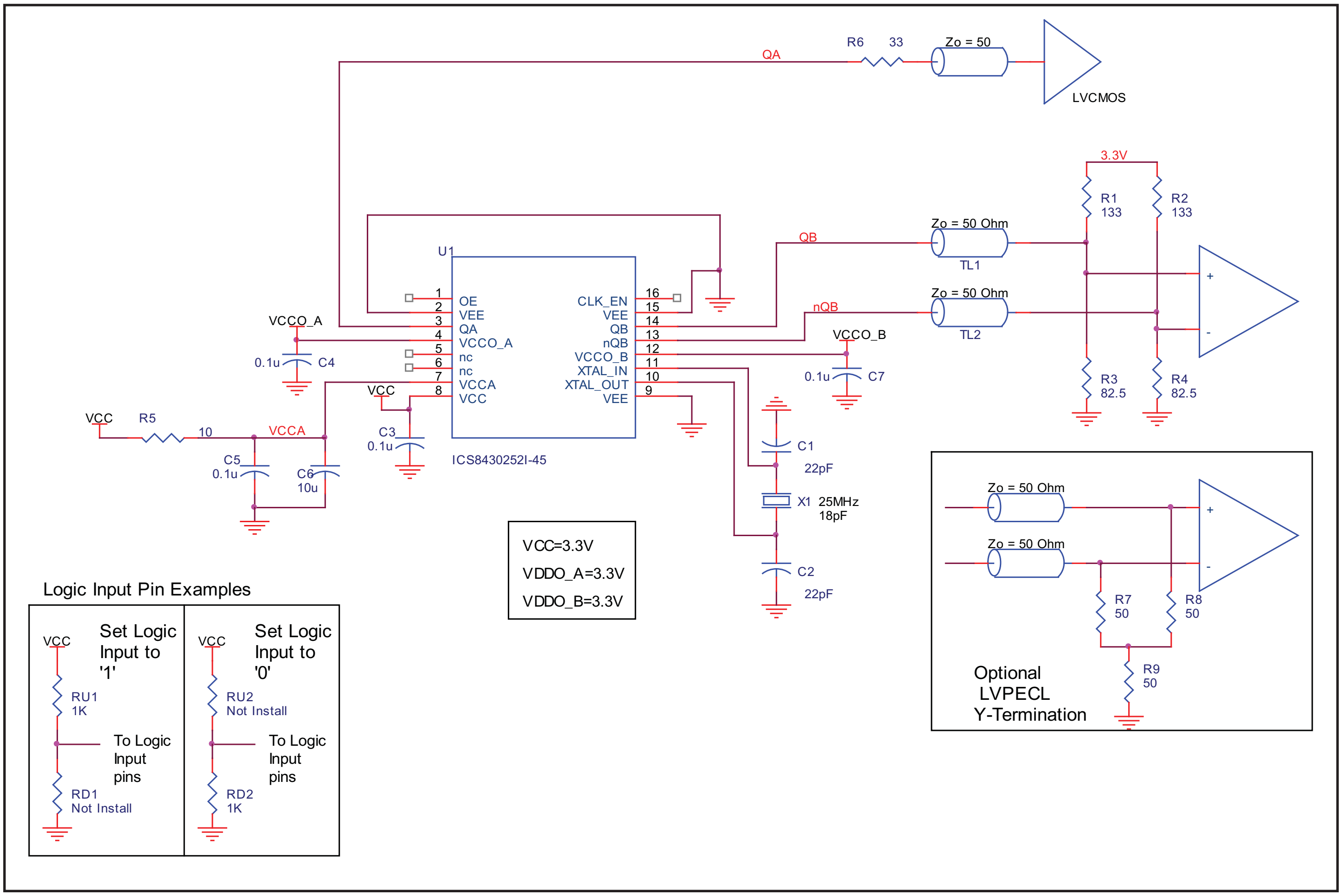


Figure 5. 8430252I-45 Schematic Example

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the 8430252I-45.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 8430252I-45 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 95mA = **329.17mW**

  (95mA includes the LVCMOS output terminated with 50Ω to V_{CC}/2 at 125MHz)
- Power (outputs)$_{MAX}$ = **30mW/Loaded Output pair**

Total Power $_{\_MAX}$ (3.465V, with all outputs switching) = 329.17mW + 30mW = **359.17mW**

2. Junction Temperature.

Junction temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 81.8°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.359W * 81.8°C/W = 114.4°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (multi-layer).

TABLE 7. THERMAL RESISTANCE θ_{JA} FOR 16-PIN TSSOP, FORCED CONVECTION

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	137.1°C/W	118.2°C/W	106.8°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	89.0°C/W	81.8°C/W	78.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

3. Calculations and Equations.

The purpose of this section is to calculate power dissipation on the IC per LVPECL output pair.

LVPECL output driver circuit and termination are shown in *Figure 6.*

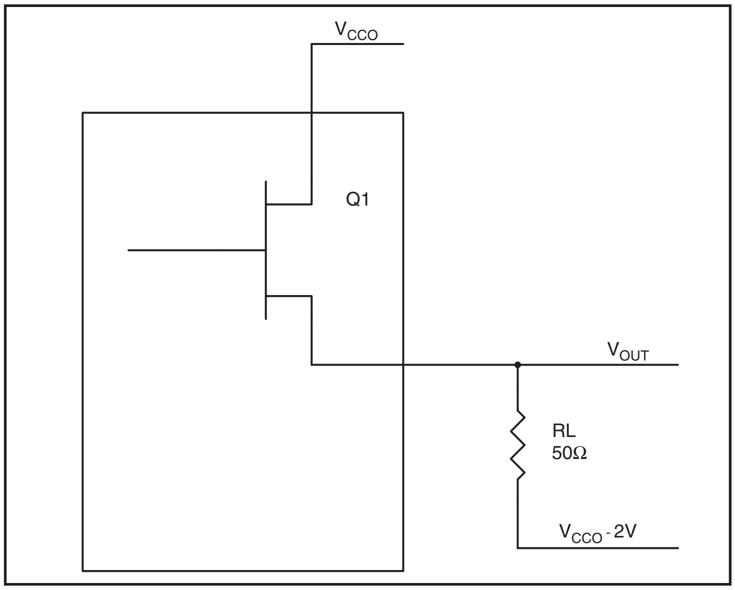


FIGURE 6. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CCO\_B} – 2V$.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CCO\_MAX} – 0.9V}$

  $(V_{CCO\_MAX} – V_{OH\_MAX}) = \mathbf{0.9V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CCO\_MAX} – 1.7V}$

  $(V_{CCO\_MAX} – V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CCO\_MAX} – 2V))/R_L] * (V_{CCO\_MAX} – V_{OH\_MAX}) = [(2V – (V_{CCO\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} – V_{OH\_MAX}) =$

$[(2V – 0.9V)/50\Omega] * 0.9V = \mathbf{19.8mW}$

$Pd\_L = [(V_{OL\_MAX} – (V_{CCO\_MAX} – 2V))/R_L] * (V_{CCO\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CCO\_MAX} – V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} – V_{OL\_MAX}) =$

$[(2V – 1.7V)/50\Omega] * 1.7V = \mathbf{10.2mW}$

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

RELIABILITY INFORMATION

TABLE 8. θ_{JA} VS. AIR FLOW TABLE FOR 16 LEAD TSSOP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	137.1°C/W	118.2°C/W	106.8°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	89.0°C/W	81.8°C/W	78.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for 8430252I-45 is: 2070

PACKAGE OUTLINE AND DIMENSIONS

PACKAGE OUTLINE - G SUFFIX FOR 16 LEAD TSSOP

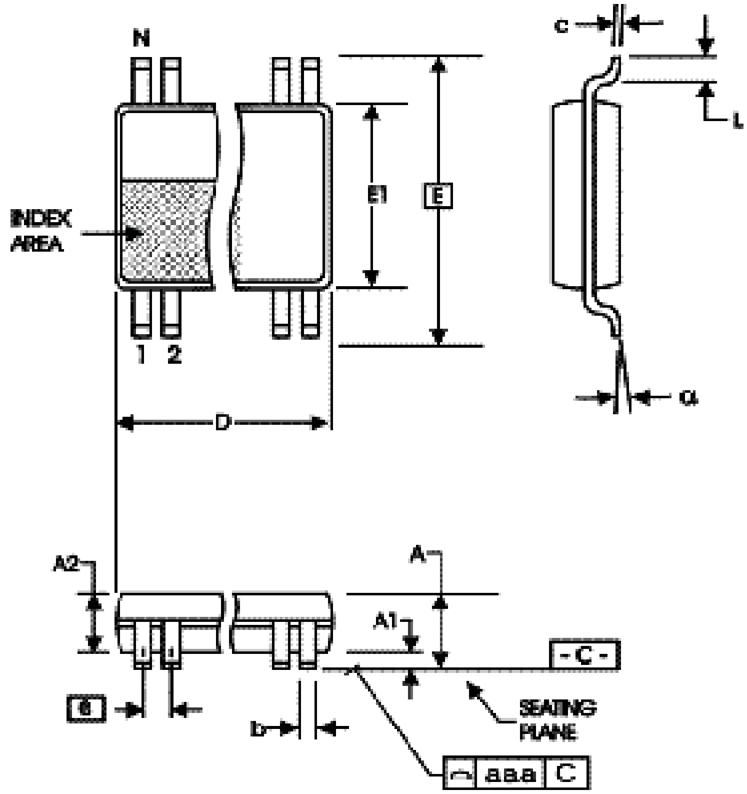


TABLE 9. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	16	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8430252CGI-45LF	252CI45L	16 Lead "Lead-Free" TSSOP	tube	-40°C to 85°C
8430252CGI-45LFT	252CI45L	16 Lead "Lead-Free" TSSOP	2500 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
A	T6 T10	4 7 8 9 15	AC Characteristics Table - added thermal note. Power Supply Filtering Techniques - updated text. Updated Over-Driving the Crystal Interface section. Termination for 3.3V LVPECL Outputs - updated Figures 4A and 4B. Ordering Information Table - deleted ICS prefix in Part/Order column. Added LF marking.	11/3/10
B	T10	15	Ordering Information - removed leaded devices. Updated datasheet format.	12/9/14

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