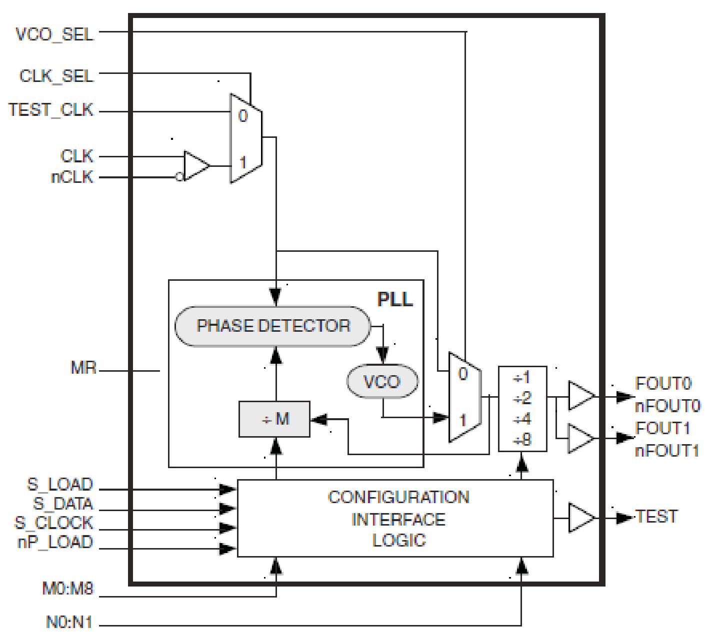
General Description

The 8432I-101 is a general purpose, dual output Differential-to-3.3V LVPECL high frequency synthesizer and a member of the family of High Performance Clock Solutions from IDT. The 8432I-101 has a selectable TEST_CLK or CLK, nCLK inputs. The TEST_CLK input accepts LVCMOS or LVTTL input levels and translates them to 3.3V LVPECL levels. The CLK, nCLK pair can accept most standard differential input levels. The VCO operates at a frequency range of 250MHz to 700MHz. The VCO frequency is programmed in steps equal to the value of the input differential or single ended reference frequency. The VCO and output frequency can be programmed using the serial or parallel interfaces to the configuration logic. The low phase noise characteristics of the 8432I-101 makes it an ideal clock source for Gigabit Ethernet and SONET applications.

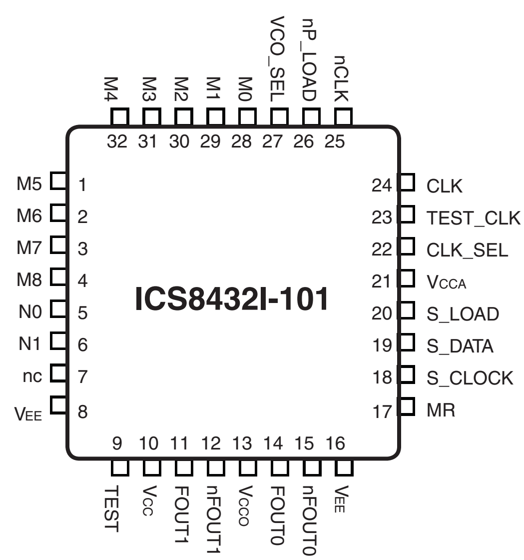
Features

- Dual differential 3.3V LVPECL outputs
- Selectable CLK, nCLK or LVCMOS/LVTTL TEST_CLK
- TEST_CLK can accept the following input levels: LVCMOS or LVTTL
- CLK, nCLK pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- CLK, nCLK or TEST_CLK maximum input frequency: 40MHz
- Output frequency range: 25MHz to 700MHz
- VCO range: 250MHz to 700MHz
- Accepts any single-ended input signal on CLK input with resistor bias on nCLK input
- Parallel interface for programming counter and output dividers
- RMS period jitter: 5ps (maximum)
- Cycle-to-cycle jitter: 25ps (maximum)
- 3.3V supply voltage
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Block Diagram



Pin Assignment



32-Lead LQFP
7mm x 7mm x 1.4mm package body
Y Package
Top View

Functional Description

NOTE: The functional description that follows describes operation using a 25MHz clock input. Valid PLL loop divider values for different input frequencies are defined in the Input Frequency Characteristics, Table 5, NOTE 1.

The 8432I-101 features a fully integrated PLL and therefore requires no external components for setting the loop bandwidth. A differential clock input is used as the input to the 8432I-101. This input is fed into the phase detector. A 25MHz clock input provides a 25MHz phase detector reference frequency. The VCO of the PLL operates over a range of 250MHz to 700MHz. The output of the M divider is also applied to the phase detector.

The phase detector and the M divider force the VCO output frequency to be M times the reference frequency by adjusting the VCO control voltage. Note, that for some values of M (either too high or too low), the PLL will not achieve lock. The output of the VCO is scaled by a divider prior to being sent to each of the LVPECL output buffers. The divider provides a 50% output duty cycle.

The programmable features of the 8432I-101 support two input modes to program the PLL M divider and N output divider. The two input operational modes are parallel and serial. *Figure1* shows the timing diagram for each mode. In parallel mode, the nP_LOAD input is initially LOW. The data on inputs M0 through M8 and N0 and N1 is passed directly to the M divider and N output divider. On the LOW-to-HIGH transition of the nP_LOAD input, the data is latched and the M divider remains loaded until the next LOW transition on nP_LOAD or until a serial event occurs. As a result, the M and N bits can be hardwired to set the M divider and N output divider to a specific default state that will automatically occur during power-up. The TEST output is LOW when operating in the parallel input mode. The relationship between the VCO frequency, the input frequency and the M divider is defined as follows: $fVCO = f_{IN} \times M$

The M value and the required values of M0 through M8 are shown in Table 3B, Programmable VCO Frequency Function Table. Valid M values for which the PLL will achieve lock for a 25MHz reference are defined as $8 \le M \le 28$. The frequency out is defined as follows:

$$fOUT = \frac{fVCO}{N} = f_{IN} \times \frac{M}{N}$$

Serial operation occurs when nP_LOAD is HIGH and S_LOAD is LOW. The shift register is loaded by sampling the S_DATA bits with the rising edge of S_CLOCK. The contents of the shift register are loaded into the M divider and N output divider when S_LOAD transitions from LOW-to-HIGH. The M divide and N output divide values are latched on the HIGH-to-LOW transition of S_LOAD. If S_LOAD is held HIGH, data at the S_DATA input is passed directly to the M divider and N output divider on each rising edge of S_CLOCK. The serial mode can be used to program the M and N bits and test bits T1 and T0. The internal registers T0 and T1 determine the state of the TEST output as follows:

T1	T0	TEST Output
0	0	LOW
0	1	S_Data, Shift Register Input
1	0	Output of M divider
1	1	CMOS Fout

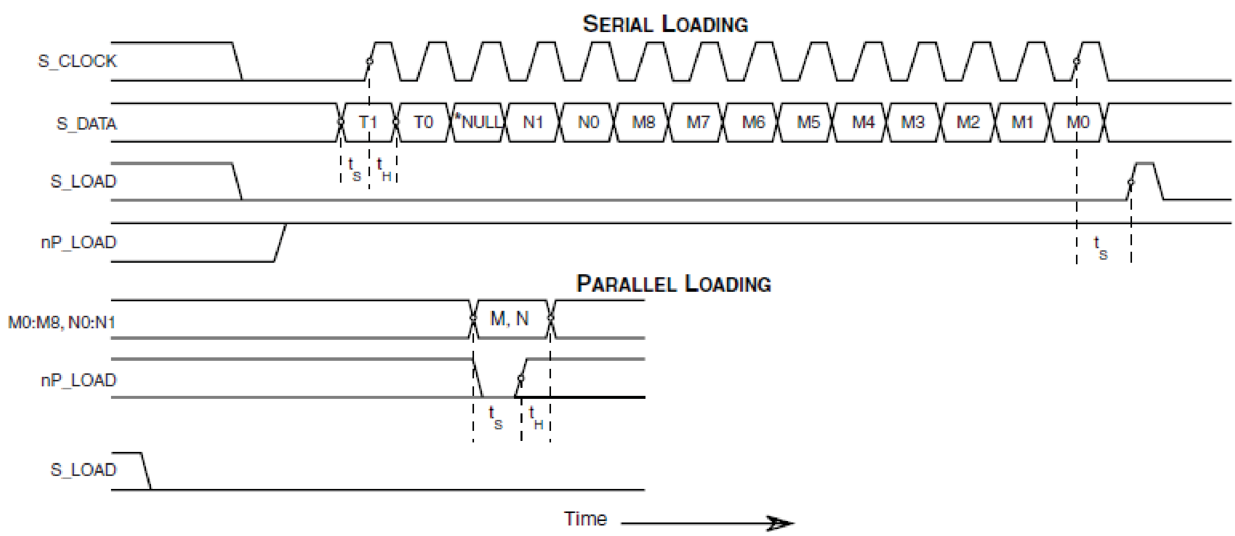


Figure 1. Parallel & Serial Load Operations

*NOTE: The NULL timing slot must be observed.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	M5	Input	Pullup	M divider inputs. Data latched on LOW-to-HIGH transistion of nP_LOAD input. LVCMOS / LVTTL interface levels.
2, 3, 4 28, 29 30, 31, 32	M6, M7, M8, M0, M1, M2, M3, M4	Input	Pulldown	
5, 6	N0, N1	Input	Pulldown	Determines output divider value as defined in Table 3C, Function Table. LVCMOS / LVTTL interface levels.
7	nc	Unused		No connect.
8, 16	V_{EE}	Power		Negative supply pins.
9	TEST	Output		Test output which is ACTIVE in the serial mode of operation. Output driven LOW in parallel mode. LVCMOS / LVTTL interface levels.
10	V_{CC}	Power		Core supply pin.
11, 12	FOUT1, nFOUT1	Output		Differential output for the synthesizer. 3.3V LVPECL interface levels.
13	V_{CCO}	Power		Output supply pin.
14, 15	FOUT0, nFOUT0	Output		Differential output for the synthesizer. 3.3V LVPECL interface levels.
17	MR	Input	Pulldown	Active High Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs FOUTx to go low and the inverted outputs nFOUTx to go high. When logic LOW, the internal dividers and the outputs are enabled. Assertion of MR does not affect loaded M, N, and T values. LVCMOS / LVTTL interface levels.
18	S_CLOCK	Input	Pulldown	Clocks in serial data present at S_DATA input into the shift register on the rising edge of S_CLOCK. LVCMOS / LVTTL interface levels.
19	S_DATA	Input	Pulldown	Shift register serial input. Data sampled on the rising edge of S_CLOCK. LVCMOS / LVTTL interface levels.
20	S_LOAD	Input	Pulldown	Controls transition of data from shift register into the dividers. LVCMOS / LVTTL interface levels.
21	V_{CCA}	Power		Analog supply pin.
22	CLK_SEL	Input	Pullup	Clock select input. Selects between differential clock input or TEST_CLK input as the PLL reference source. When HIGH, selects CLK, nCLK inputs. When LOW, selects TEST_CLK input. LVCMOS / LVTTL interface levels.
23	TEST_CLK	Input	Pulldown	Test clock input. LVCMOS / LVTTL interface levels.
24	CLK	Input	Pulldown	Non-inverting differential clock input.
25	nCLK	Input	Pullup	Inverting differential clock input.
26	nP_LOAD	Input	Pulldown	Parallel load input. Determines when data present at M8:M0 is loaded into M divider, and when data present at N1:N0 sets the N output divider value. LVCMOS / LVTTL interface levels.
27	VCO_SEL	Input	Pullup	Determines whether synthesizer is in PLL or bypass mode. LVCMOS / LVTTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characterisitics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

TABLE 3A. PARALLEL AND SERIAL MODE FUNCTION TABLE

Inputs							Conditions
MR	nP_LOAD	M	N	S_LOAD	S_CLOCK	S_DATA	
H	X	X	X	X	X	X	Reset. Forces outputs LOW.
L	L	Data	Data	X	X	X	Data on M and N inputs passed directly to the M divider and N output divider. TEST output forced LOW.
L	↑	Data	Data	L	X	X	Data is latched into input registers and remains loaded until next LOW transition or until a serial event occurs.
L	H	X	X	L	↑	Data	Serial input mode. Shift register is loaded with data on S_DATA on each rising edge of S_CLOCK.
L	H	X	X	↑	L	Data	Contents of the shift register are passed to the M divider and N output divider.
L	H	X	X	↓	L	Data	M divider and N output divider values are latched.
L	H	X	X	L	X	X	Parallel or serial inputs do not affect shift registers.
L	H	X	X	H		Data	S_DATA passed directly to M divider as it is clocked.

NOTE: L = LOW
H = HIGH
X = Don't care
↑ = Rising edge transition
↓ = Falling edge transition

TABLE 3B. PROGRAMMABLE VCO FREQUENCY FUNCTION TABLE

VCO Frequency (MHz)	M Divide	256	128	64	32	16	8	4	2	1
		M8	M7	M6	M5	M4	M3	M2	M1	M0
200	8	0	0	0	0	0	1	0	0	0
225	9	0	0	0	0	0	1	0	0	1
250	10	0	0	0	0	0	1	0	1	0
275	11	0	0	0	0	0	1	0	1	1
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
650	26	0	0	0	0	1	1	0	1	0
675	27	0	0	0	0	1	1	0	1	1
700	28	0	0	0	0	1	1	1	0	0

NOTE 1: These M divide values and the resulting frequencies correspond to differential input or TEST_CLK input frequency of 25MHz.

TABLE 3C. PROGRAMMABLE OUTPUT DIVIDER FUNCTION TABLE

Inputs		N Divider Value	Output Frequency (MHz)	
N1	N0		Minimum	Maximum
0	0	1	250	700
0	1	2	125	350
1	0	4	62.5	175
1	1	8	31.25	87.5

Absolute Maximum Ratings

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5 V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	47.9°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{CC} = V_{CCA} = V_{CCO}$ = 3.3V±5%, TA = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{CCO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				120	mA
I_{CCA}	Analog Supply Current				15	mA

Table 4B. LVCMOS / LVTTL DC Characteristics, $V_{CC} = V_{CCA} = V_{CCO}$ = 3.3V±5%, TA = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	VCO_SEL, CLK_SEL, MR, S_LOAD, S_DATA, S_CLOCK, nP_LOAD, M0:M8, N0:N1		2		V_{CC} + 0.3	V
		TEST_CLK		2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	VCO_SEL, CLK_SEL, MR, S_LOAD, S_DATA, S_CLOCK, nP_LOAD, M0:M8, N0:N1		-0.3		0.8	V
		TEST_CLK		-0.3		1.3	V
I_{IH}	Input High Current	M0-M4, M6-M8, N0, N1, MR, S_CLOCK, TEST_CLK, S_DATA, S_LOAD, nP_LOAD	$V_{CC} = V_{IN}$ = 3.465V			150	µA
		M5, CLK_SEL, VCO_SEL	$V_{CC} = V_{IN}$ = 3.465V			5	µA
I_{IL}	Input Low Current	M0-M4, M6-M8, N0, N1, MR, S_CLOCK, TEST_CLK, S_DATA, S_LOAD, nP_LOAD	V_{CC} = 3.465V, V_{IN} = 0V	-5			µA
		M5, CLK_SEL, VCO_SEL	V_{CC} = 3.465V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage	TEST	V_{CC} = 3.135V, I_{OH} = -36mA	2.6			V
V_{OL}	Output Low Voltage	TEST	V_{CC} = 3.135V, I_{OL} = 36mA			0.5	V

TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO}$ = 3.3V±5%, TA = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK	$V_{CC} = V_{IN}$ = 3.465V			150	µA
		nCLK	$V_{CC} = V_{IN}$ = 3.465V			5	µA
I_{IL}	Input Low Current	CLK	V_{CC} = 3.465V, V_{IN} = 0V	-5			µA
		nCLK	V_{CC} = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage			V_{EE} + 0.5		V_{CC} - 0.85	V

NOTE 1: For single ended applications, the maximum input voltage for CLK, nCLK is V_{CC} + 0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

TABLE 4D. LVPECL DC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO}$ = 3.3V±5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CCO} - 1.4		V_{CCO} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CCO} - 2.0		V_{CCO} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50 Ω to V_{CCO} - 2V.

TABLE 5. INPUT FREQUENCY CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO}$ = 3.3V±5%, TA = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Input Frequency	TEST_CLK; NOTE 1		10		25	MHz
		CLK, nCLK; NOTE 1		10		25	MHz
		S_CLOCK				25	MHz

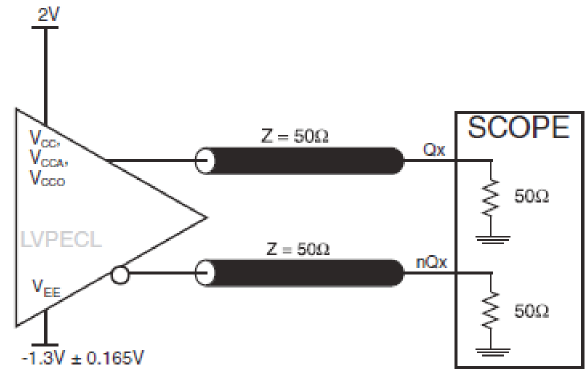
NOTE 1: For the differential input and TEST_CLK frequency range, the M value must be set for the VCO to operate within the 250MHz to 700MHz range. Using the minimum input frequency of 10MHz, valid values of M are 25 ≤ M ≤ 70.
Using the maximum frequency of 25MHz, valid values of M are 10 ≤ M ≤ 28.

TABLE 6. AC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO}$ = 3.3V±5%, TA = -40°C TO 85°C

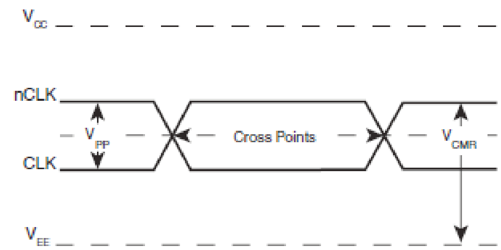
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
F_{OUT}	Output Frequency			31.25		700	MHz
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 1		fVCO > 350MHz			25	ps
*t*jit(per)	Period Jitter, RMS		fOUT > 100MHz			5	ps
*t*sk(o)	Output Skew; NOTE 1, 2					15	ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	200		700	ps
t_S	Setup Time	M, N to nP_LOAD		5			ns
		S_DATA to S_CLOCK		5			ns
		S_CLOCK to S_LOAD		5			ns
t_H	Hold Time	M, N to nP_LOAD		5			ns
		S_DATA to S_CLOCK		5			ns
		S_CLOCK to S_LOAD		5			ns
odc	Output Duty Cycle		N > 1	47		53	%
t_{PW}	Output Pulse Width		N = 1	t_{PERIOD}/2 - 150		t_{PERIOD}/2 + 150	ps
t_{LOCK}	PLL Lock Time					1	ms

See Parameter Measurement Information section.
NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured at the output differential cross points.

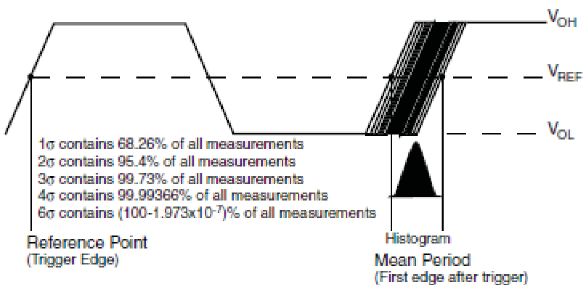
Parameter Measurement Information



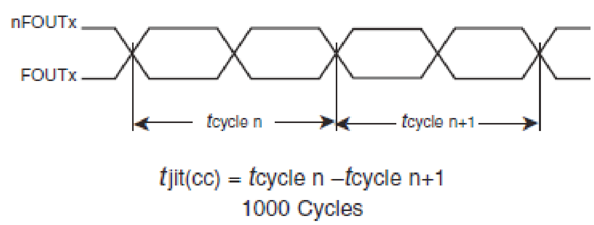
3.3V Output Load AC Test Circuit



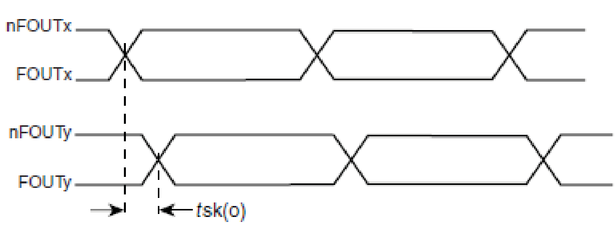
Differential Input Level



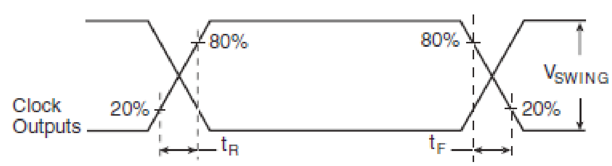
Period Jitter



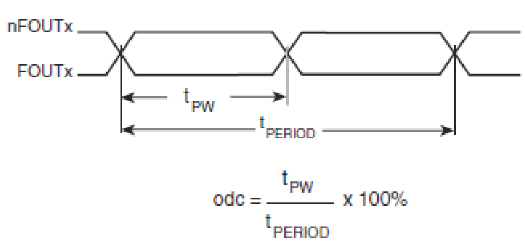
Cycle-to-Cycle Jitter



Output Skew



Output Rise/Fall Time



Output Duty Cycle/Pulse Width/Period

Application Information

Storage Area Networks

A variety of technologies are used for interconnection of the elements within a SAN. The tables below list the common application frequencies as well as the 8432I-101 configurations used to generate the appropriate frequency.

Table 7. Common SANs Application Frequencies

Interconnect Technology	Clock Rate	Reference Frequency to SERDES (MHz)	Crystal Frequency (MHz)
Gigabit Ethernet	1.25 GHz	125, 250, 156.25	25, 19.53125
Fibre Channel	FC1 1.0625 GHz FC2 2.1250 GHz	106.25, 53.125, 132.8125	16.6015625, 25
Infiniband	2.5 GHz	125, 250	25

Table 8. Configuration Details for SANs Applications

Interconnect Technology	CLK, nCLK Input (MHz)	8432I-101 Output Frequency to SERDES (MHz)	8432I-101 M & N Settings										
			M8	M7	M6	M5	M4	M3	M2	M1	M0	N1	N0
Gigabit Ethernet	25	125	0	0	0	0	1	0	1	0	0	1	0
	25	250	0	0	0	0	1	0	1	0	0	0	1
	25	156.25	0	0	0	0	1	1	0	0	1	1	0
	19.53125	156.25	0	0	0	1	0	0	0	0	0	1	0
Fiber Channel 1	25	53.125	0	0	0	0	1	0	0	0	1	1	1
	25	106.25	0	0	0	0	1	0	0	0	1	1	0
Fiber Channel 2	16.6015625	132.8125	0	0	0	1	0	0	0	0	0	1	0
Infiniband	25	125	0	0	0	0	1	0	1	0	0	1	0
	25	250	0	0	0	0	1	0	1	0	0	0	1

Power Supply Filtering Techniques

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The 8432I-101 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC}, V_{CCA}, and V_{CCO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 2* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{CCA} pin.

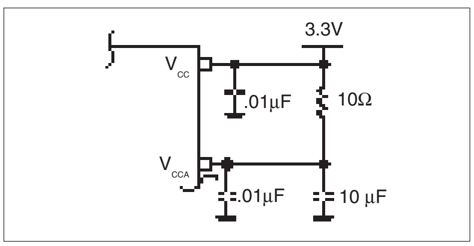


Figure 2. Power Supply Filtering

Wiring the Differential Input to Accept Single Ended Levels

Figure 3 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = $V_{CC}/2$ is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{CC} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

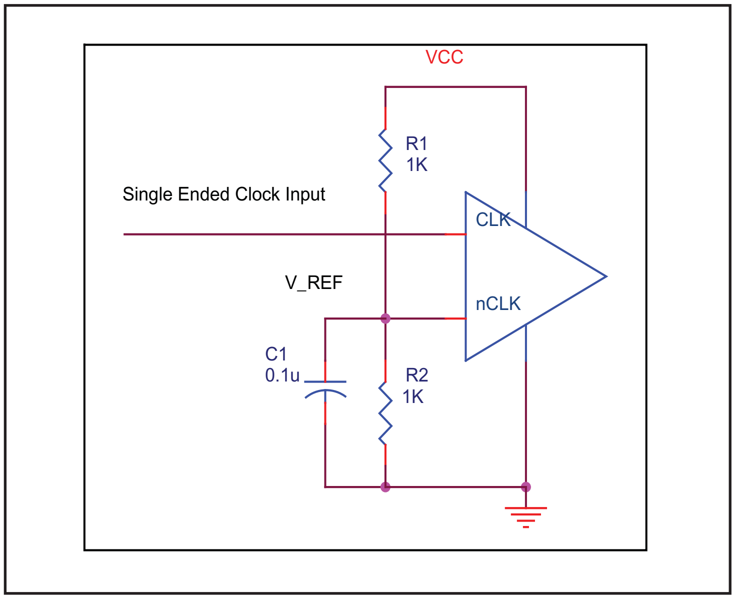


Figure 3. Single Ended Signal Driving Differential Input

Recommendations for Unused Input and Output Pins

Inputs:

TEST_CLK Input:
For applications not requiring the use of the test clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the TEST_CLK to ground.

CLK/nCLK Input:
For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

LVCMOS Control Pins:
All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Output:
All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 4A to 4E show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 4A,* the input termination applies for IDT HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

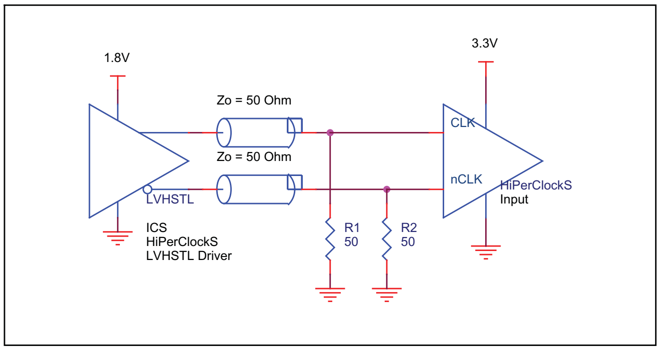


Figure 4A. HiPerClockS CLK/nCLK Input Driven by IDT HiPerClockS LVHSTL Driver

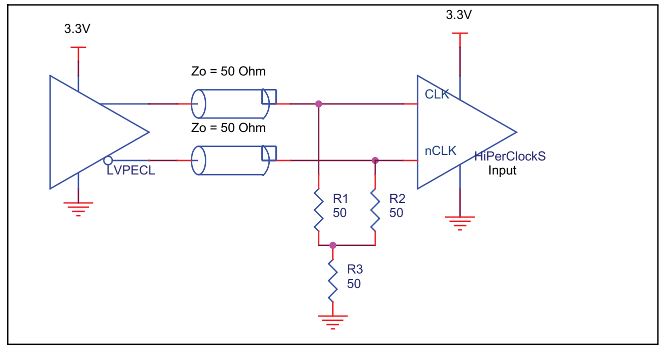


Figure 4B. HiPerClockS CLK/nCLK Input Driven by 3.3V LVPECL Driver

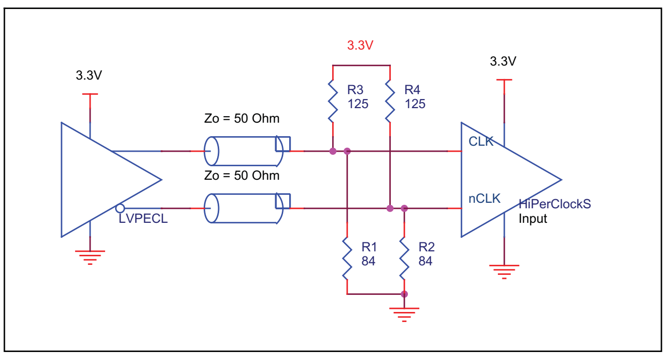


Figure 4C. HiPerClockS CLK/nCLK Input Driven by 3.3V LVPECL Driver

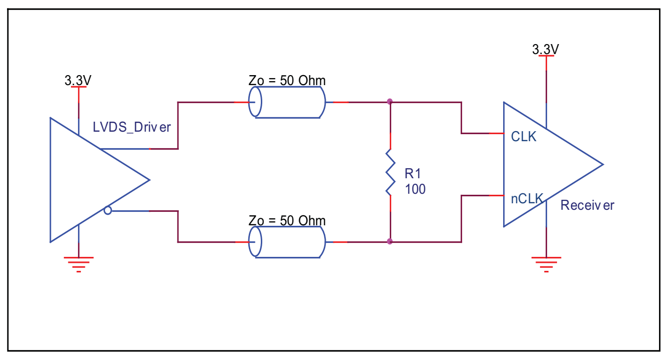


Figure 4D. HiPerClockS CLK/nCLK Input Driven by 3.3V LVDS Driver

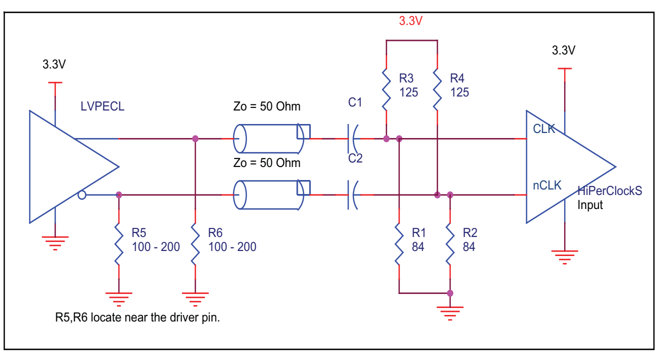


Figure 4E. HiPerClockS CLK/nCLK Input Driven by 3.3V LVPECL Driver with AC Couple

Termination for LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 5A and 5B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

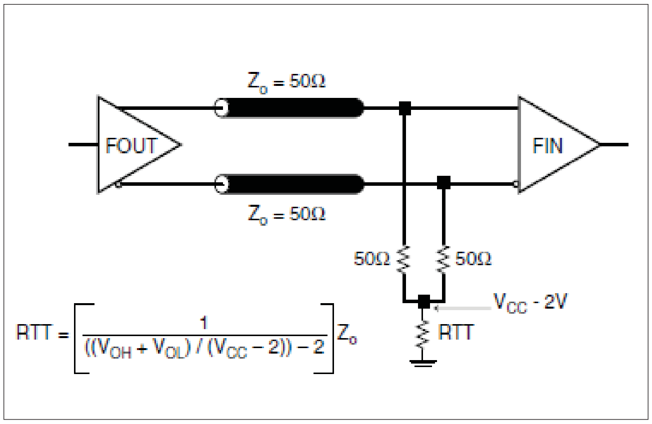


Figure 5A. LVPECL Output Termination

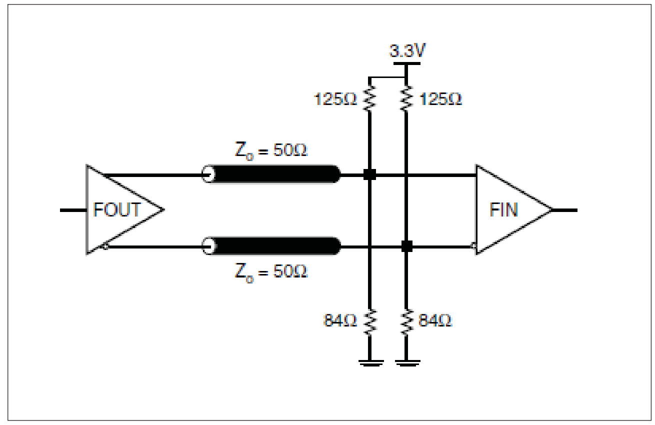


Figure 5B. LVPECL Output Termination

Layout Guideline

The schematic of the 8432I-101 layout example used in this layout guideline is shown in *Figure 6A.* The 8432I-101 recommended PCB board layout for this example is shown in *Figure 6B*. This layout example is used as a general guideline. The layout in the actual system will depend on the selected component types, the density of the components, the density of the traces, and the stack up of the P.C. board.

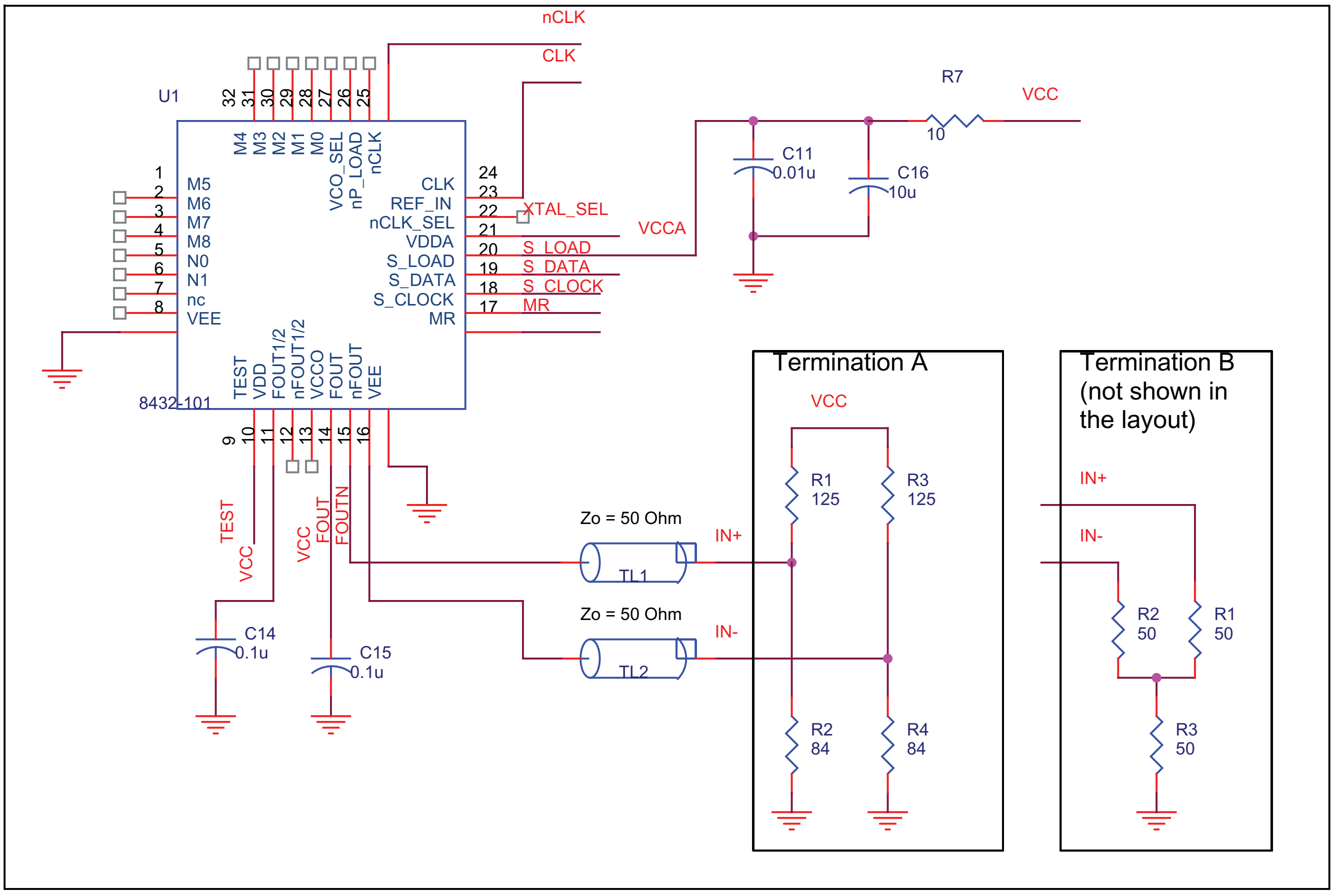


Figure 6A. Schematic of Recommended Layout

The following component footprints are used in this layout example: All the resistors and capacitors are size 0603.

Power and Grounding

Place the decoupling capacitors C14 and C15 as close as possible to the power pins. If space allows, placing the decoupling capacitor at the component side is preferred. This can reduce unwanted inductance between the decoupling capacitor and the power pin generated by the via.

Maximize the pad size of the power (ground) at the decoupling capacitor. Maximize the number of vias between power (ground) and the pads. This can reduce the inductance between the power (ground) plane and the component power (ground) pins.

If V_{CCA} shares the same power supply with V_{CC}, insert the RC filter R7, C11, and C16 in between. Place this RC filter as close to the V_{CCA} as possible.

Clock Traces and Termination

The component placements, locations and orientations should be arranged to achieve the best clock signal quality. Poor clock signal quality can degrade the system performance or cause system failure. In the synchronous high-speed digital system, the clock signal is less tolerable to poor signal quality than other signals. Any ringing on the rising or falling edge or excessive ring back can cause system failure. The trace shape and the trace delay might be restricted by the available space on the board and the component location. While routing the traces, the clock signal traces should be routed first and should be locked prior to routing other signal traces.

- The traces with 50Ω transmission lines TL1 and TL2 at FOUT and nFOUT should have equal delay and run adjacent to each other. Avoid sharp angles on the clock trace. Sharp angle turns cause the characteristic impedance to change on the transmission lines.
- Keep the clock trace on same layer. Whenever possible, avoid any vias on the clock traces. Any via on the trace can affect the trace characteristic impedance and hence degrade signal quality.
- To prevent cross talk, avoid routing other signal traces in parallel with the clock traces. If running parallel traces is unavoidable, allow more space between the clock trace and the other signal trace.
- Make sure no other signal trace is routed between the clock trace pair.

The matching termination resistors R1, R2, R3 and R4 should be located as close to the receiver input pins as possible. Other termination schemes can also be used but are not shown in this example.

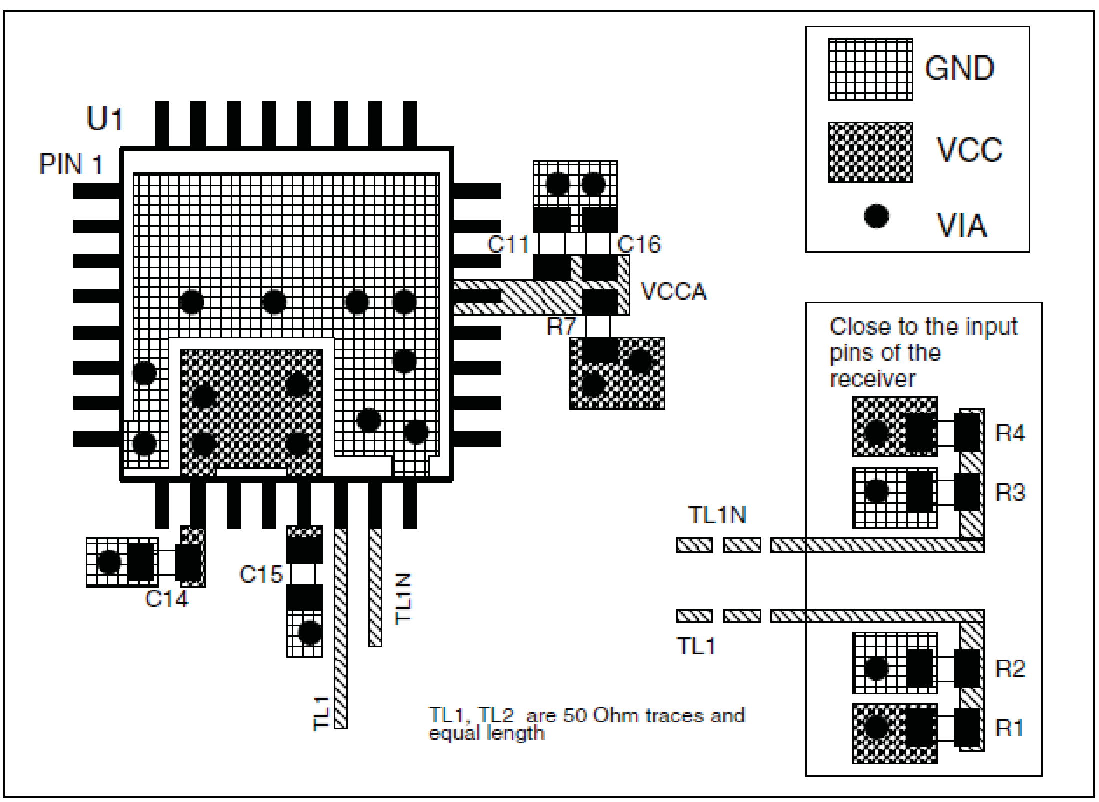


Figure 6B. PCB Board Layout for 8432I-101

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the 8432I-101.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the 8432I-101 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 120mA = **416mW**
Power (outputs)$_{MAX}$ = **30mW/Loaded Output pair**
If all outputs are loaded, the total power is 2 * 30mW = **60mW**

Total Power $_{\_MAX}$ (3.465V, with all outputs switching) = 416mW + 60mW = **476mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)
T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 42.1°C/W per Table 9 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 0.476W * 42.1°C/W = 105°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 9. THERMAL RESISTANCE θ_{JA} FOR 32-PIN LQFP, FORCED CONVECTION

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 7.*

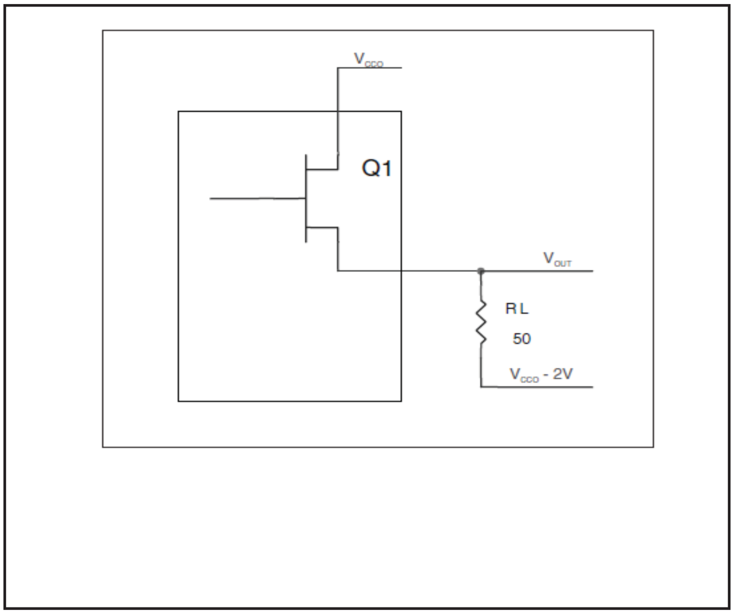


FIGURE 7. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CCO\_MAX} - 0.9V}$

  $(V_{CCO\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CCO\_MAX} - 1.7V}$

  $(V_{CCO\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) =$
[(2V - 0.9V)/50Ω] * 0.9V = 19.8mW

$Pd\_L = [(V_{OL\_MAX} – (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) =$
[(2V - 1.7V)/50Ω] * 1.7V = 10.2mW

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

RELIABILITY INFORMATION

TABLE 10. θ_{JA} VS. AIR FLOW TABLE FOR 32 LEAD LQFP

θ_{JA} by Velocity (Linear Feet per Minute)

	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for 8432I-101 is: 3712

Package Outline - Y Suffix for 32 Lead LQFP

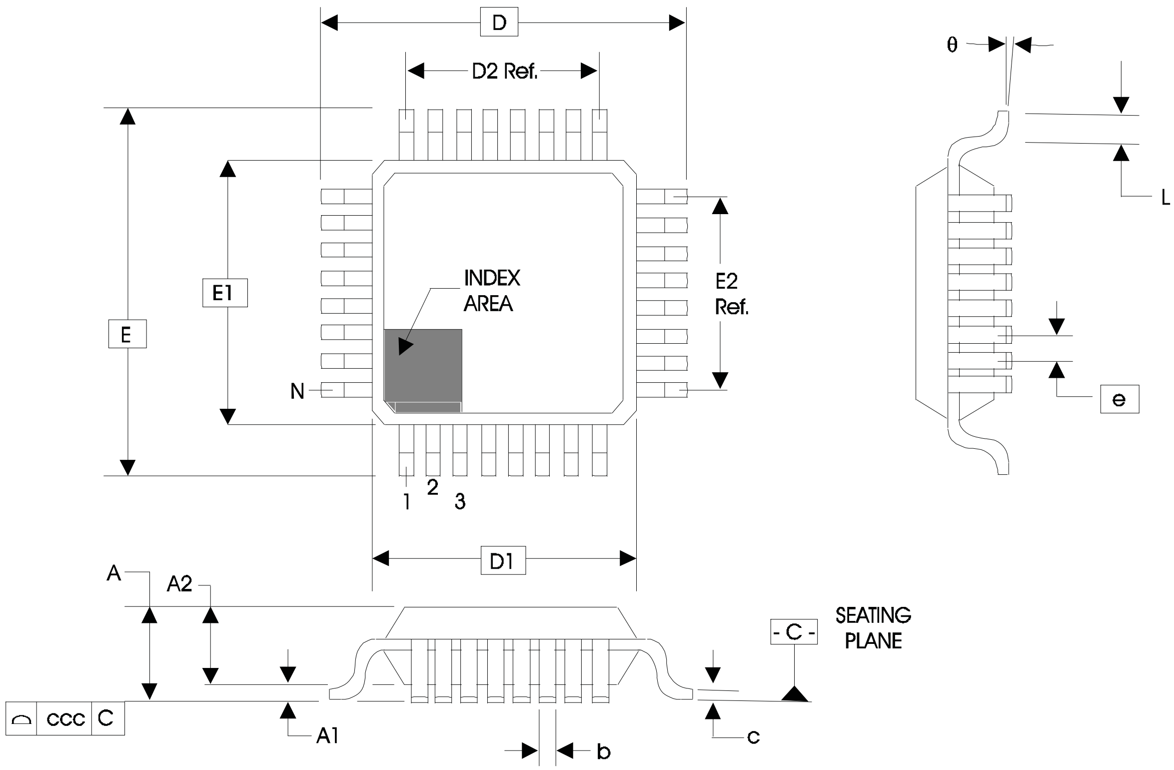


Table 11. Package Dimensions

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBA		
	MINIMUM	NOMINAL	MAXIMUM
N		32	
A			1.60
A1	0.05		0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09		0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.60	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.60	
e		0.80 BASIC	
L	0.45	0.60	0.75
θ	0°		7°
ccc			0.10

Reference Document: JEDEC Publication 95, MS-026

TABLE 12. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8432DYI-101LF	ICS432DI101L	32 Lead “Lead-Free” LQFP	250	-40°C to 85°C
8432DYI-101LFT	ICS432DI101L	32 Lead “Lead-Free” LQFP	tape & reel	-40°C to 85°C

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
A	 T12	1 17	Features Section - added Lead-Free bullet. Ordering Information Table - add Lead-Free parts.	5/23/05
B	T5	6 9	Input Frequency Characteristics Table - changed $_{fIN}$ (TEST_CLK and CLK, nCLK) from 14MHz min. to 10MHz min. *Added Recommendations for Unused Input and Output Pins.*	10/26/06
C	T4D	6 14 - 15	LVPECL DC Characteristics Table -corrected V_{OH} max. from V_{CCO} - 1.0V to V_{CCO} - 0.9V. Power Considerations - corrected power dissipation to reflect V_{OH} max in Table 4D.	4/10/07
C	T12	18	Ordering Information - removed leaded devices. Updated data sheet information.	10/23/15
C	T12	18	Ordering Information - removed ICS from part/order number. Removed 1000 from tape and reel and removed LF note from below the table. Updated headers and footers.	1/8/16

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