FemtoClock® Crystal-to-LVDS Frequency Synthesizer

General Description

The ICS844004I-01 is a 4 output LVDS Synthesizer optimized to generate Ethernet reference clock frequencies. Using a 25MHz 18pF parallel resonant crystal, the following frequencies can be generated based on the 2 frequency select pins (F_SEL[1:0]): 156.25MHz, 125MHz and 62.5MHz. The ICS844004I-01 uses IDT's 3rd generation low phase noise VCO technology and can achieve <1ps typical rms phase jitter, easily meeting Ethernet jitter requirements. The ICS844004I-01 is packaged in a small 24-pin TSSOP package.

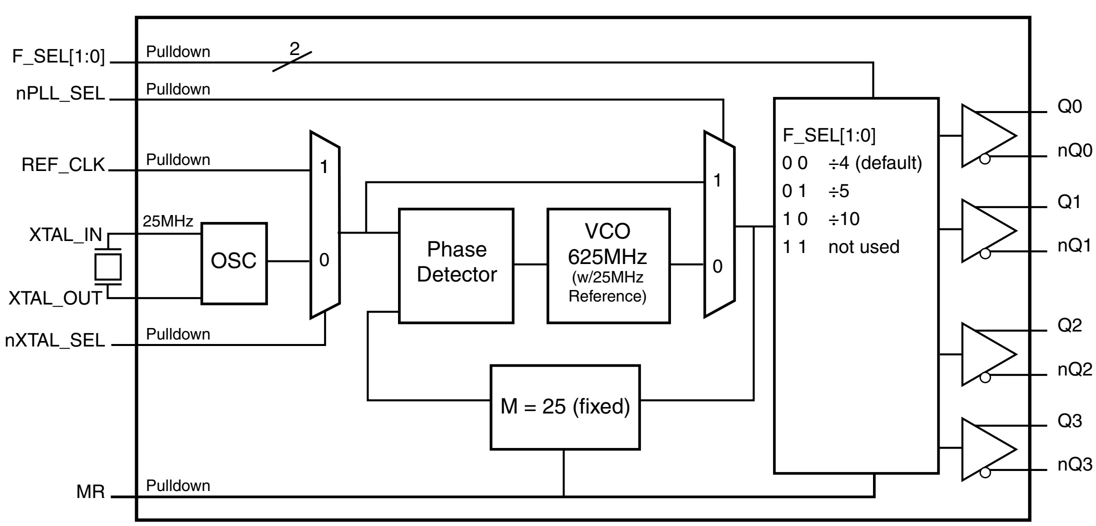
Features

- Four LVDS output pairs
- Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended input
- Supports the following output frequencies: 156.25MHz, 125MHz, 62.5MHz
- VCO range: 560MHz - 680MHz
- RMS phase jitter @ 156.25MHz, using a 25MHz crystal (1.875MHz - 20MHz): 0.41ps (typical)
- Full 3.3V or 2.5V supply modes
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages
- **Not Recommended For New Designs**

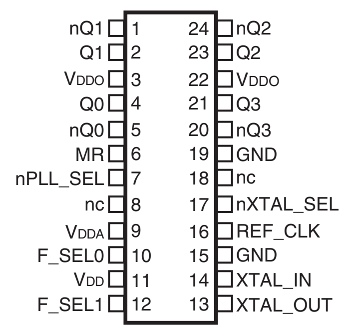
Frequency Select Function Table

Inputs					Output Frequency (MHz), (25MHz Ref.)
F_SEL1	F_SEL0	M Div. Value	N Div. Value	M/N Div. Value	
0	0	25	4	6.25	156.25 (default)
0	1	25	5	5	125
1	0	25	10	2.5	62.5
1	1	25	not used		not used

Block Diagram



Pin Assignment



ICS844004I-01
24-Lead TSSOP
4.4mm x 7.8mm x 0.92mm package body
G Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	nQ1, Q1	Output		Differential output pair. LVDS interface levels.
3, 22	V_{DDO}	Power		Output supply pins.
4, 5	Q0, nQ0	Output		Differential output pair. LVDS interface levels.
6	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Qx to go low and the inverted outputs nQx to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
7	nPLL_SEL	Input	Pulldown	PLL select. Selects between the PLL and REF_CLK as input to the dividers. When LOW, selects PLL (PLL enabled). When HIGH, the PLL is bypassed. LVCMOS/LVTTL interface levels.
8, 18	nc	Unused		No connect.
9	V_{DDA}	Power		Analog supply pin.
10, 12	F_SEL0, F_SEL1	Input	Pulldown	Frequency select pins. LVCMOS/LVTTL interface levels.
11	V_{DD}	Power		Core supply pin.
13, 14	XTAL_OUT, XTAL_IN	Input		Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input.
15, 19	GND	Power		Power supply ground.
16	REF_CLK	Input	Pulldown	Single-ended reference clock input. LVCMOS/LVTTL interface levels.
17	nXTAL_SEL	Input	Pulldown	Selects between crystal or REF_CLK inputs as the PLL reference source. Selects XTAL inputs when LOW. Selects REF_CLK when HIGH. LVCMOS/LVTTL interface levels.
20, 21	nQ3, Q3	Output		Differential output pair. LVDS interface levels.
23, 24	Q2, nQ2	Output		Differential output pair. LVDS interface levels.

NOTE: *Pulldown* refers to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I XTAL_IN Other Inputs	 0V to V_{DD} -0.5V to V_{DD} + 0.5V
Outputs, I_O Continuous Current Surge Current	 10mA 15mA
Package Thermal Impedance, θ_{JA}	82.3°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 3A. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = -40°C$ to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.11	3.3	V_{DD}	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				64	mA
I_{DDA}	Analog Supply Current				11	mA
I_{DDO}	Output Supply Current				48	mA

Table 3B. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, $T_A = -40°C$ to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.11	2.5	V_{DD}	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Core Supply Current				62	mA
I_{DDA}	Analog Supply Current				11	mA
I_{DDO}	Output Supply Current				45	mA

Table 3C. LVCMOS/LVTTL DC Characteristics, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.3V	2		V_{DD} + 0.3	V
			V_{DD} = 2.5V	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.3V	-0.3		0.8	V
			V_{DD} = 2.5V	-0.3		0.7	V
I_{IH}	Input High Current	REF_CLK, MR, F_SEL[0:1], nPLL_SEL, nXTAL_SEL	V_{DD} = V_{IN} = 3.465V or 2.625V			150	µA
I_{IL}	Input Low Current	REF_CLK, MR, F_SEL[0:1], nPLL_SEL, nXTAL_SEL	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-5			µA

Table 3D. LVDS DC Characteristics, V_{DD} = V_{DDO} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		247		454	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.2		1.55	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

Table 3E. LVDS DC Characteristics, V_{DD} = V_{DDO} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		247		454	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.1		1.5	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

Table 4. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		22.4	25	27.2	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

NOTE: Characterized using an 18pF parallel resonant crystal.

AC Electrical Characteristics

Table 5A. AC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	F_SEL[1:0] = 00		156.25		MHz
		F_SEL[1:0] = 01		125		MHz
		F_SEL[1:0] = 10		62.5		MHz
*t*sk(o)	Output Skew; NOTE 1, 2				55	ps
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 3	156.25MHz, (1.875MHz – 20MHz)		0.41		ps
		125MHz, (1.875MHz – 20MHz)		0.45		ps
		62.5MHz, (1.875MHz – 20MHz)		0.45		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	350		920	ps
odc	Output Duty Cycle		48		52	%
t_{LOCK}	PLL Lock Time				100	ms

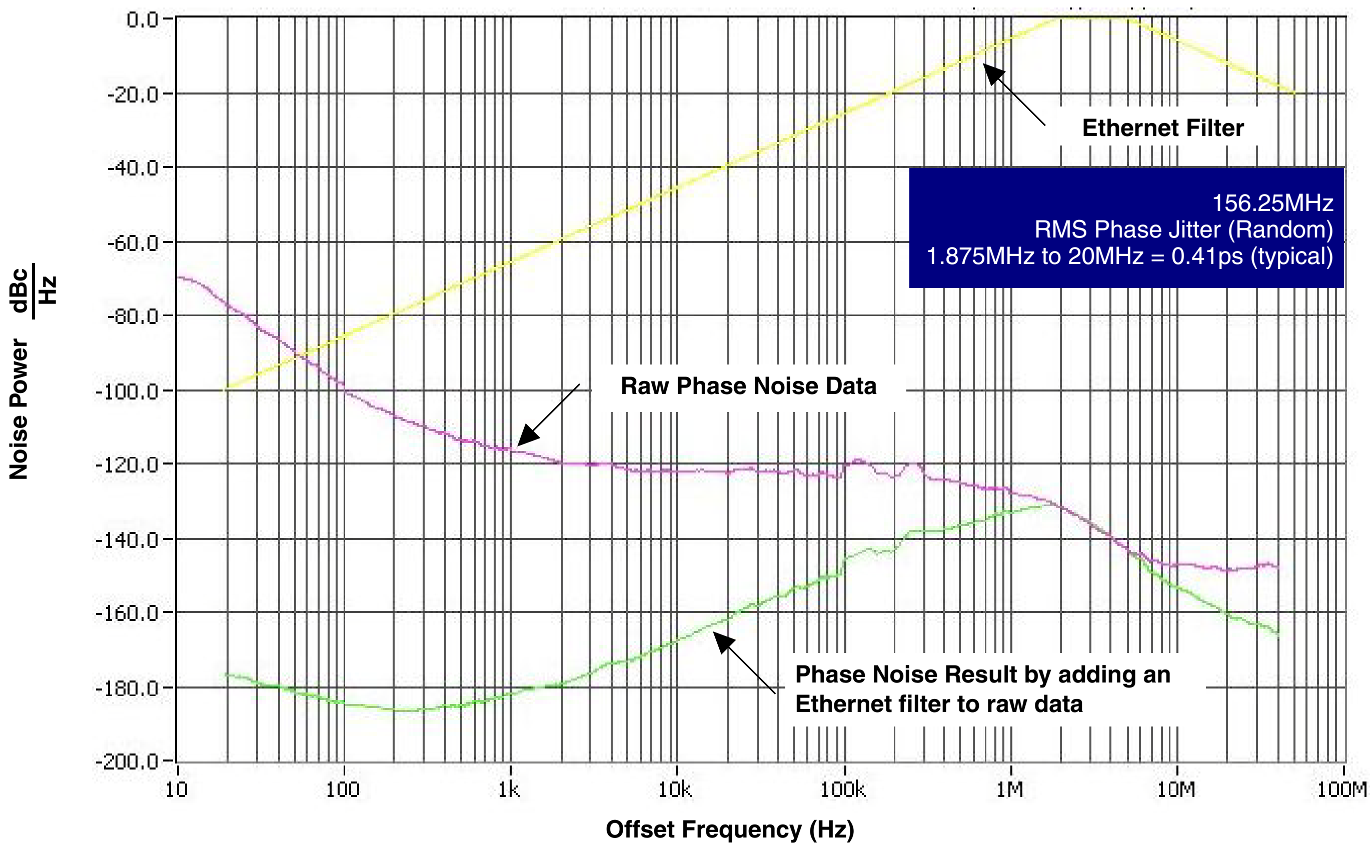
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: Using 25MHz crystal.
NOTE 1: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Please refer to the Phase Noise Plot.

Table 5B. AC Characteristics, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, T_A = -40°C to 85°C

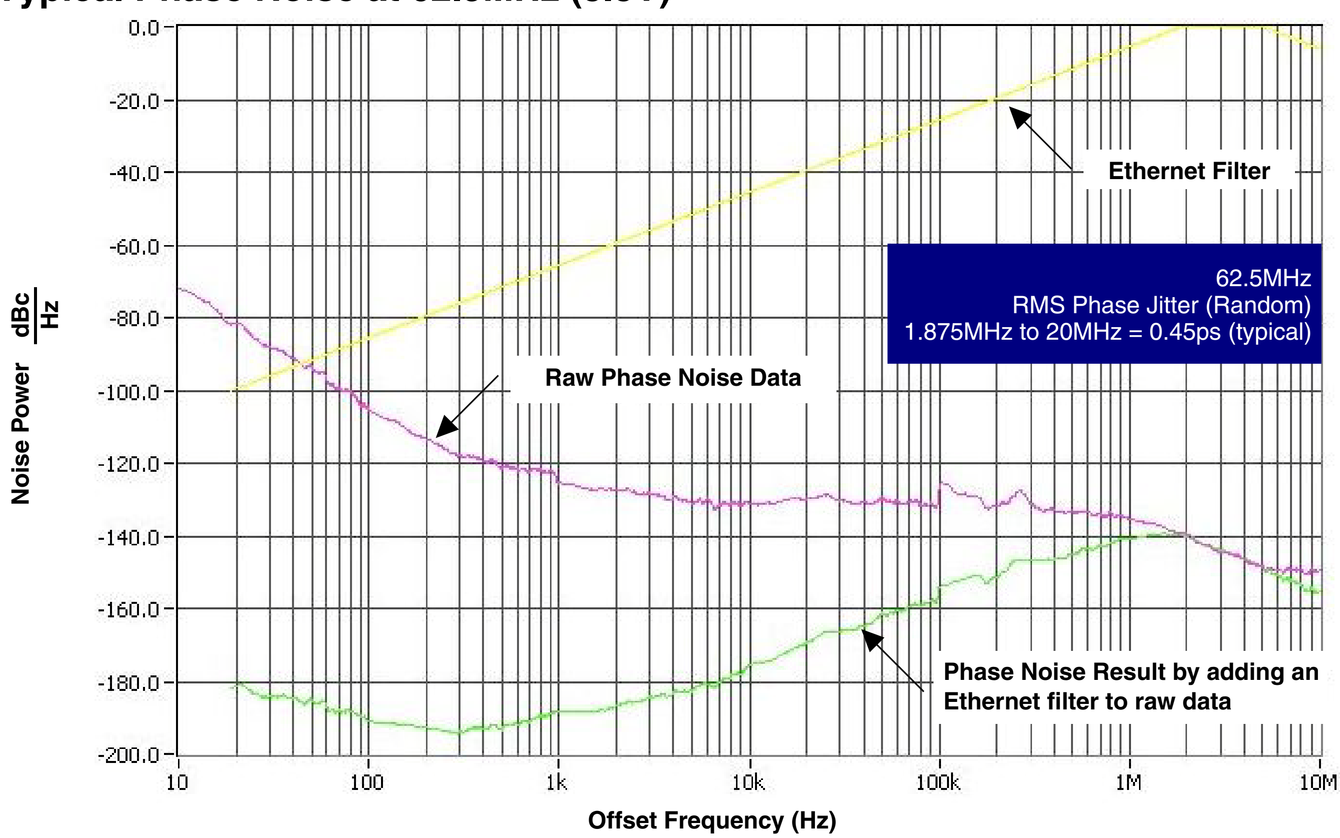
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	F_SEL[1:0] = 00		156.25		MHz
		F_SEL[1:0] = 01		125		MHz
		F_SEL[1:0] = 10		62.5		MHz
*t*sk(o)	Output Skew; NOTE 1, 2				55	ps
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 3	156.25MHz, (1.875MHz – 20MHz)		0.41		ps
		125MHz, (1.875MHz – 20MHz)		0.45		ps
		62.5MHz, (1.875MHz – 20MHz)		0.45		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	330		940	ps
odc	Output Duty Cycle		48		52	%
t_{LOCK}	PLL Lock Time				100	ms

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: Using 25MHz crystal.
NOTE 1: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Please refer to the Phase Noise Plot.

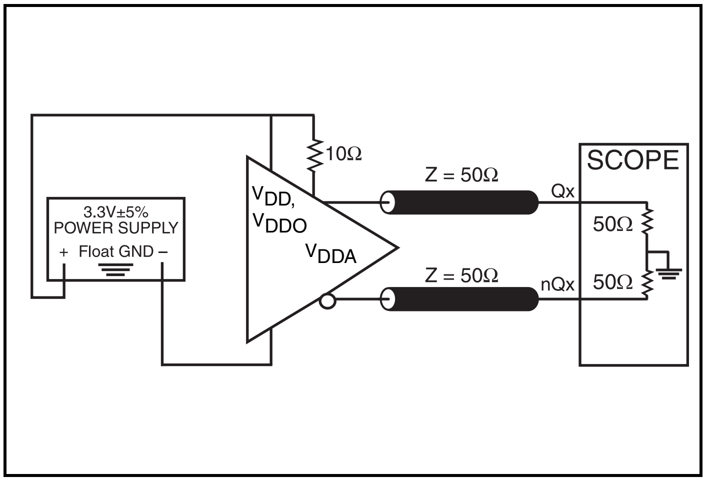
Typical Phase Noise at 156.25MHz (3.3V)



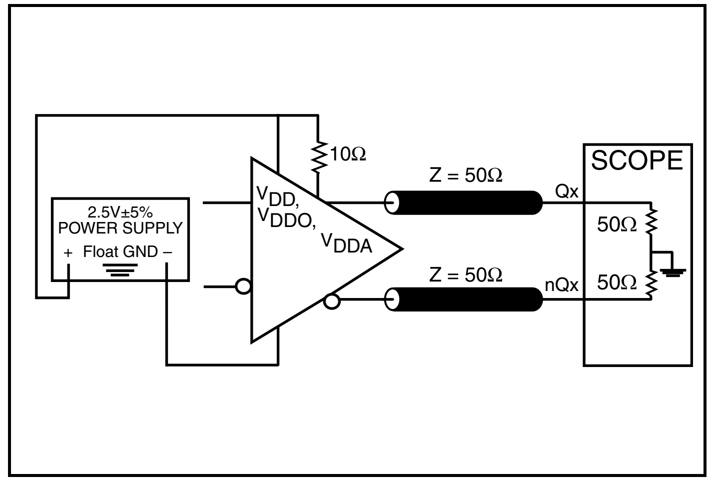
Typical Phase Noise at 62.5MHz (3.3V)



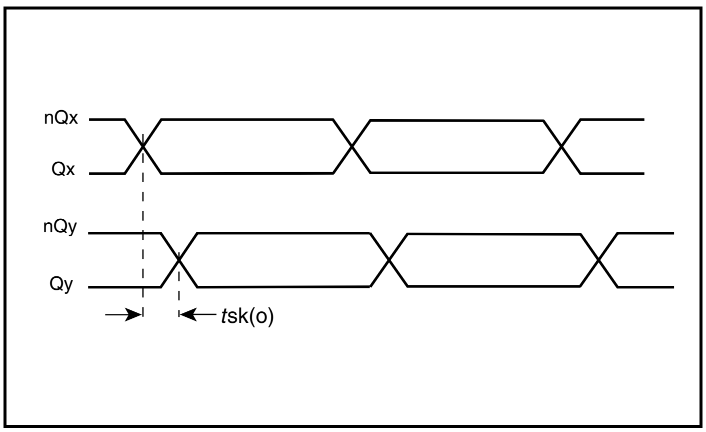
Parameter Measurement Information



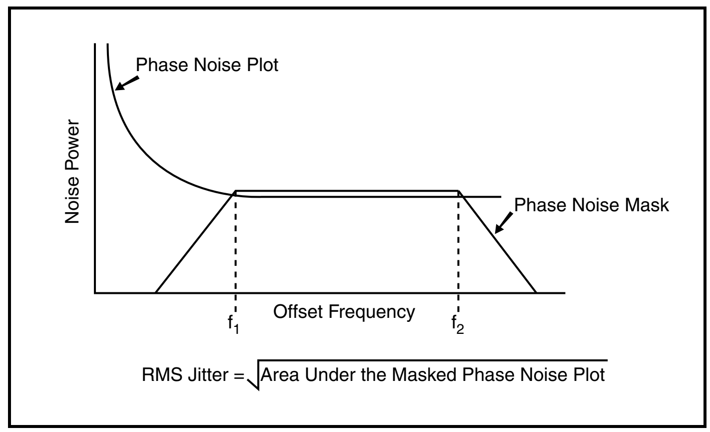
3.3V Output Load AC Test Circuit



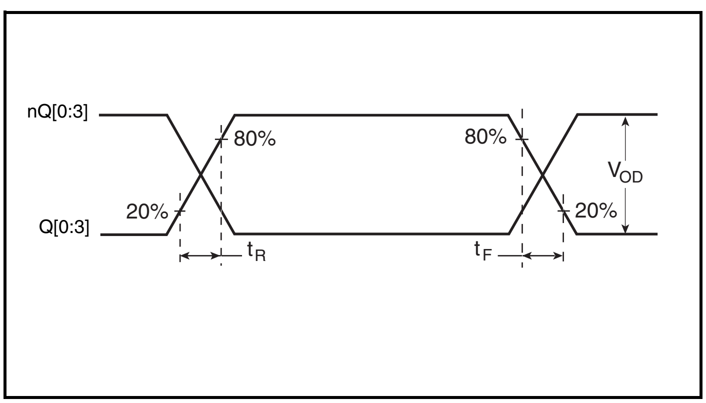
2.5V Output Load AC Test Circuit



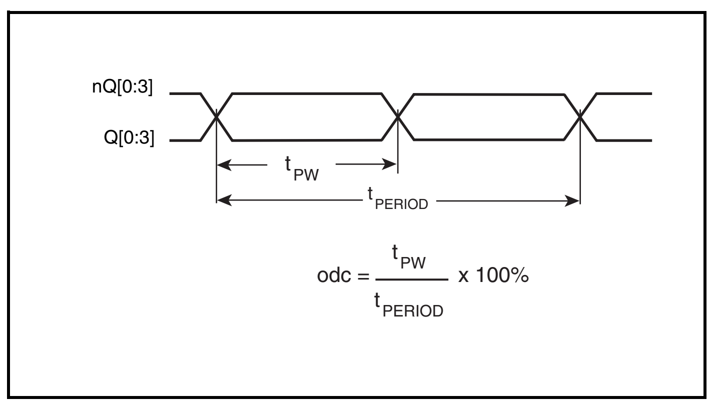
Output Skew



RMS Phase Jitter

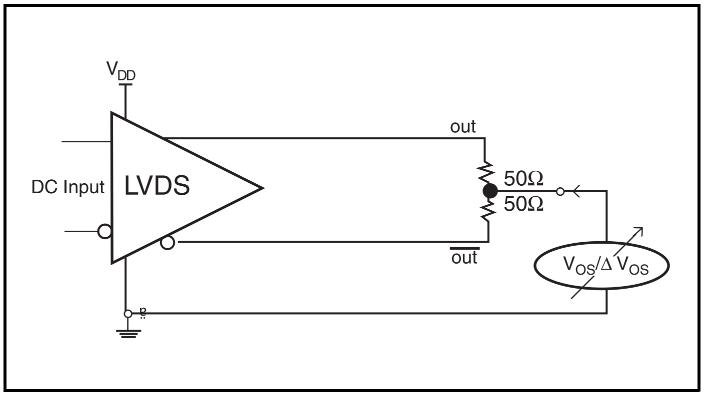


Output Rise/Fall Time

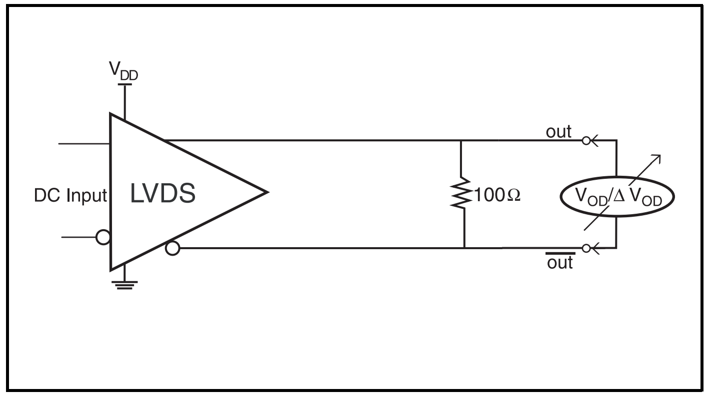


Output Duty Cycle/Pulse Width/Period

Parameter Measurement Information, continued



Offset Voltage Setup



Differential Output Voltage Setup

Application Information

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS844004I-01 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA} and V_{DDO} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{DDA} pin.

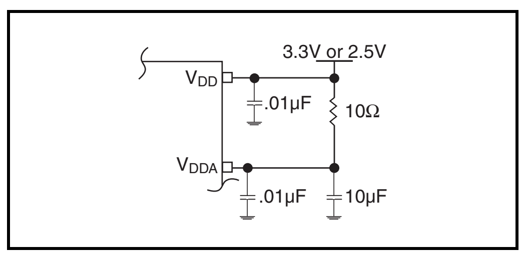


Figure 1. Power Supply Filtering

Crystal Input Interface

The ICS844004I-01 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.

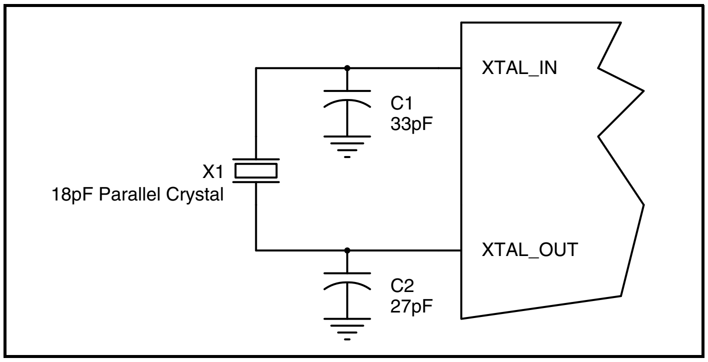


Figure 2. Crystal Input Interface

Overdriving the XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3A.* The XTAL_OUT pin can be left floating. The maximum amplitude of the input signal should not exceed 2V and the input edge rate can be as slow as 10ns. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.

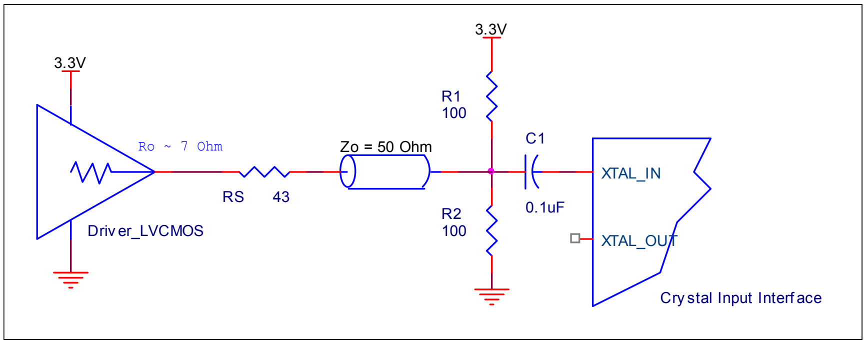


Figure 3A. General Diagram for LVCMOS Driver to XTAL Input Interface

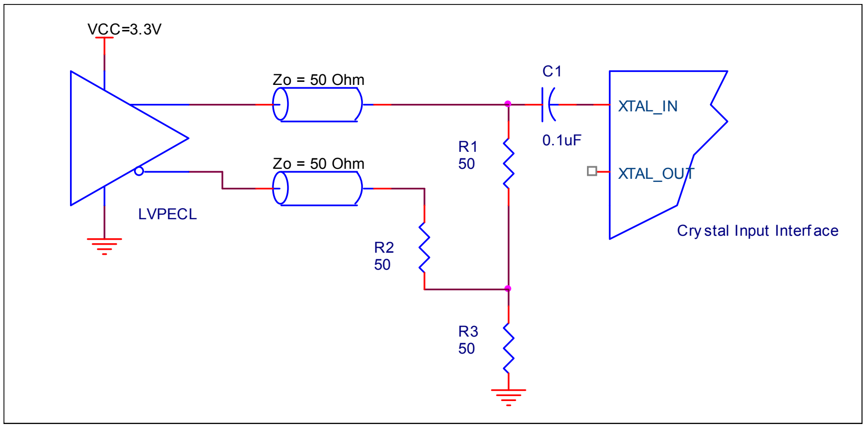


Figure 3B. General Diagram for LVPECL Driver to XTAL Input Interface

3.3V, 2.5V LVDS Driver Termination

A general LVDS interface is shown in *Figure 4.* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

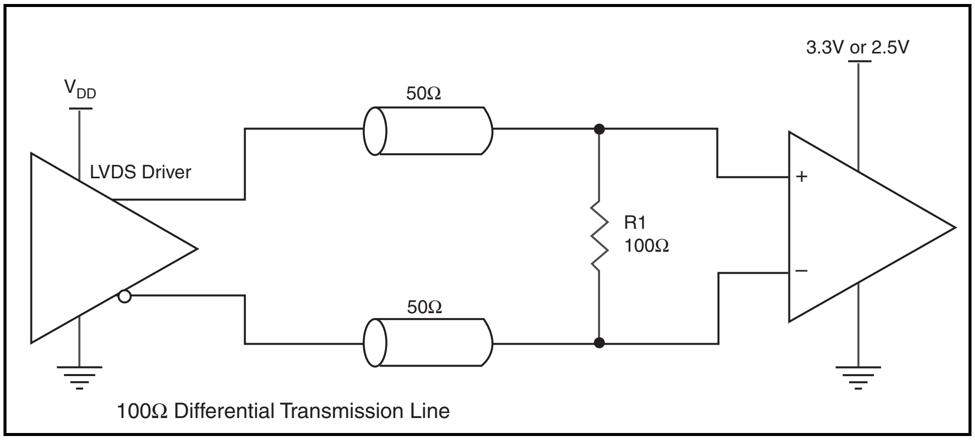


Figure 4. Typical LVDS Driver Termination

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

REF_CLK Input

For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the REF_CLK to ground.

Outputs:

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

Schematic Example

Figure 5 shows an example of ICS844004I-01 application schematic. In this example, t he device is operated at $V_{DD} = V_{DDO}$ = 3.3V. The 18pF parallel resonant 25MHz crystal is used. The C1= 33pF and C2 = 27pF are recommended for frequency accuracy. For different board layouts, the C1 and C2 may be slightly adjusted for optimizing frequency accuracy. Two examples of LVDS for receiver without built-in termination are shown in this schematic.

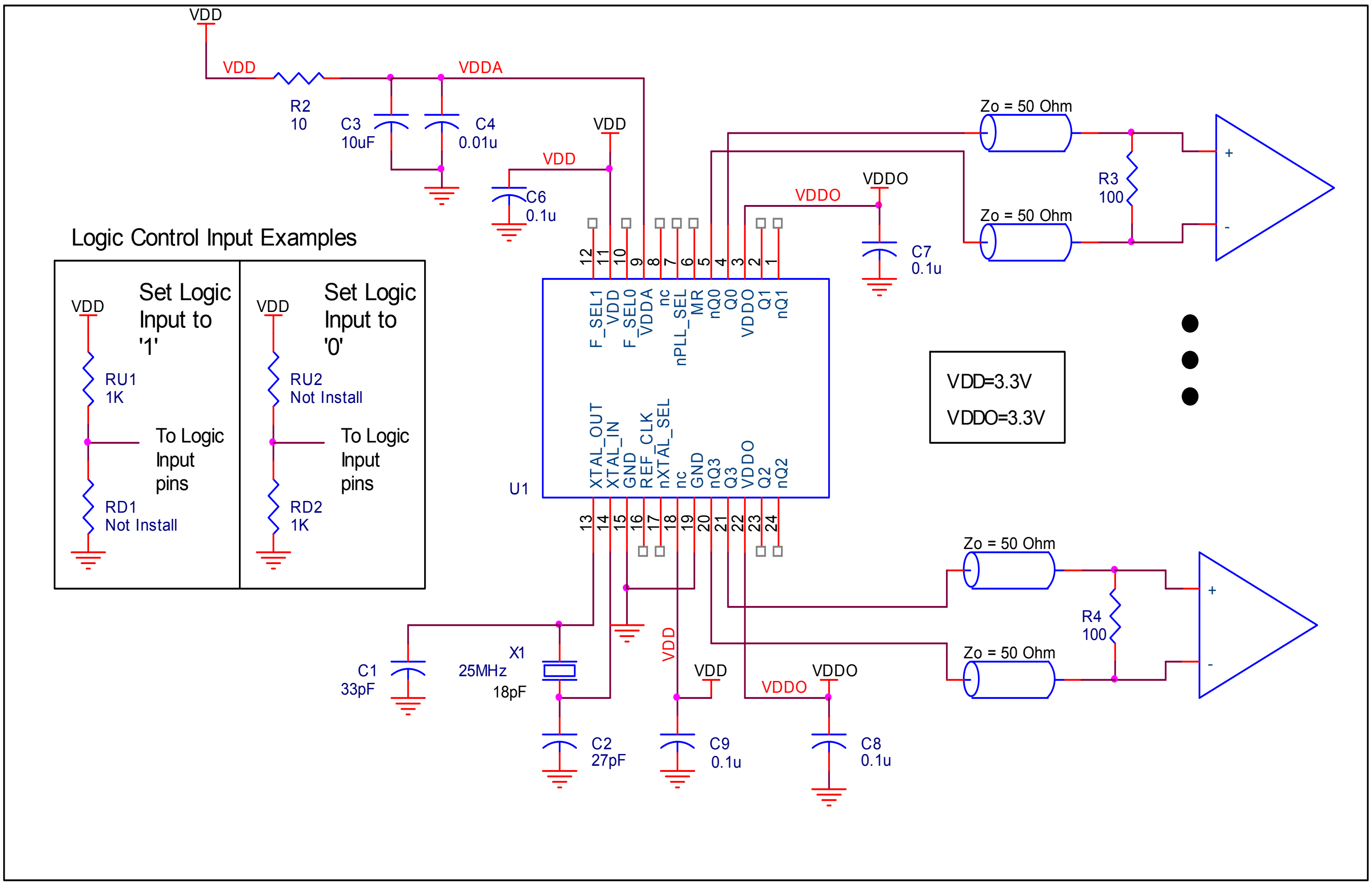


Figure 5. ICS844004I-01 Schematic Layout Example

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS844004I-01.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS844004I-01 is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

- Power $(core)_{MAX} = V_{DD\_MAX} * (I_{DD\_MAX} + I_{DDA\_MAX})$ = 3.465V * (64mA + 11mA) = **259.875mW**
- Power $(outputs)_{MAX} = V_{DDO\_MAX} * I_{DDO\_MAX}$ = 3.465V * 48mA = **166.32mW**

Total Power$_{\_MAX}$ = 259.875mW + 166.32mW = **426.195mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 82.3°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.426W * 82.3°C/W = 120.1°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 24 Lead TSSOP, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	82.3°C/W	78.0°C/W	75.9°C/W

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 24 Lead TSSOP

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	82.3°C/W	78.0°C/W	75.9°C/W

Transistor Count

The transistor count for ICS844004I-01 is: 2832

Package Outline and Package Dimensions

Package Outline - G Suffix for 24 Lead TSSOP

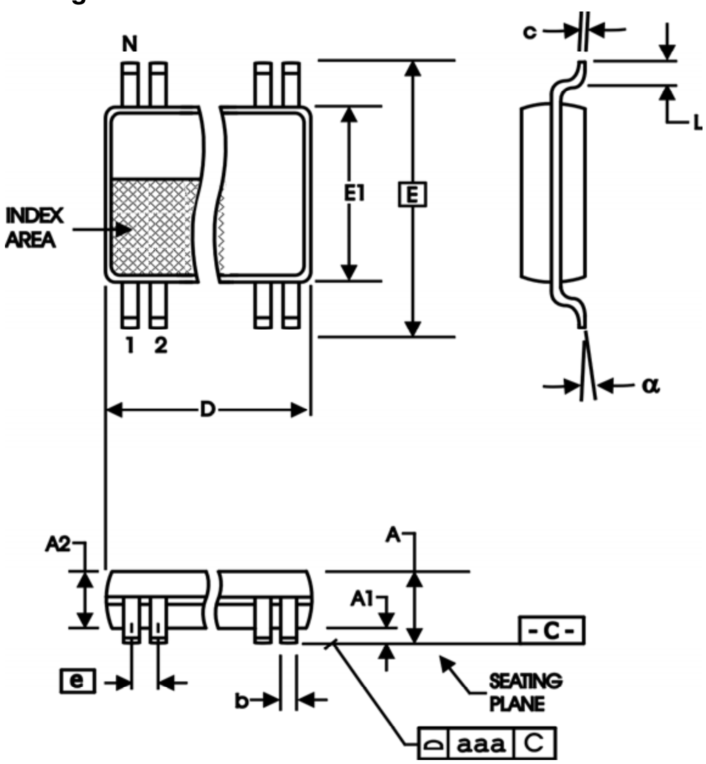


Table 8. Package Dimensions

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	24	
A		1.20
A1	0.5	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
844004BGI-01	ICS844004BI01	24 Lead TSSOP	Tube	-40°C to 85°C
844004BGI-01T	ICS844004BI01	24 Lead TSSOP	2500 Tape & Reel	-40°C to 85°C
844004BGI-01LF	ICS44004BI01L	“Lead-Free” 24 Lead TSSOP	Tube	-40°C to 85°C
844004BGI-01LFT	ICS44004BI01L	“Lead-Free” 24 Lead TSSOP	2500 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
a		1	NRND – Not Recommend for New Designs	5/20/2013

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