

GENERAL DESCRIPTION

The 844021-01 is an Ethernet Clock Generator. The 844021-01 uses an 18pF parallel resonant crystal over the range of 24.5MHz – 34MHz. For Ethernet applications, a 25MHz crystal is used. The 844021-01 has excellent <1ps phase jitter performance, over the 1.875MHz – 20MHz integration range. The 844021-01 is packaged in a small 8-pin TSSOP, making it ideal for use in systems with limited board space.

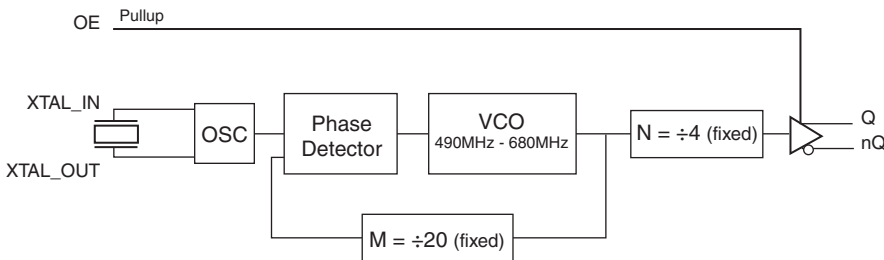
FEATURES

- One Differential LVDS output
- Crystal oscillator interface, 18pF parallel resonant crystal (24.5MHz – 34MHz)
- Output frequency range: 122.5MHz – 170MHz
- VCO range: 490MHz – 680MHz
- RMS phase jitter @ 125MHz, using a 25MHz crystal (1.875MHz – 20MHz): 0.32ps (typical) @ 3.3V
- 3.3V or 2.5V operating supply
- 0°C to 70°C ambient operating temperature
- Available in lead-free (RoHS 6) package

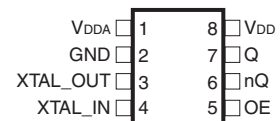
COMMON CONFIGURATION TABLE - Gb ETHERNET

| Inputs | | | | Output Frequency (MHz) |
|-------------------------|----|---|--------------------------|------------------------|
| Crystal Frequency (MHz) | M | N | Multiplication Value M/N | |
| 25 | 20 | 4 | 5 | 125 |
| 26.666 | 20 | 4 | 5 | 133.33 |
| 33.33 | 20 | 4 | 5 | 166.66 |

BLOCK DIAGRAM



PIN ASSIGNMENT



844021-01

8-Lead TSSOP

4.40mm x 3.0mm x 0.925mm
package body
G Package
Top View

TABLE 1. PIN DESCRIPTIONS

| Number | Name | Type | | Description |
|---------|----------------------|--------|--------|--|
| 1 | V _{DDA} | Power | | Analog supply pin. |
| 2 | GND | Power | | Power supply ground. |
| 3, 4 | XTAL_OUT, XTAL_IN | Input | | Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output. |
| 5 | OE | Input | Pullup | Output enable pin. When HIGH, Q/nQ output is active. When LOW, the Q/nQ output is in a high impedance state. LVCMOS/LVT-TL interface levels. |
| 6, 7 | nQ, Q | Output | | Differential clock outputs. LVDS interface levels. |
| 8 | V _{DD} | Power | | Core supply pin. |

NOTE: *Pullup* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---------------------|-----------------------|-----------------|---------|---------|---------|-------|
| C _{IN} | Input Capacitance | | | 4 | | pF |
| R _{PULLUP} | Input Pullup Resistor | | | 51 | | kΩ |

ABSOLUTE MAXIMUM RATINGS

| | |
|--|---------------------------|
| Supply Voltage, V_{DD} | 4.6V |
| Inputs, V_I | -0.5V to $V_{DD} + 0.5$ V |
| Outputs, I_O (LVDS) | |
| Continuous Current | 10mA |
| Surge Current | 15mA |
| Package Thermal Impedance, θ_{JA} | 129.5°C/W (0 mps) |
| Storage Temperature, T_{STG} | -65°C to 150°C |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 3A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $T_A = 0^\circ\text{C}$ TO 70°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-----------------------|-----------------|-----------------|---------|----------|-------|
| V_{DD} | Core Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| V_{DDA} | Analog Supply Voltage | | $V_{DD} - 0.10$ | 3.3 | V_{DD} | V |
| I_{DD} | Power Supply Current | | | | 75 | mA |
| I_{DDA} | Analog Supply Current | | | | 10 | mA |

TABLE 3B. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = 2.5V \pm 5\%$, $T_A = 0^\circ\text{C}$ TO 70°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-----------------------|-----------------|-----------------|---------|----------|-------|
| V_{DD} | Core Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| V_{DDA} | Analog Supply Voltage | | $V_{DD} - 0.10$ | 2.5 | V_{DD} | V |
| I_{DD} | Power Supply Current | | | | 70 | mA |
| I_{DDA} | Analog Supply Current | | | | 10 | mA |

TABLE 3C. LVC MOS/LVTTL DC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$ OR $2.5V \pm 5\%$, $T_A = 0^\circ\text{C}$ TO 70°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|--------------------|---|---------|---------|----------------|---------------|
| V_{IH} | Input High Voltage | $V_{DD} = 3.3V$ | 2 | | $V_{DD} + 0.3$ | V |
| | | $V_{DD} = 2.5V$ | 1.7 | | $V_{DD} + 0.3$ | V |
| V_{IL} | Input Low Voltage | $V_{DD} = 3.3V$ | -0.3 | | 0.8 | V |
| | | $V_{DD} = 2.5V$ | -0.3 | | 0.7 | V |
| I_{IH} | Input High Current | $V_{DD} = V_{IN} = 3.465V$ or $2.625V$ | | | 5 | μA |
| I_{IL} | Input Low Current | $V_{DD} = 3.465V$ or $2.625V$, $V_{IN} = 0V$ | -150 | | | μA |

TABLE 3D. LVDS DC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------|-----------------------------|-----------------|---------|---------|---------|-------|
| V_{OD} | Differential Output Voltage | | 275 | | 425 | mV |
| ΔV_{OD} | V_{OD} Magnitude Change | | | | 50 | mV |
| V_{OS} | Offset Voltage | | 1.15 | | 1.45 | V |
| ΔV_{OS} | V_{OS} Magnitude Change | | | | 50 | mV |

NOTE: Please refer to Parameter Measurement Information for output information.

TABLE 3E. LVDS DC CHARACTERISTICS, $V_{DD} = 2.5V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------|-----------------------------|-----------------|---------|---------|---------|-------|
| V_{OD} | Differential Output Voltage | | 215 | | 430 | mV |
| ΔV_{OD} | V_{OD} Magnitude Change | | | | 50 | mV |
| V_{OS} | Offset Voltage | | 1.05 | | 1.45 | V |
| ΔV_{OS} | V_{OS} Magnitude Change | | | | 50 | mV |

NOTE: Please refer to Parameter Measurement Information for output information.

TABLE 4. CRYSTAL CHARACTERISTICS

| Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|------------------------------------|-----------------|-------------|---------|---------|----------|
| Mode of Oscillation | | Fundamental | | | |
| Frequency | | 24.5 | | 34 | MHz |
| Equivalent Series Resistance (ESR) | | | | 50 | Ω |
| Shunt Capacitance | | | | 7 | pF |

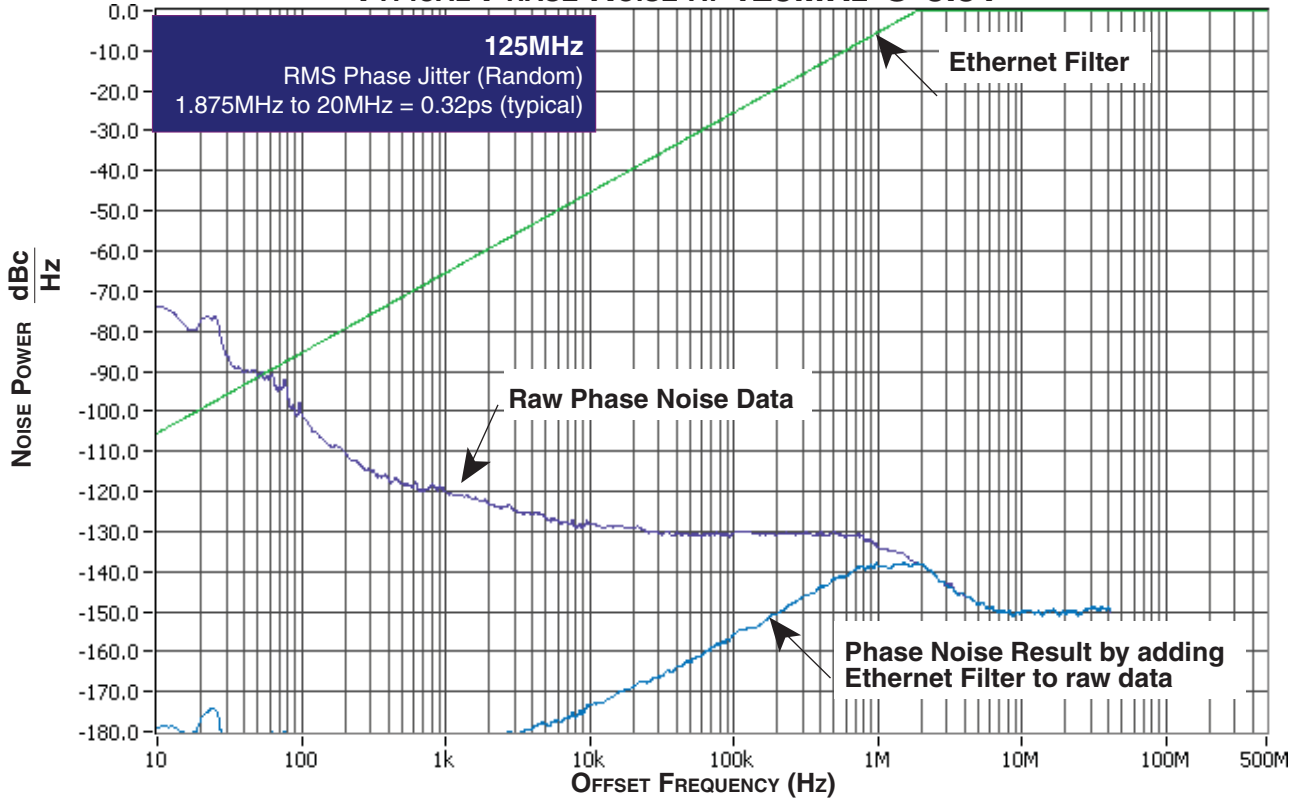
NOTE: It is not recommended to overdrive the crystal input with an external clock.

TABLE 5. AC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$ OR $2.5V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

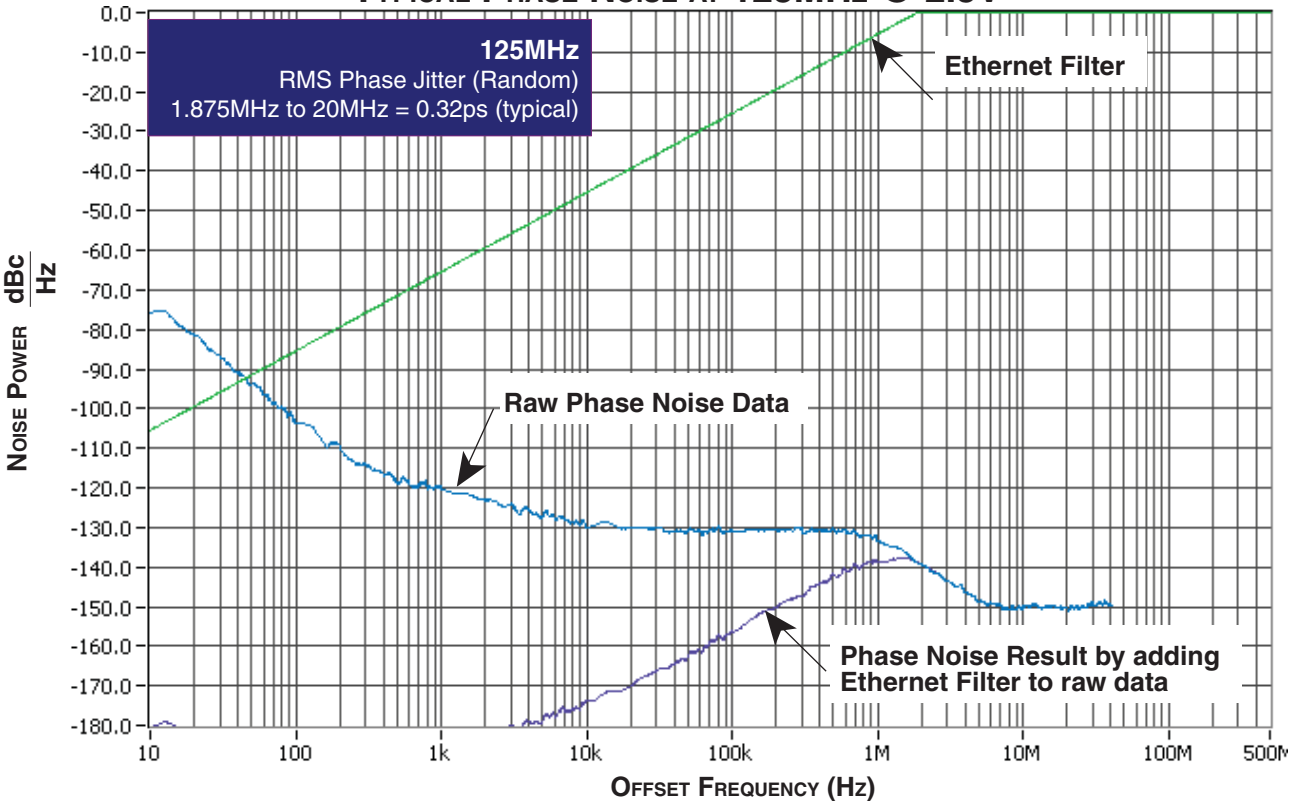
| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------------------|---------------------------------------|---|---------|---------|---------|-------|
| f_{OUT} | Output Frequency | | 122.5 | | 170 | MHz |
| $t_{jit}(\emptyset)$ | RMS Phase Jitter (Random); NOTE 1 | 125MHz @ Integration Range: 1.875MHz - 20MHz | | 0.32 | | ps |
| t_R / t_F | Output Rise/Fall Time | 20% to 80% | 200 | | 400 | ps |
| odc | Output Duty Cycle | | 48 | | 52 | % |

NOTE 1: Please refer to the Phase Noise Plots following this section.

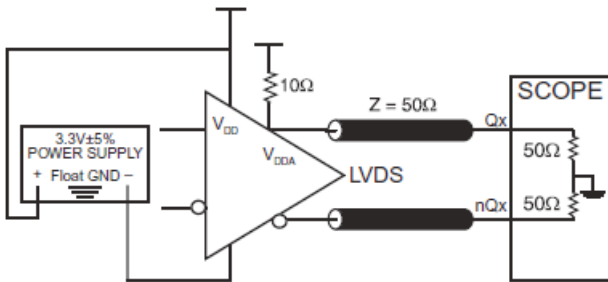
TYPICAL PHASE NOISE AT 125MHz @ 3.3V



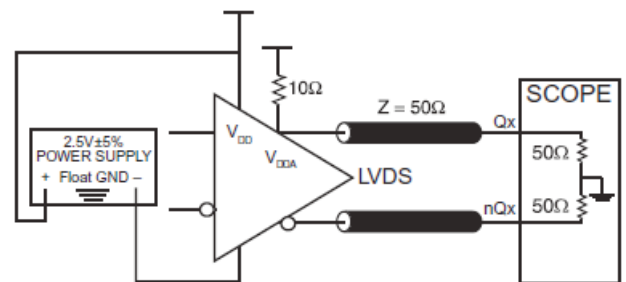
TYPICAL PHASE NOISE AT 125MHz @ 2.5V



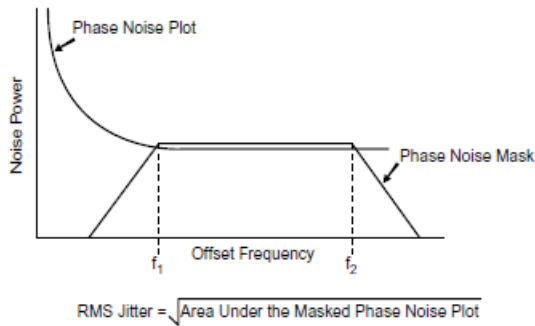
PARAMETER MEASUREMENT INFORMATION



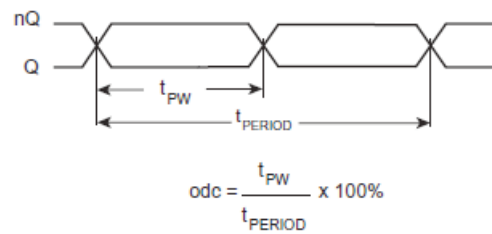
LVDS 3.3V OUTPUT LOAD AC TEST CIRCUIT



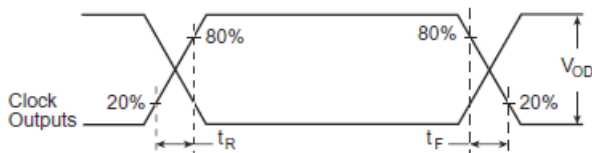
LVDS 2.5V OUTPUT LOAD AC TEST CIRCUIT



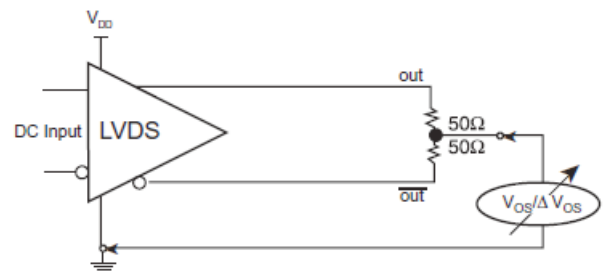
RMS PHASE JITTER



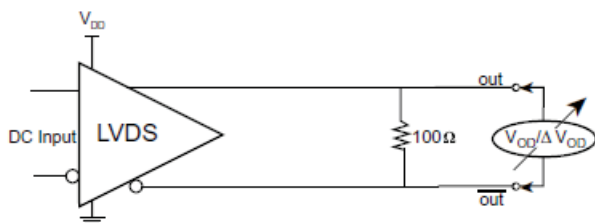
OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



OUTPUT RISE/FALL TIME



OFFSET VOLTAGE SETUP



DIFFERENTIAL OUTPUT VOLTAGE SETUP

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 844021-01 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} and V_{DDA} should be individually connected to the power supply plane through vias, and $0.01\mu\text{F}$ bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional 10Ω resistor along with a $10\mu\text{F}$ bypass capacitor be connected to the V_{DDA} pin.

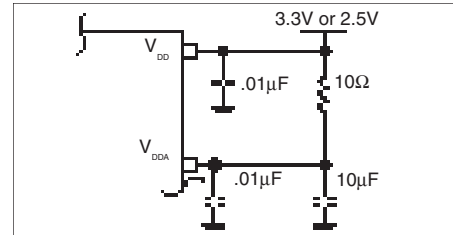


FIGURE 1. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

The 844021-01 has been characterized with 18pF parallel resonant crystals. The capacitor values, $C1$ and $C2$, shown in *Figure 2* below were determined using a 25MHz , 18pF parallel

resonant crystal and were chosen to minimize the ppm error. The optimum $C1$ and $C2$ values can be slightly adjusted for different board layouts.

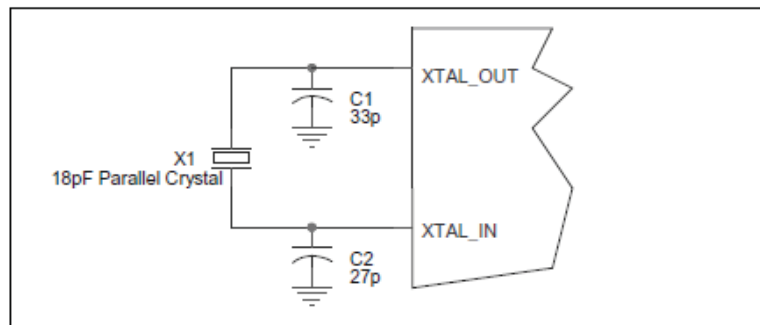


FIGURE 2. CRYSTAL INPUT INTERFACE

3.3V, 2.5V LVDS DRIVER TERMINATION

A general LVDS interface is shown in *Figure 4*. In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near

the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

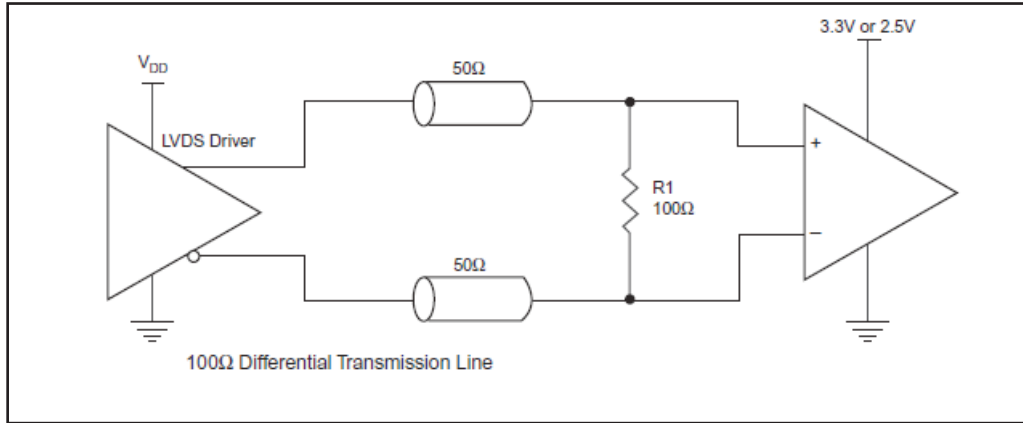


FIGURE 4. TYPICAL LVDS DRIVER TERMINATION

SCHEMATIC LAYOUT

Figure 5 shows an example of 844021-01 application schematic. In this example, the device is operated at $V_{DD} = 3.3V$. The decoupling capacitor should be located as close as possible to the power pin. The 18pF parallel resonant 25MHz crystal is used. The $C1 = 33pF$ and $C2 = 27pF$ are recommended

for frequency accuracy. For different board layout, the $C1$ and $C2$ may be slightly adjusted for optimizing frequency accuracy. For the LVDS output drivers, place a 100Ω resistor as close to the receiver as possible.

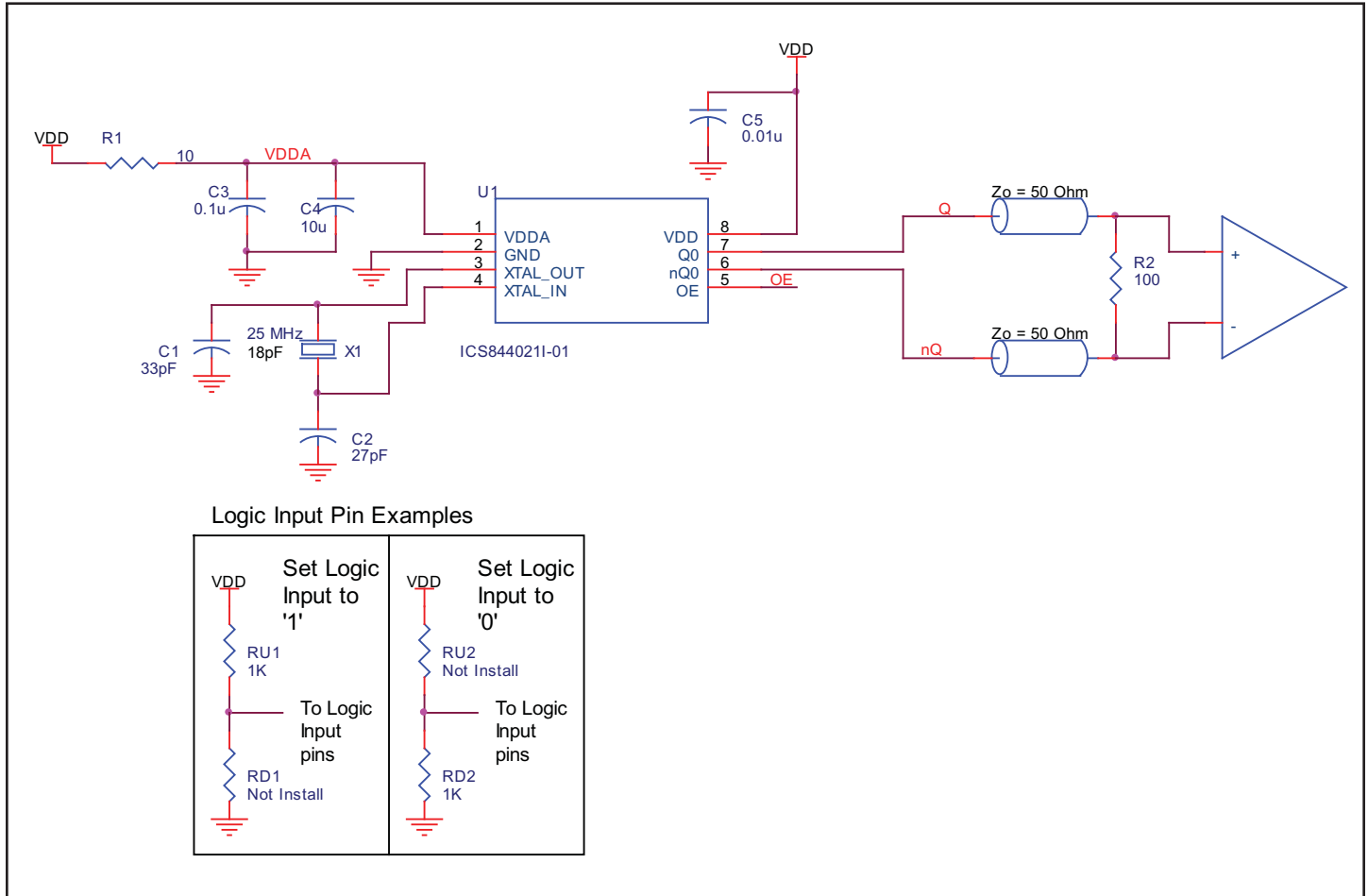


FIGURE 5. 844021-01 SCHEMATIC LAYOUT

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the 844021-01. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 844021-01 is the sum of the core power plus the analog plus the power dissipated in the load(s). The following is the power dissipation for $V_{DD} = 3.3V + 5\% = 3.465V$, which gives worst case results.

- Power (core)_{MAX} = $V_{DD_MAX} * (I_{DD_MAX} + I_{DDA_MAX}) = 3.465V * (75mA + 10mA) = \mathbf{294.5mW}$

2. Junction Temperature.

Junction temperature, T_j, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_total + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_{total} = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 129.5°C/W per Table 6 below.

Therefore, T_j for an ambient temperature of 70°C with all outputs switching is:
 $70^\circ C + 0.295W * 129.5^\circ C/W = 108.2^\circ C$. This is well below the limit of 125°C.

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 8-LEAD TSSOP, FORCED CONVECTION

| θ_{JA} by Velocity (Meters per Second) | | | |
|---|-----------|-----------|-----------|
| | 0 | 1 | 2.5 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 129.5°C/W | 125.5°C/W | 123.5°C/W |

RELIABILITY INFORMATION

TABLE 7. θ_{JA} vs. AIR FLOW TABLE FOR 8 LEAD TSSOP

| θ_{JA} by Velocity (Meters per Second) | | | |
|---|-----------|-----------|-----------|
| | 0 | 1 | 2.5 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 129.5°C/W | 125.5°C/W | 123.5°C/W |

TRANSISTOR COUNT

The transistor count for 844021-01 is: 2533

PACKAGE OUTLINE & DIMENSIONS

PACKAGE OUTLINE - G SUFFIX FOR 8 LEAD TSSOP

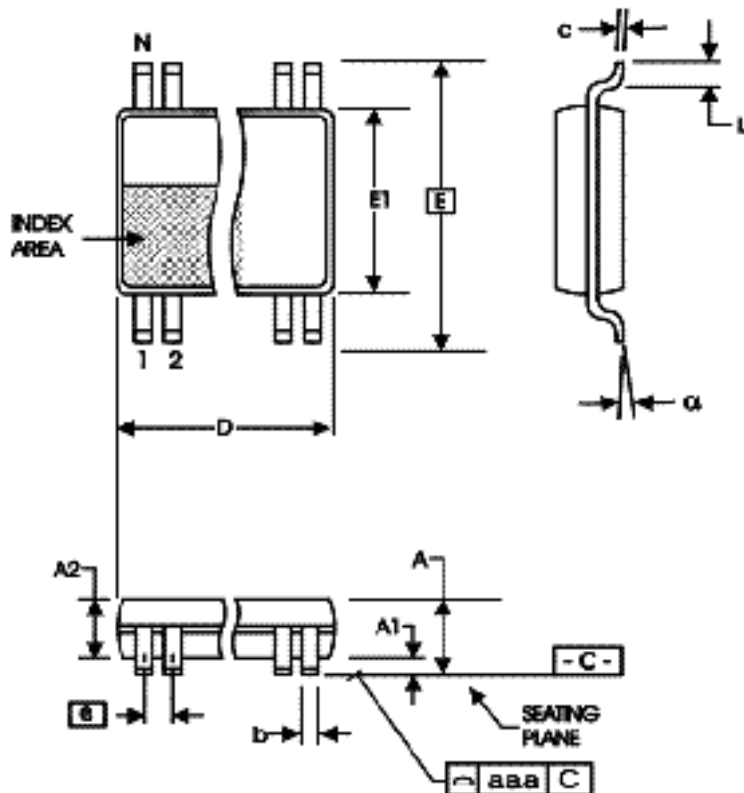


TABLE 8. PACKAGE DIMENSIONS

| SYMBOL | Millimeters | |
|--------|-------------|---------|
| | Minimum | Maximum |
| N | 8 | |
| A | -- | 1.20 |
| A1 | 0.05 | 0.15 |
| A2 | 0.80 | 1.05 |
| b | 0.19 | 0.30 |
| c | 0.09 | 0.20 |
| D | 2.90 | 3.10 |
| E | 6.40 BASIC | |
| E1 | 4.30 | 4.50 |
| e | 0.65 BASIC | |
| L | 0.45 | 0.75 |
| alpha | 0° | 8° |
| aaa | -- | 0.10 |

Reference Document: JEDEC Publication 95, MO-153

TABLE 9. ORDERING INFORMATION

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|-------------------|---------|--------------------------|--------------------|-------------|
| 844021BG-01LF | 1B01L | 8 lead "Lead-Free" TSSOP | tube | 0°C to 70°C |
| 844021BG-01LFT | 1B01L | 8 lead "Lead-Free" TSSOP | tape & reel | 0°C to 70°C |

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET

| Rev | Table | Page | Description of Change | Date |
|------------|--------------|-------------|--|-------------|
| A | T5 | 4 | AC Characteristics Table - Added "or 2.5V±5%" to table title condition. | 9/5/08 |
| A | T4 | 1 | Deleted HiPerClockS references. | 9/23/12 |
| | | 4 | Crystal Characteristics Table - added note. | |
| | | 8 | Deleted application note, LVCMOS to XTAL Interface. | |
| | T9 | 12 | Deleted quantity from tape and reel. | |
| A | T9 | 12 | Ordering Information - removed leaded devices. Updated data sheet format. | 10/26/15 |

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