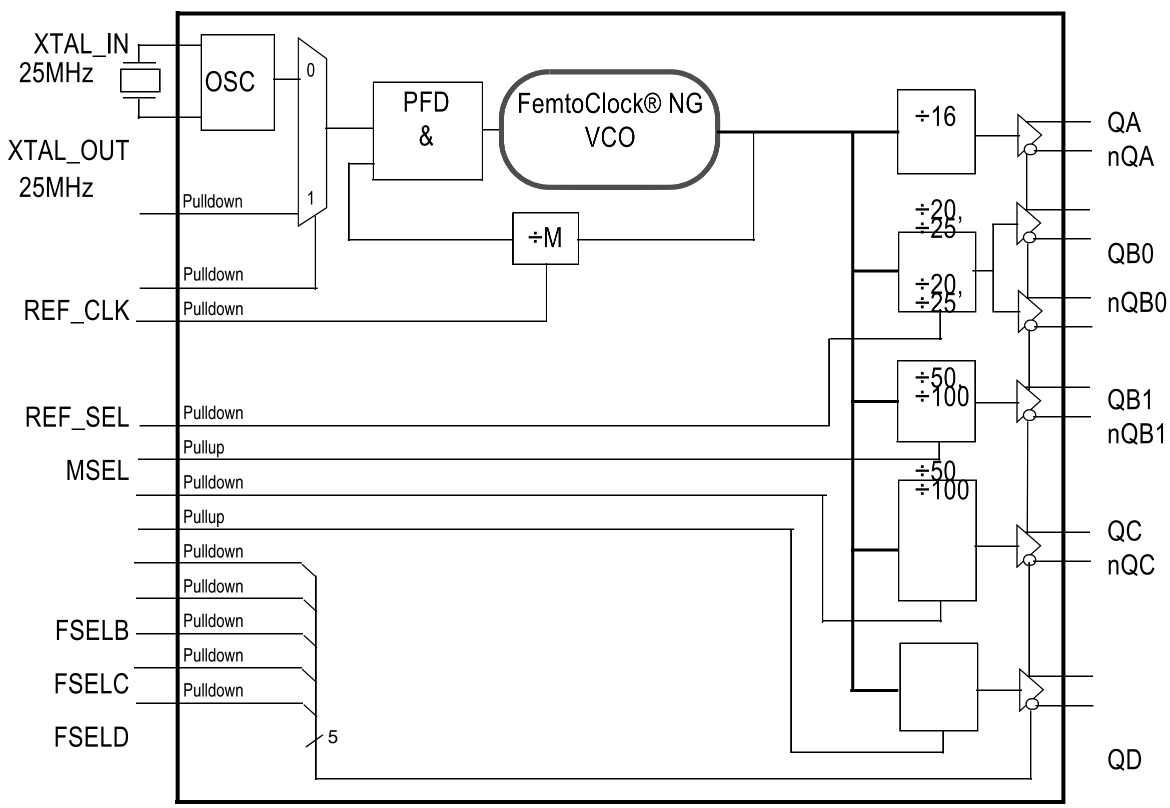
General Description

The 844N255I is a 6-output clock synthesizer designed for wireless infrastructure clock applications. The device uses IDT's fourth generation FemtoClock® NG technology for an optimum of high clock frequency and low phase noise performance, combined with a low power consumption and high power supply noise rejection. The reference frequency is selectable and the following frequency is supported: 25MHz. The synthesizer generates selectable 156.25MHz, 125MHz, 100MHz, 50MHz and 25MHz clock signals. The device is optimized for very low phase noise and cycle to cycle jitter. The synthesized clock frequency and the phase-noise performance are optimized for driving SRIO 1.3 and 2.0 SerDes reference, DSP and host-processor clocks. The device supports a 2.5V voltage supply and is packaged in a small, lead-free (RoHS 6) 48-lead VFQFN package. The extended temperature range supports wireless infrastructure, telecommunication and networking end equipment requirements.

Features

- 4TH generation FemtoClock® NG technology
- Selectable 156.25MHz, 125MHz, 100MHz, 50MHz and 25MHz output clock signals synthesized from a 25MHz reference frequency
- Six differential LVDS clock outputs
- Crystal interface designed for a 25MHz crystal
- RMS phase jitter @ 156.25MHz, using a 25MHz crystal (1MHz - 20MHz): 0.27ps (typical)
- Internal regulator for optimum noise rejection
- LVCMOS interface levels for the frequency select and output enable inputs
- Full 2.5V supply voltage
- Lead-free (RoHS 6) 48-lead VFQFN package
- -40°C to 85°C ambient operating temperature

Block Diagram



Pin Assignment

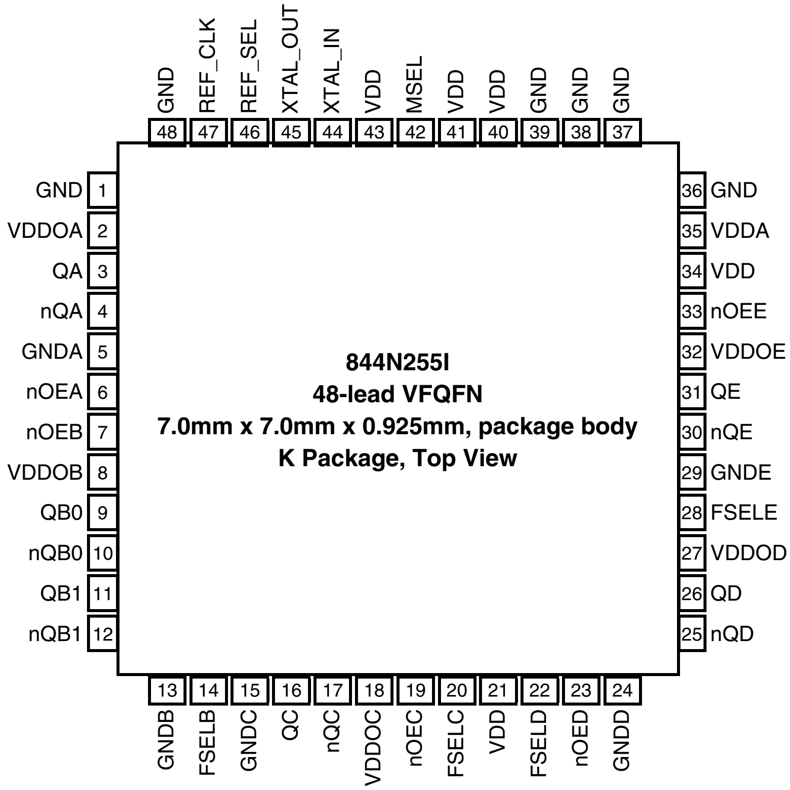


Table 1. Pin Descriptions

Number	Name	Type		Description
1, 36, 37, 38, 39, 48	GND	Power		Power supply ground.
2	V_{DDOA}	Power		Output supply pin for the output QA.
3, 4	QA, nQA	Output		Differential clock output A. LVDS interface levels.
5	GNDA	Power		Power supply ground for the output QA.
6	nOEA	Input	Pulldown	Output enable input. See Table 3G. LVCMOS/LVTTL interface levels.
7	nOEB	Input	Pulldown	Output enable input. See Table 3H. LVCMOS/LVTTL interface levels.
8	V_{DDOB}	Power		Output supply pin for the Bank QB outputs.
9, 10, 11, 12	QB0, nQB0, QB1, nQB1	Output		Differential clock outputs (Bank B). LVDS interface levels.
13	GNDB	Power		Power supply ground for the outputs QB0 and QB1.
14	FSELB	Input	Pulldown	Frequency select input for Bank B outputs. See Table 3C. LVCMOS/LVTTL interface levels.
15	GNDC	Power		Power supply ground for the output QC.
16, 17	QC, nQC	Output		Differential clock output C. LVDS interface levels.
18	V_{DDOC}	Power		Output supply pin for the output QC.
19	nOEC	Input	Pulldown	Output enable input. See Table 3I. LVCMOS/LVTTL interface levels.
20	FSELC	Input	Pullup	Frequency select input for output QC. See Table 3D. LVCMOS/LVTTL interface levels.
21, 34, 40, 41, 43	V_{DD}	Power		Core supply pin.
22	FSELD	Input	Pulldown	Frequency select input for output QD. See Table 3E. LVCMOS/LVTTL interface levels.
23	nOED	Input	Pulldown	Output enable input. See Table 3J. LVCMOS/LVTTL interface levels.
24	GNDD	Power		Power supply ground for the output QD.
25, 26	nQD, QD	Output		Differential clock output D. LVDS interface levels.
27	V_{DDOD}	Power		Output supply pin for the output QD.
28	FSELE	Input	Pullup	Frequency select input for output QE. See Table 3F. LVCMOS/LVTTL interface levels.
29	GNDE	Power		Power supply ground for the output QE.
30, 31	nQE, QE	Output		Differential clock output E. LVDS interface levels.
32	V_{DDOE}	Power		Output supply pin for the output QE.
33	nOEE	Input	Pulldown	Output enable input. See Table 3K. LVCMOS/LVTTL interface levels.
35	V_{DDA}	Power		Analog power supply.
42	MSEL	Input	Pulldown	Unused control input. Connect to logic LOW level. See Table 3A. LVCMOS/LVTTL interface levels.
44, 45	XTAL_IN, XTAL_OUT	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
46	REF_SEL	Input	Pulldown	Reference select input. See Table 3B for function. LVCMOS/LVTTL interface levels.
47	REF_CLK	Input	Pulldown	Alternative reference clock input. See Table 3B. LVCMOS/LVTTL interface levels.

NOTE: *Pulldown and Pullup* refer to an internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			3.5		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{PULLUP}	Input Pullup Resistor			51		kΩ

Function Tables

Table 3A. Input Reference Frequency and PLL Feedback Multiplier

Reference Frequency Select	Reference Frequency	PLL Feedback Multiplier M
MSEL	f_{ref}	
0 (default)	25MHz	100

Table 3B. PLL Reference Clock Select Function Table

Input	Operation
REF_SEL	
0 (default)	The crystal interface is selected as reference clock. Crystal frequency is 25MHz.
1	The external reference input REF_CLK is selected.

NOTE: REF_SEL is an asynchronous control.

Table 3C. Output QB[1:0] Frequency Select Function Table

Input	QB[1:0], nQB[1:0] Frequency (MHz)
FSELB	
0 (default)	125
1	100

NOTE: FSELB is an asynchronous control.

Table 3D. Output QC Frequency Select Function Table

Input	QC, nQC Frequency (MHz)
FSELC	
0	125
1 (default)	100

NOTE: FSELC is an asynchronous control.

Table 3E. Output QD Frequency Select Function Table

Input	QD, nQD Frequency (MHz)
FSELD	
0 (default)	50
1	25

NOTE: FSELD is an asynchronous control.

Table 3F. Output QE Frequency Select Function Table

Input	QE, nQE Frequency (MHz)
FSELE	
0	50
1 (default)	25

NOTE 1: FSELE is an asynchronous control.

Table 3G. nOEA Output Enable Function Table

Input	QA, nQA Frequency (MHz)
nOEA	
0 (default)	Output enabled
1	Output disabled in high-impedance state

NOTE: nOEA is an asynchronous control.

Table 3H. nOEB Output Enable Function Table

Input	Operation
nOEB	
0 (default)	QB0, nQB0 - QB1, nQB1 outputs are enabled
1	QB0, nQB0 - QB1, nQB1 Outputs are disabled (high-impedance)

NOTE: nOEB is an asynchronous control.

Table 3I. nOEC Output Enable Function Table

Input	Operation
nOEC	
0 (default)	QC, nQC output is enabled
1	QC, nQC output is disabled (high-impedance)

NOTE: nOEC is an asynchronous control.

Table 3J. nOED Output Enable Function Table

Input	Operation
nOED	
0 (default)	QD, nQD output is enabled
1	QD, nQD output is disabled (high-impedance)

NOTE: nOED is an asynchronous control.

Table 3K. nOEE Output Enable Function Table

Input	Operation
nOEE	
0 (default)	QE, nQE output is enabled
1	QE, nQE is disabled (high-impedance)

NOTE 1: nOEE is an asynchronous control.

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	3.63V
Inputs, V_I Crystal Inputs Other Inputs	 0V to 2V -0.5V to V_{DD} + 0.5V
Outputs, I_O Continuous Current Surge Current	 10mA 15mA
Package Thermal Impedance, θ_{JA}	29°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C
ESD - Human Body Model, NOTE 1	2000V
ESD - Charged Device Model, NOTE 1	1500V

NOTE 1: According to JEDEC/JESD 22-A114/22-C101.

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDOX}$ = 2.5V±5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5V	2.625	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.24	2.5V	V_{DD}	V
V_{DDOX}	Output Supply Voltage		2.375	2.5V	2.625	V
I_{DD}	Power Supply Current				140	mA
I_{DDA}	Analog Supply Current				24	mA
I_{DDOx}	Output Supply Current				111	mA

NOTE: V_{DDOX} denotes V_{DDOA}, V_{DDOB}, V_{DDOC}, V_{DDOD}, and V_{DDOE}.
NOTE: I_{DDOX} denotes I_{DDOA}, I_{DDOB}, I_{DDOC}, I_{DDOD}, and I_{DDOE}.

Table 4B. LVCMOS/LVTTL Input DC Characteristics, $V_{DD} = V_{DDOX}$ = 2.5V±5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	nOE[A:E], REF_CLK, REF_SEL, FSELB, FSELD, MSEL	$V_{DD} = V_{IN}$ = 2.625V			150	µA
		FSELC, FSELE	$V_{DD} = V_{IN}$ = 2.625V	5			µA
I_{IL}	Input Low Current	nOE[A:E], REF_CLK, REF_SEL, FSELB, FSELD, MSEL	V_{DD} = 2.625V, V_{IN} = 0V	-5			µA
		FSELC, FSELE	V_{DD} = 2.625V, V_{IN} = 0V			-150	µA

NOTE: V_{DDOX} denotes V_{DDOA}, V_{DDOB}, V_{DDOC}, V_{DDOD}, and V_{DDOE}.

Table 4C. LVDS DC Characteristics, V_{DD} **=** V_{DDOX} **= 2.5V±5%,** T_A **= -40°C to 85°C**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		247		454	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.125		1.375	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

NOTE: V_{DDOX} denotes V_{DDOA}, V_{DDOB}, V_{DDOC}, V_{DDOD}, and V_{DDOE}.

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental		
Frequency			25		MHz
Equivalent Series Resistance (ESR)				80	Ω
Shunt Capacitance				7	pF
Drive Level			205		µW

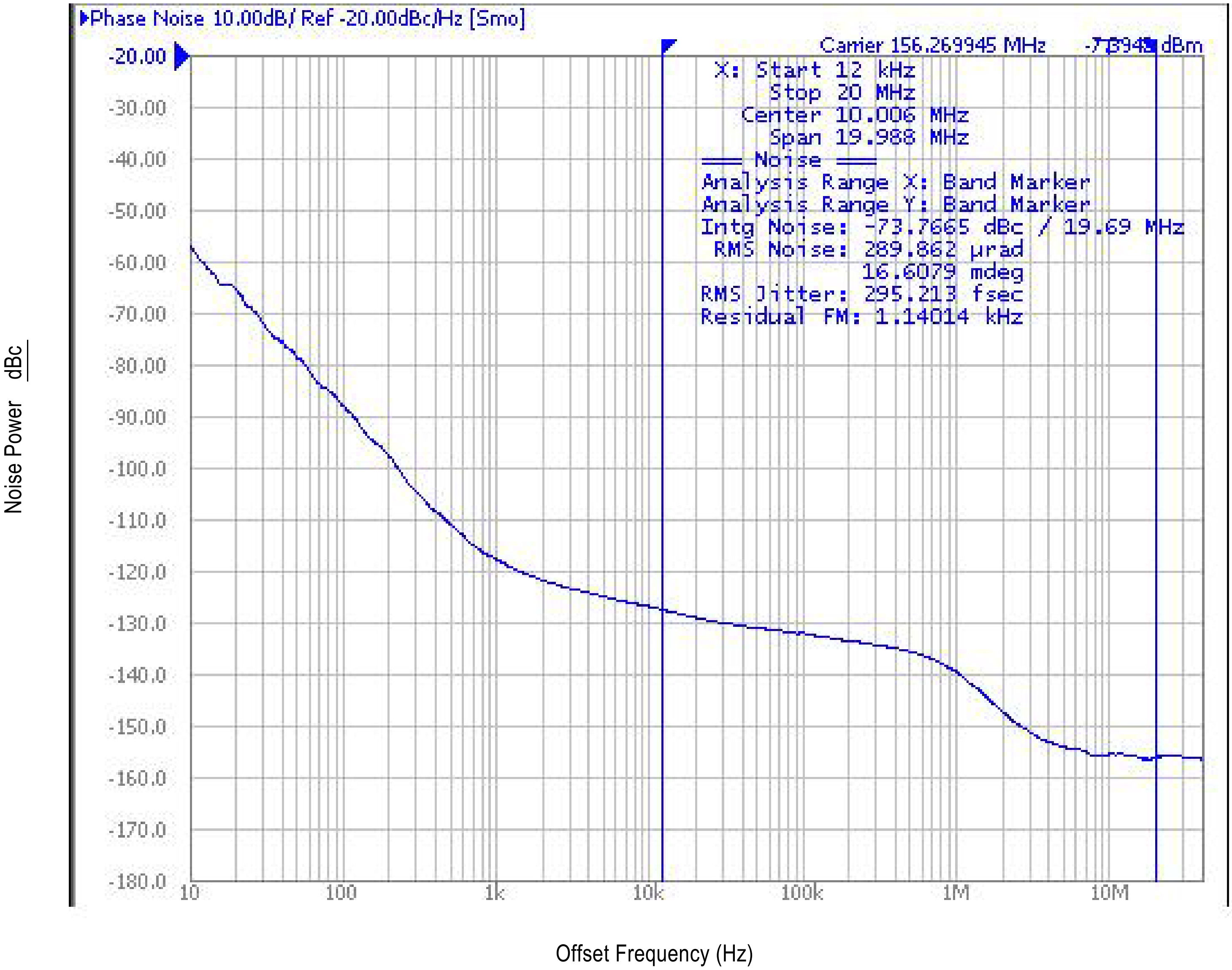
AC Electrical Characteristics

Table 6. AC Characteristics, $V_{DD} = V_{DDOX}$ = 2.5V±5%, T_A = -40°C to 85°C

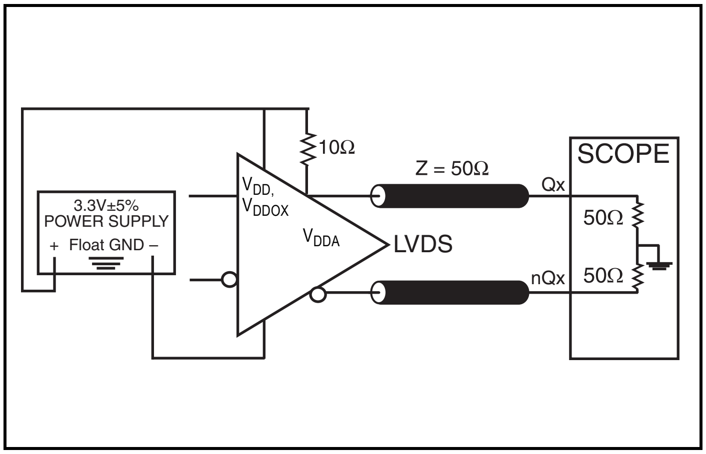
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	QA		125		156.25	MHz
		QB, QC		100		125	MHz
		QD		25		50	MHz
		QE		25		50	MHz
f_{REF}	Reference Frequency				25		MHz
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 1	156.25MHz	Integration Range: 1MHz – 20MHz		0.27	0.34	ps
			Integration Range: 12kHz – 20MHz		0.30	0.39	ps
		125MHz	Integration Range: 12kHz – 20MHz		0.30	0.43	ps
			Integration Range: 10kHz – 1.5MHz		0.26	0.40	ps
			Integration Range: 1.5MHz – 62.5MHz		0.25	0.40	ps
		100MHz	Integration Range: 12kHz – 20MHz		0.31	0.43	ps
			Integration Range: 10kHz – 1.5MHz		0.26	0.38	ps
			Integration Range: 1.5MHz – 50MHz		0.28	0.42	ps
Φ_N	Single-Side Band Noise Power	156.25MHz	Offset: 100Hz		-58		dBc/Hz
			Offset: 1kHz		-117		dBc/Hz
			Offset: 10kHz		-127		dBc/Hz
			Offset: 100kHz		-133		dBc/Hz
			Offset: 20MHz		-157		dBc/Hz
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 2		100MHz			6.8	ps
			125MHz			6.7	ps
			156.25MHz			7.3	ps
tsk(b)	Bank Skew; NOTE 2, 3	QB[0:1], nQB[0:1]			8	16	ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	250		650	ps
t_{LOCK}	PLL Lock Time					10	ms
odc	Output Duty Cycle			48		52	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: Characterized with 25MHz crystal, unless otherwise noted.
NOTE: V_{DDOX} denotes V_{DDOA}, V_{DDOB}, V_{DDOC}, V_{DDOD}, and V_{DDOE}.
NOTE 1: Please refer to the phase noise plots.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Defined as skew within a bank of outputs at the same voltage and with equal load conditions.

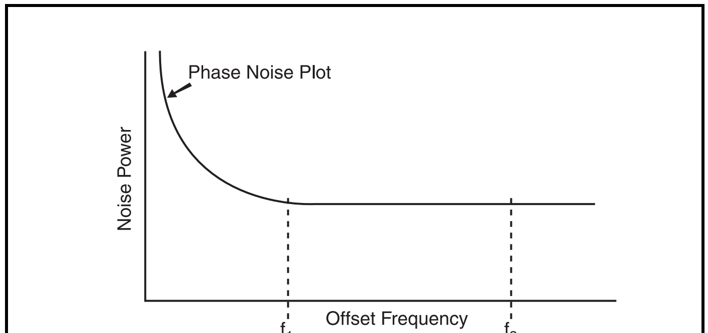
Typical Phase Noise at 156.25MHz



Parameter Measurement Information



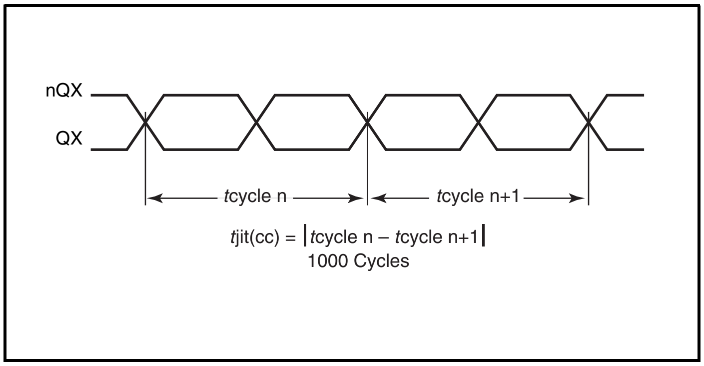
LVDS Output Load AC Test Circuit



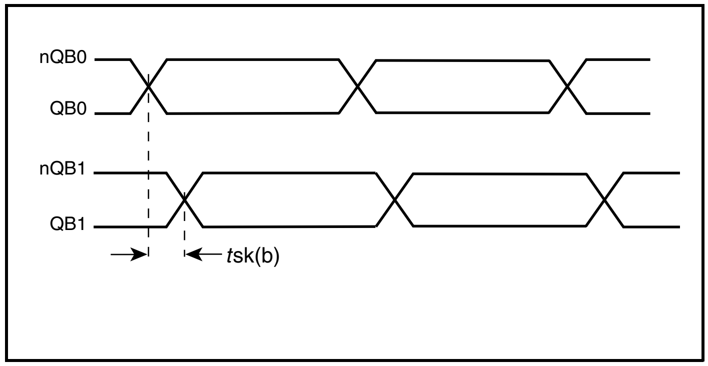
RMS Phase Jitter =

$$\frac{1}{\sqrt{2} * \pi * f} * \sqrt{\text{Area Under Curve Defined by the Offset Frequency Markers}}$$

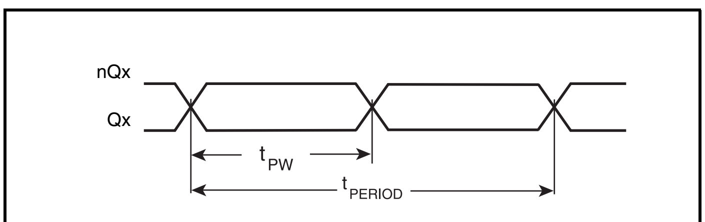
RMS Phase Jitter



Cycle-to-Cycle Jitter

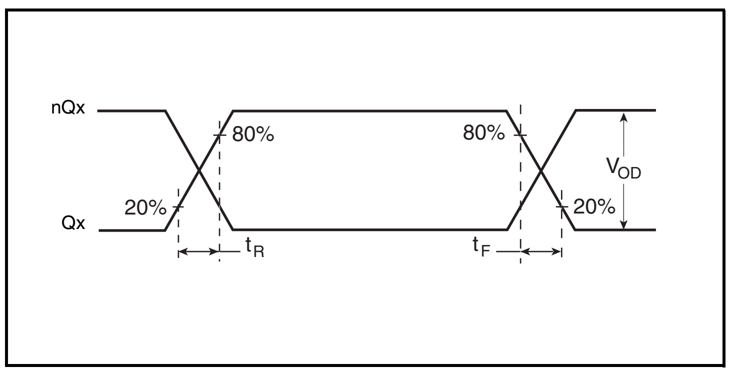


Bank Skew



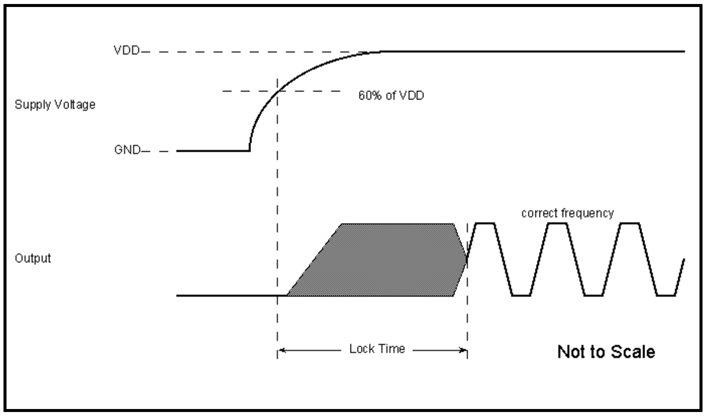
$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

Output Duty Cycle/Pulse Width/Period

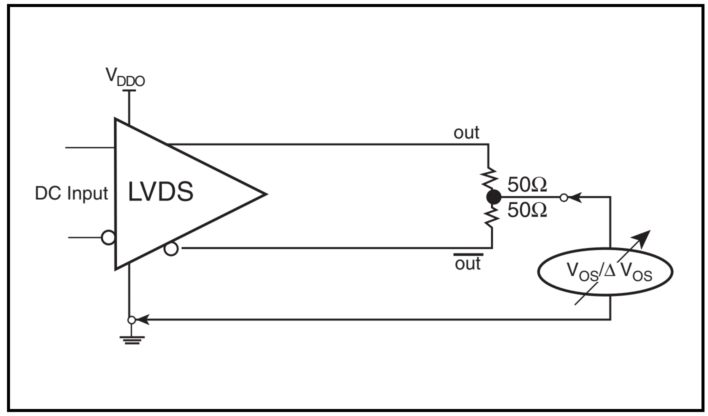


Output Rise/Fall Time

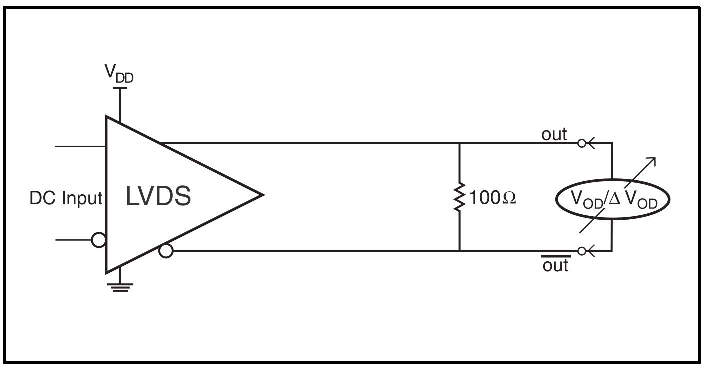
Parameter Measurement Information, continued



Lock Time



Offset Voltage Setup



Differential Output Voltage Setup

Applications Information

Interface to IDT SRIO Switches

The 844N255I is designed for driving the differential reference clock input (REF_CLK) of IDT's SRIO 1.3 and 2.0 switch devices. The LVDS outputs of the ICS844N255I have the low-jitter, differential voltage and impedance characteristics required to provide a high-quality 156.25MHz clock signal for both SRIO 1.3 and 2.0 switch devices. Please refer to *Figure 1* for a suggested interfaces. In Figure 1, the AC-coupling capacitors are mandatory by the IDT SRIO switch devices. The differential REF_CLK input is internally re-biased and AC-terminated. The interface circuit is optimized for 50Ω transmission lines and generates the voltage swing required to reliably drive the clock reference input of a IDT SRIO switch. Please refer to IDT's SRIO device datasheet for more details.

Figure 1 shows the recommended interface circuit for driving the 156.25MHz reference clock of an IDT SRIO 2.0 switch by a LVDS output of the ICS844N255I. The LVDS-to-differential interface as shown in Figure 1 does not require any external termination resistors: the ICS844N255I driver contains an internal source termination at QA0 and QA1. The differential REF_CLK input contains an internal AC-termination (R_L) and re-bias (V_{BIAS}).

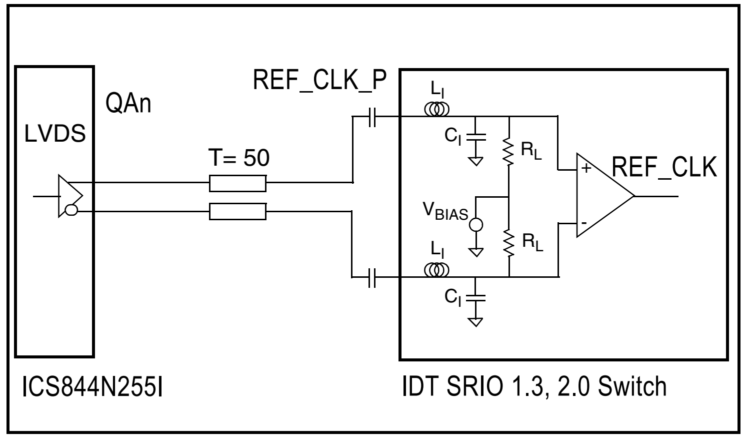


Figure 1. LVDS-to-SRIO 2.0 Reference Clock Interface

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pullups and pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

REF_CLK Input

For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the REF_CLK to ground.

Outputs:

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

Overdriving the XTAL Interface

The XTAL_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/nS. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. *Figure 2A* shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and changing R2 to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. *Figure 2B* shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

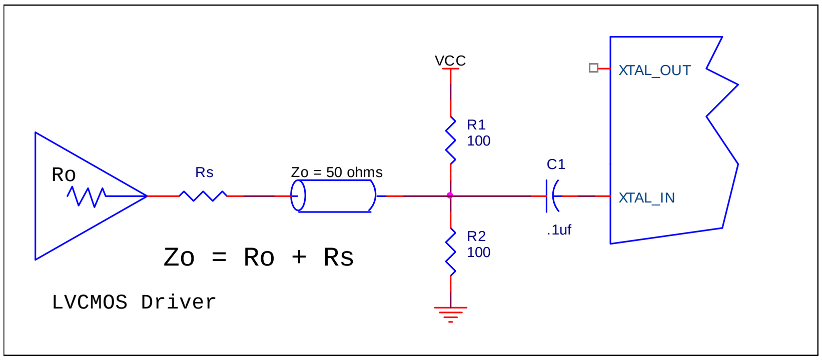


Figure 2A. General Diagram for LVCMOS Driver to XTAL Input Interface

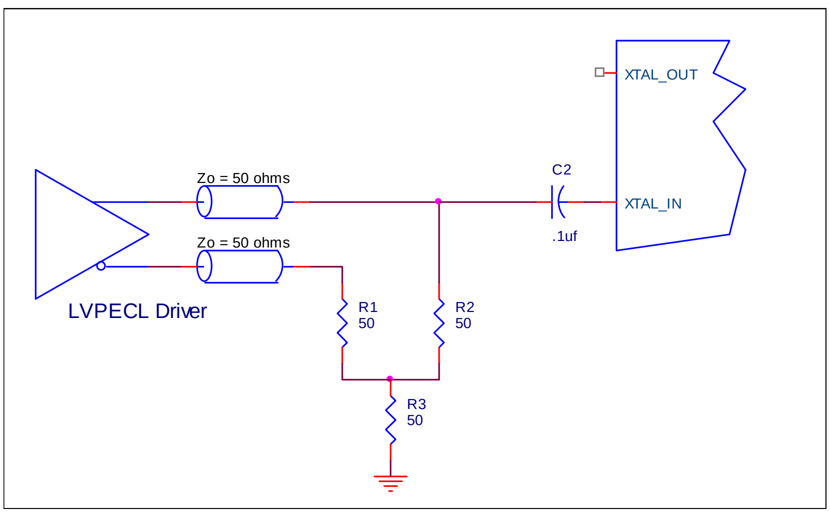


Figure 2B. General Diagram for LVPECL Driver to XTAL Input Interface

LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in *Figure 3A* can be used with either type of output structure. *Figure 3B*, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

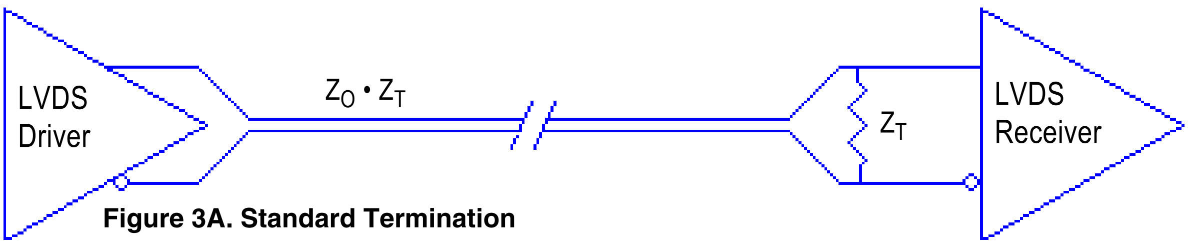


Figure 3A. Standard Termination

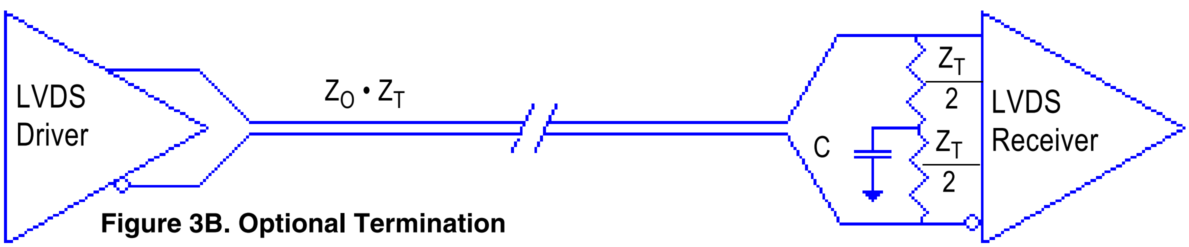


Figure 3B. Optional Termination

LVDS Termination

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

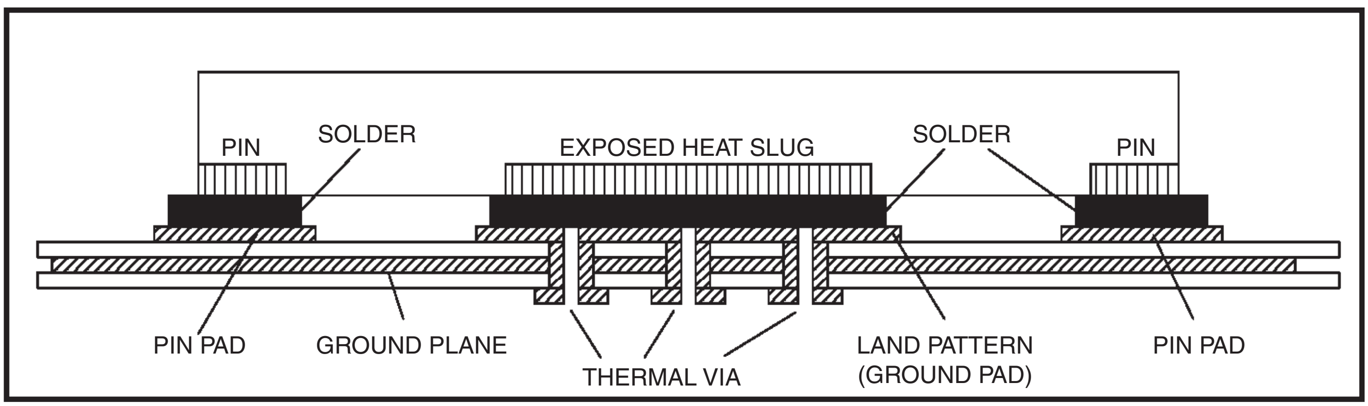


Figure 4. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Schematic Layout

Figure 5 shows an example of 844N255I application schematic. In this example, the device is operated at $V_{DD} = V_{DDOA} = V_{DDOB} = V_{DDOC} = V_{DDOD} = V_{DDOE} = 2.5V$. The 16pF parallel resonant 25MHz crystal is used. The load capacitance C1 = 15pF and C2 = 15pF are recommended for frequency accuracy. Depending on the parasitics of the printed circuit board layout, these values might require a slight adjustment to optimize the frequency accuracy. Crystals with other load capacitance specifications can be used. For this device, the crystal load capacitors are required for proper operation.

As with any high speed analog circuitry, the power supply pins are vulnerable to noise. To achieve optimum jitter performance, power supply isolation is required. The 844N255I provides separate power supplies to isolate from coupling into the internal PLL.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1uF capacitor in each power pin filter should be placed on the device side of the PCB and the other components can be placed on the opposite side.

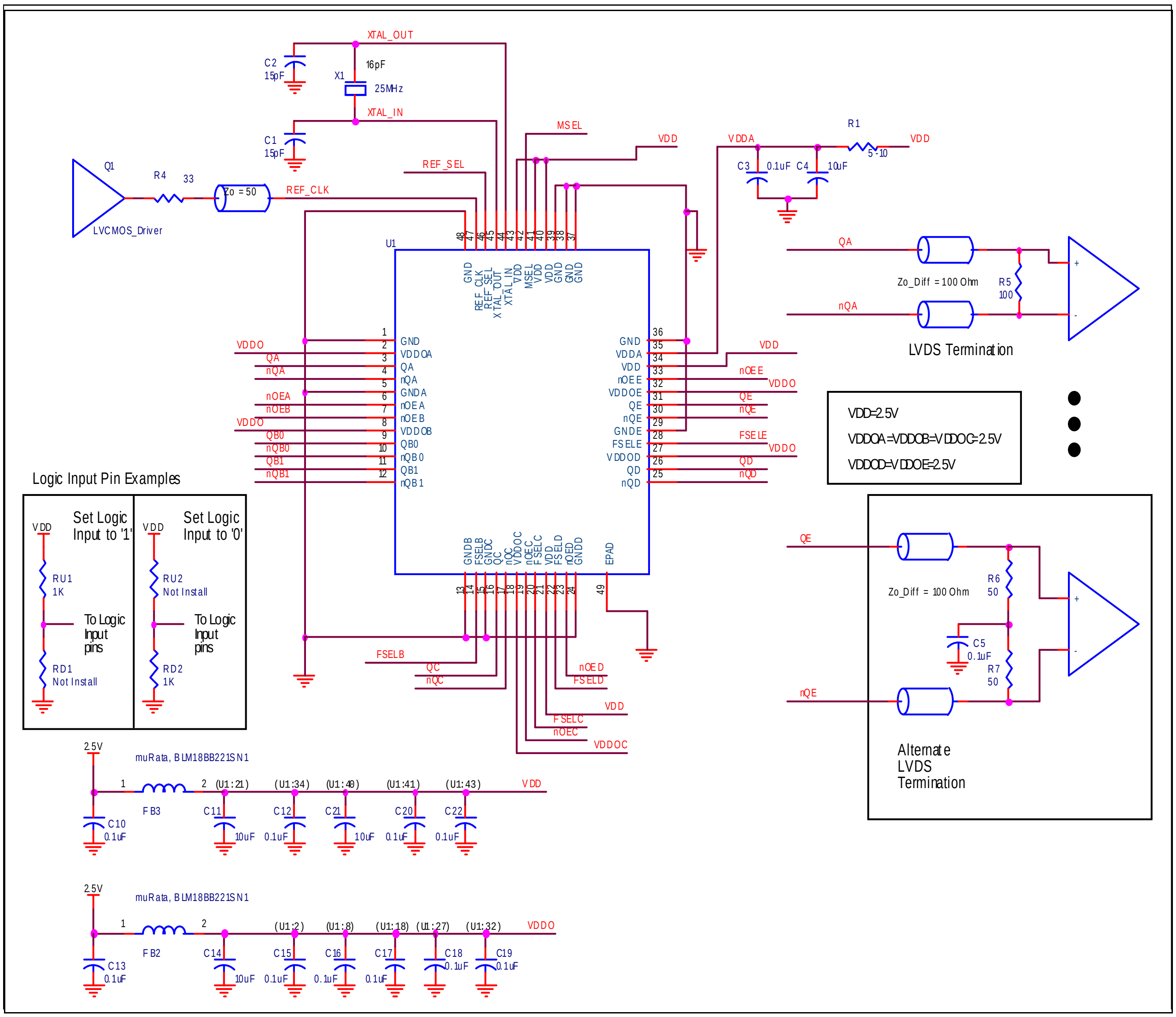


Figure 5. 844N255I Application Schematic

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supply frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitances in the local area of all devices.

The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure the logic control inputs are properly set.

Power Considerations

This section provides information on power dissipation and junction temperature for the 844N255I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 844N255I is the sum of the core power plus the analog power plus the power dissipation in the load(s). The following is the power dissipation for V_{DD} = 2.5V + 5% = 2.625V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipation in the load.

- Power $(core)_{MAX} = V_{DD\_MAX} * (I_{DD\_MAX} + I_{DDA\_MAX})$ = 2.625V * (140mA + 24mA) = **430.5mW**
- Power $(outputs)_{MAX} = V_{DDO\_MAX} * I_{DDO\_MAX}$ = 2.625V * 111mA = **291.375mW**

Total Power$_{\_MAX}$ = 430.5mW + 291.375mW = **721.875mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow of and a multi-layer board, the appropriate value is 29°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.722W * 29°C/W = 105.9°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance θ_{JA} for 48 Lead VFQFN, Forced Convection

θ_{JA} **by Velocity**			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	29.0°C/W	25.4°C/W	22.8°C/W

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for a 48-lead VFQFN

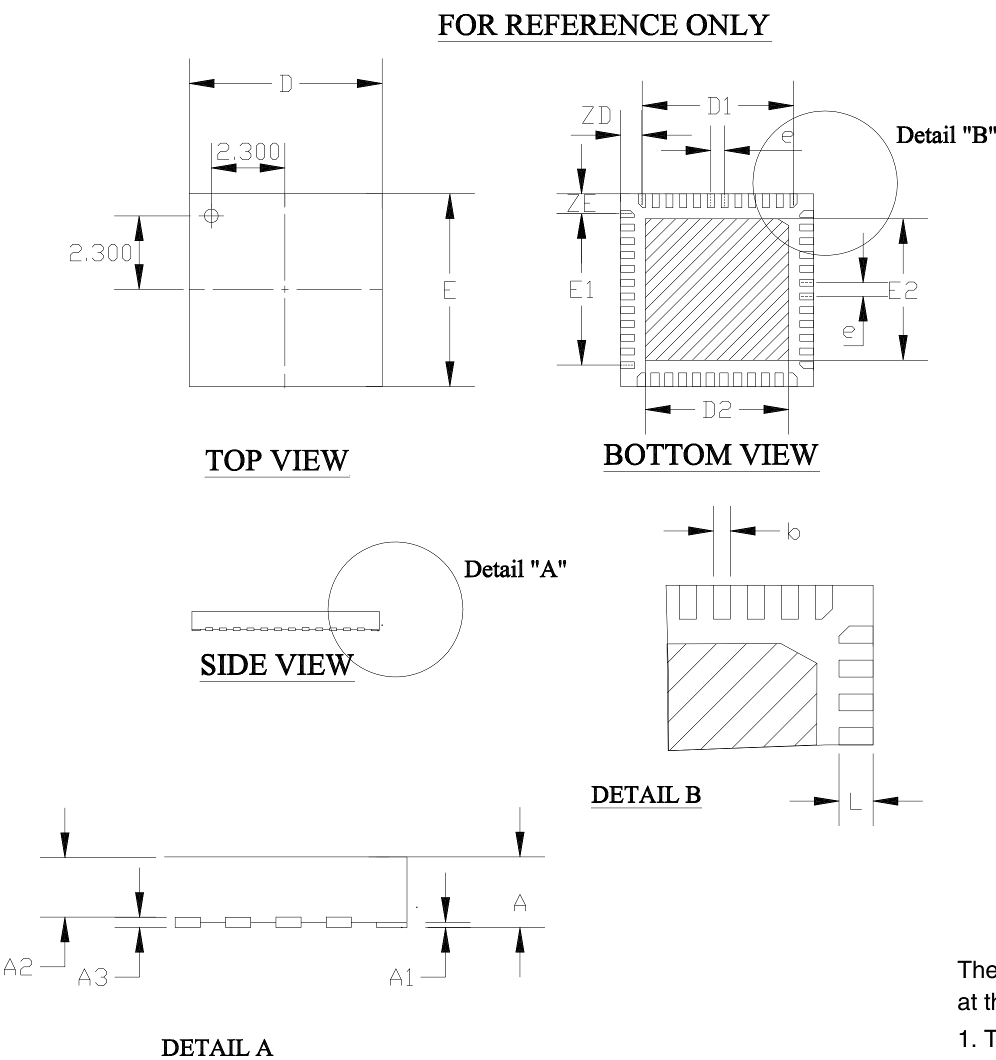
θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	29.0°C/W	25.4°C/W	22.8°C/W

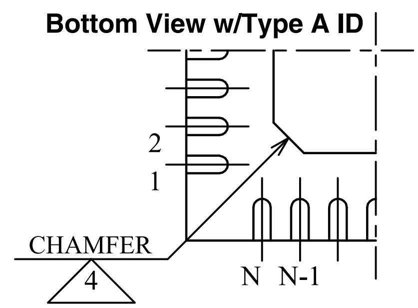
Transistor Count

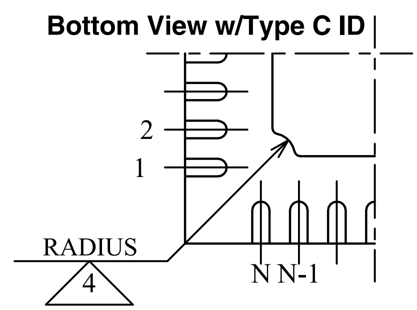
The transistor count for 844N255I is: 21,109

Package Outline and Package Dimensions

Package Outputline -K Suffix for 48 Lead VFQFN







There are 2 methods of indicating pin 1 corner at the back of the VFQFN package:

1. Type A: Chamfer on the paddle (near pin 1)
2. Type C: Mouse bite on the paddle (near pin 1)

Table 9. PackageDimensions for 48 Lead VFQFN

All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		48	
A		0.8	0.9
A1	0	0.02	0.05
A3		0.2 Ref.	
b	0.18	0.25	0.30
D & E		7.00 Basic	
D1 & E1		5.50 Basic	
D2 & E2	5.50	5.65	5.80
e		0.50 Basic	
R		0.20~0.25	
ZD & ZE		0.75 Basic	
L	0.35	0.40	0.45

Reference Document: IDT Drawing #PSC-4203

Ordering Information

Table 10. Ordering Information Table

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
844N255AKILF	ICS844N255AIL	Lead-Free, 48-lead VFQFN	Tray	-40°C to 85°C
844N255AKILFT	ICS844N255AIL	Lead-Free, 48-lead VFQFN	Tape & Reel	-40°C to 85°C

Revision History

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Revision Date	Description of Change
April 28, 2016	▪ Remove ICS from the part number where needed. ▪ Ordering Information - Removed quantity from tape and reel. Deleted LF note below table. ▪ Updated data sheet header and footer.

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