Low Skew, 1-to16, Differential-to-2.5V LVPECL Fanout Buffer

General Description

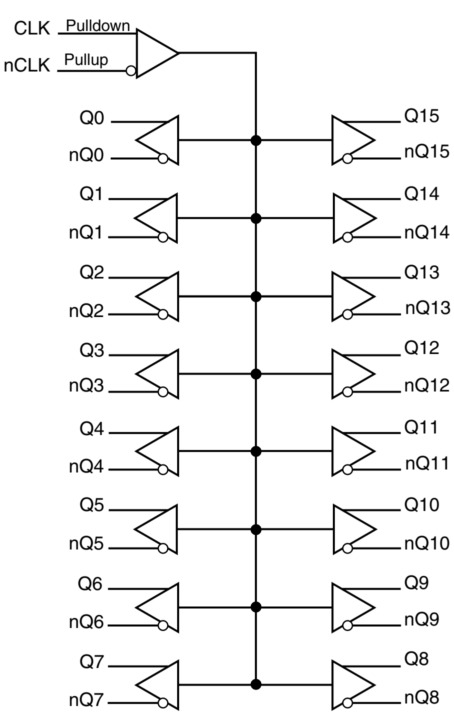
The 8530 is a low skew, 1-to-16 Differential-to- 2.5V LVPECL Fanout Buffer. The CLK, nCLK pair can accept most standard differential input levels. The high gain differential amplifier accepts peak-to-peak input voltages as small as 150mV, as long as the common mode voltage is within the specified minimum and maximum range.

Guaranteed output and part-to-part skew characteristics make the 8530 ideal for those clock distribution applications demanding well defined performance and repeatability.

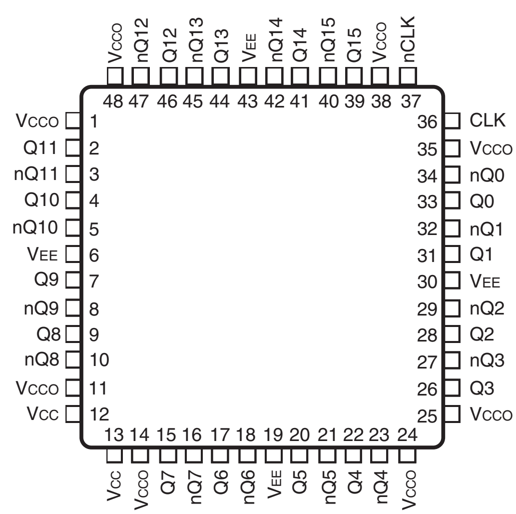
Features

- Sixteen differential LVPECL output pairs
- CLK, nCLK input pair
- CLK, nCLK pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, HCSL, SSTL
- Maximum output frequency: 500MHz
- Translates any single-ended input signal to 2.5V LVPECL levels with a resistor bias on nCLK input
- Output skew: 50ps (maximum)
- Part-to-part skew: 250ps (maximum)
- Propagation delay: 2ns (maximum)
- 3.3V core, 2.5V output operating supply
- 0°C to 70°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Block Diagram



Pin Assignment



8530

48-Lead LQFP
7mm x 7mm x 1.4mm package body
Y Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 11, 14, 24, 25, 35, 38, 48	V_{CCO}	Power		Output power supply pins.
2, 3	Q11, nQ11	Output		Differential output pair. LVPECL interface levels.
4, 5	Q10, nQ10	Output		Differential output pair. LVPECL interface levels.
6, 19, 30, 43	V_{EE}	Power		Negative power supply pins.
7, 8	Q9, nQ9	Output		Differential output pair. LVPECL interface levels.
9, 10	Q8, nQ8	Output		Differential output pair. LVPECL interface levels.
12, 13	V_{CC}	Power		Positive power supply pins.
15, 16	Q7, nQ7	Output		Differential output pair. LVPECL interface levels.
17, 18	Q6, nQ6	Output		Differential output pair. LVPECL interface levels.
20, 21	Q5, nQ5	Output		Differential output pair. LVPECL interface levels.
22, 23	Q4, nQ4	Output		Differential output pair. LVPECL interface levels.
26, 27	Q3, nQ3	Output		Differential output pair. LVPECL interface levels.
28, 29	Q2, nQ2	Output		Differential output pair. LVPECL interface levels.
31, 32	Q1, nQ1	Output		Differential output pair. LVPECL interface levels.
33, 34	Q0, nQ0	Output		Differential output pair. LVPECL interface levels.
36	CLK	Input	Pulldown	Non-inverting differential clock input.
37	nCLK	Input	Pullup	Inverting differential clock input.
39, 40	Q15, nQ15	Output		Differential output pair. LVPECL interface levels.
41. 42	Q14, nQ14	Output		Differential output pair. LVPECL interface levels.
44, 45	Q13, nQ13	Output		Differential output pair. LVPECL interface levels.
46, 47	Q12, nQ12	Output		Differential output pair. LVPECL interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Function Table

Table 3. Clock Input Function Table

Inputs		Outputs		Input to Output Mode	Polarity
CLK	nCLK	Q[0:15]	nQ[0:15]		
0	1	LOW	HIGH	Differential to Differential	Non-Inverting
1	0	HIGH	LOW	Differential to Differential	Non-Inverting
0	Biased; NOTE 1	LOW	HIGH	Single-Ended to Differential	Non-Inverting
1	Biased; NOTE 1	HIGH	LOW	Single-Ended to Differential	Non-Inverting
Biased; NOTE 1	0	HIGH	LOW	Single-Ended to Differential	Inverting
Biased; NOTE 1	1	LOW	HIGH	Single-Ended to Differential	Inverting

NOTE 1: Refer to the Application Information section, *Wiring the Differential Input to Accept single-ended Levels.*

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O Continuous Current Surge Current	 50mA 100mA
Package Thermal Impedance, θ_{JA}	47.9°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{CC} = 3.3V ± 5%, V_{CCO} = 2.5V ± 5%, V_{EE} = 0V, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{CCO}	Output Supply Voltage		2.375	25	2.625	V
I_{EE}	Power Supply Current				150	mA

Table 4B. Differential Input DC Characteristics, V_{CC} = 3.3V ± 5%, V_{CCO} = 2.5V ± 5%, V_{EE} = 0V, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK				150	µA
		nCLK				5	µA
I_{IL}	Input Low Current	CLK		-5			µA
		nCLK		-150			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1			0.05		V_{CC} – 0.85	V

NOTE 1: Common mode input voltage is defined as V_{IH}.

Table 4C. LVPECL DC Characteristics, V_{CC} = 3.3V ± 5%, V_{CCO} = 2.5V ± 5%, V_{EE} = 0V, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CCO} – 1.1		V_{CCO} – 0.7	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CCO} – 2.0		V_{CCO} – 1.4	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.55		0.93	V

NOTE 1: Outputs terminated with 50Ω to V_{CCO} – 2V.

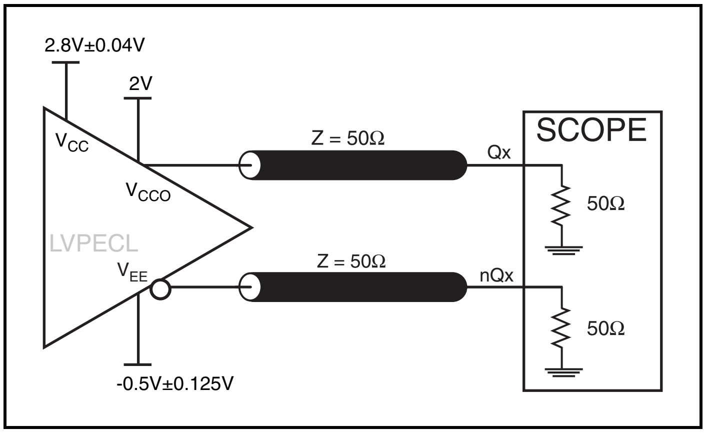
AC Electrical Characteristics

Table 5. AC Electrical Characteristics, V_{CC} = 3.3V ± 5%, V_{CCO} = 2.5V ± 5%, V_{EE} = 0V, T_A = 0°C to 70°C

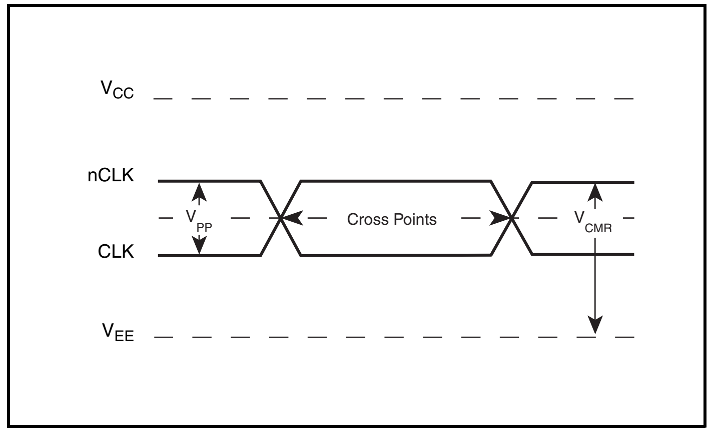
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				500	MHz
t_{PD}	Propagation Delay; NOTE 1	$f \leq$ 500MHz	1		2	ns
*t*sk(o)	Output Skew; NOTE 2, 3			26	50	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 4				250	ps
t_R / t_F	Output Rise/ Fall Time	20% to 80% @ 50MHz	300		700	ps
odc	Output Duty Cycle		47	50	53	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. Device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE All parameters measured at 250MHz unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

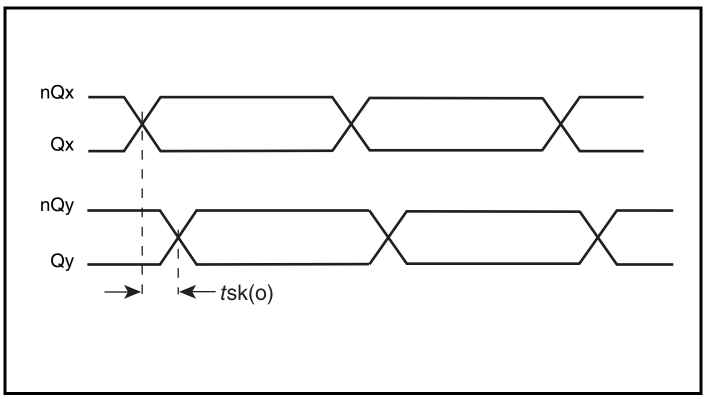
Parameter Measurement Information



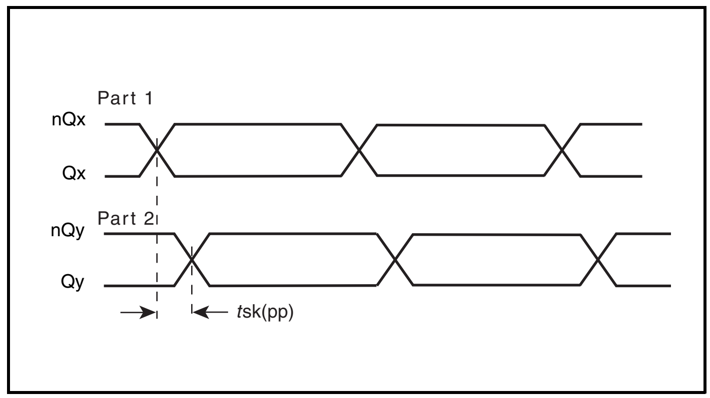
3.3V Core/ 2.5V LVPECL Output Load AC Test Circuit



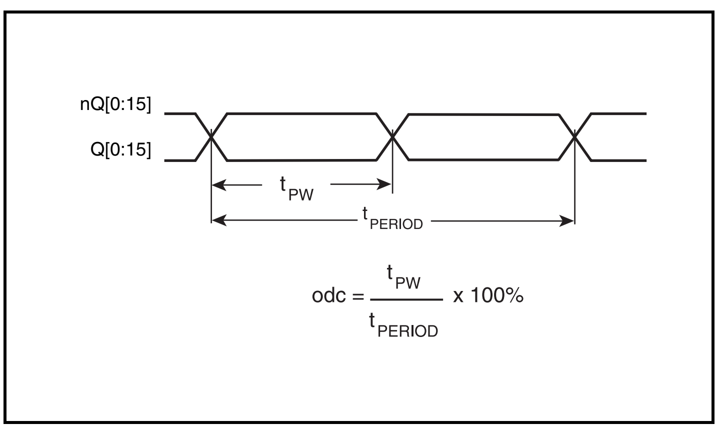
Differential Input Level



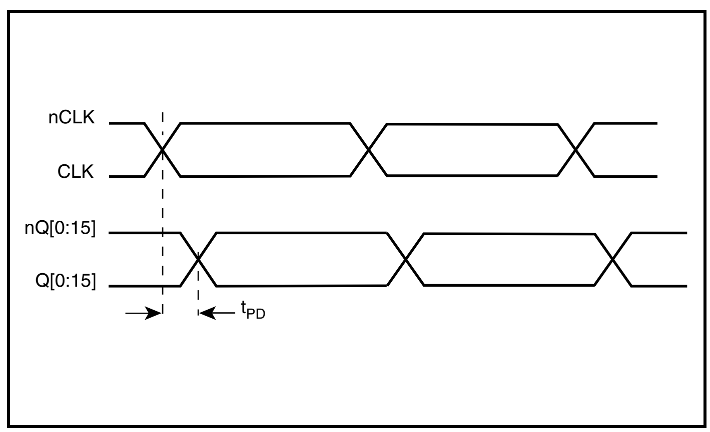
Output Skew



Part-to-Part Skew

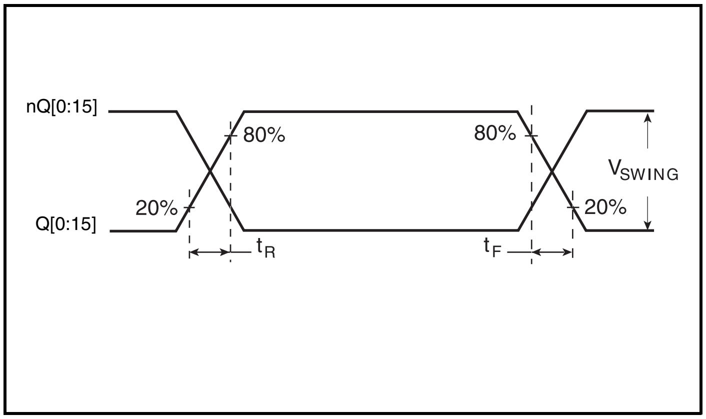


Output Duty Cycle/Pulse Width/Period



Propagation Delay

Parameter Measurement Information, continued



Output Rise/Fall Time

Applications Information

Recommendations for Unused Output Pins

Outputs:

LVPECL Outputs
The unused LVPECL output pair can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{CC}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{CC} = 3.3V, R1 and R2 value should be adjusted to set V_{REF} at 1.25V. The values below are for when both the single ended swing and V_{CC} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{CC} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

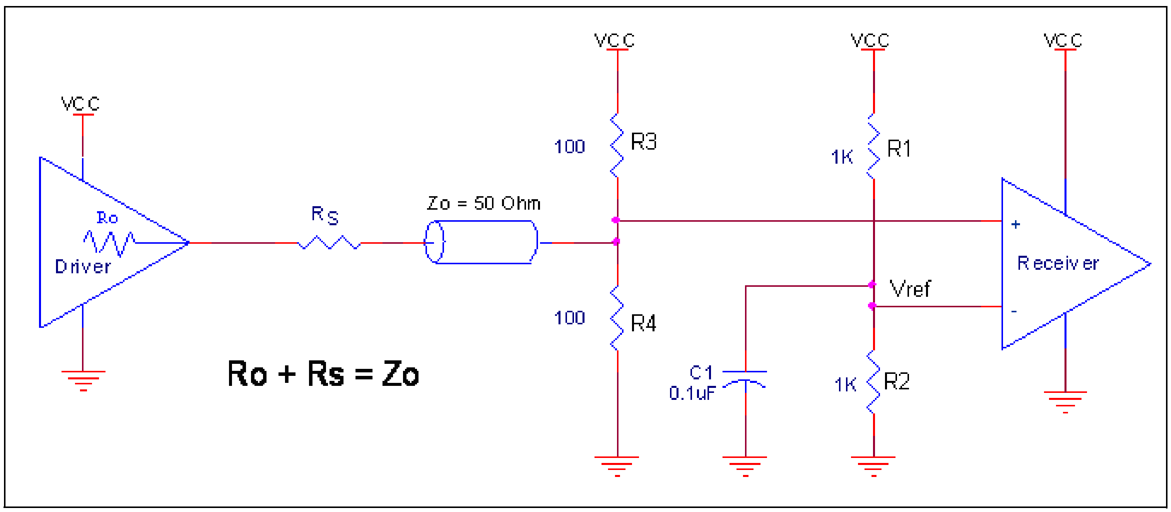


Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 2A to 2F show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 2A,* the input termination applies for IDT LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

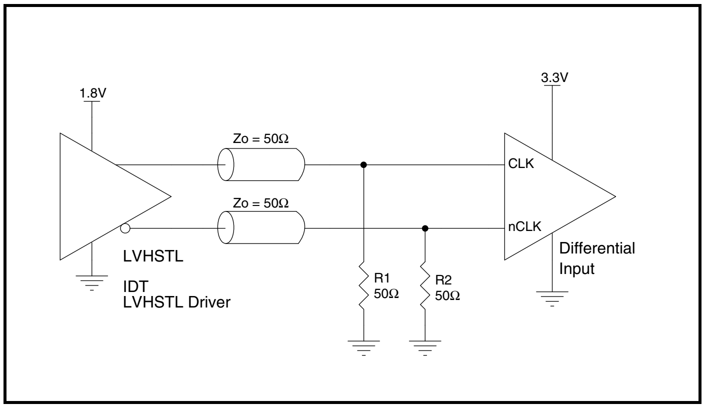


Figure 2A. CLK/nCLK Input Driven by an IDT LVHSTL Driver

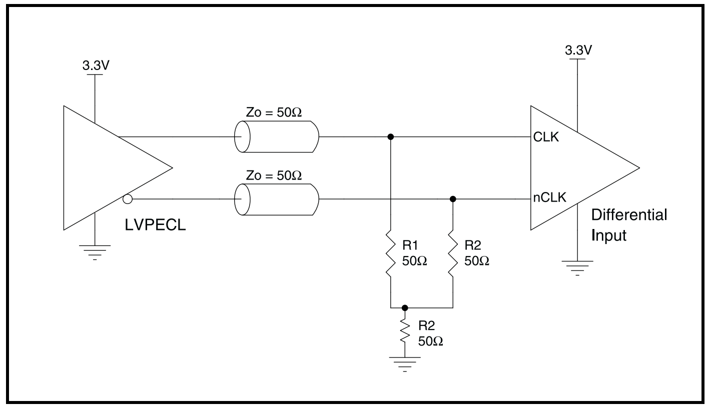


Figure 2B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

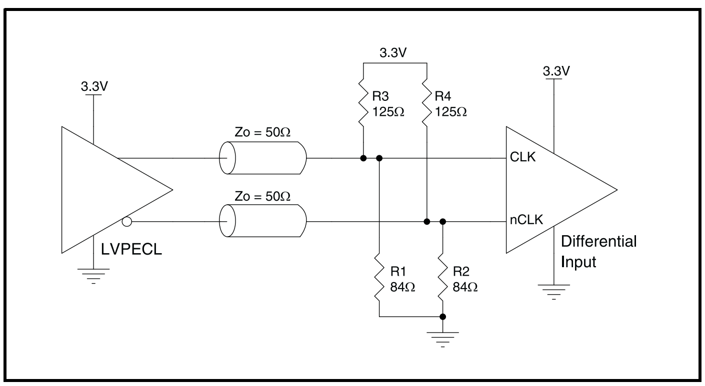


Figure 2C. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

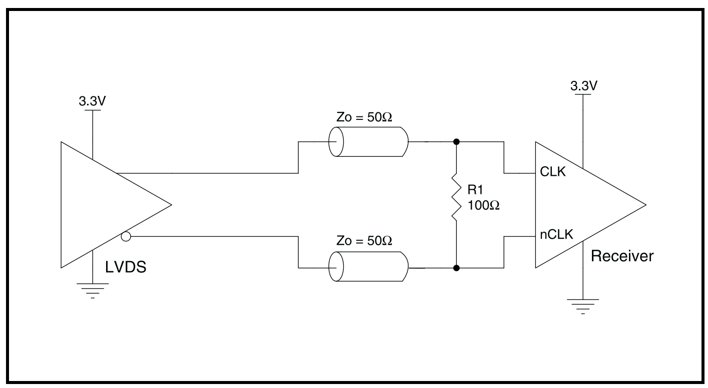


Figure 2D. CLK/nCLK Input Driven by a 3.3V LVDS Driver

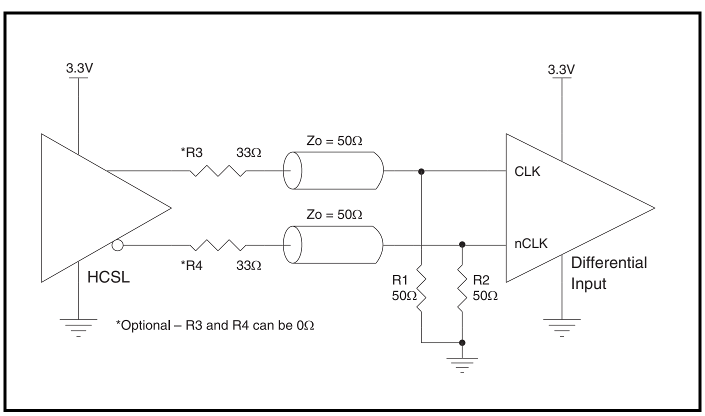


Figure 2E. CLK/nCLK Input Driven by a 3.3V HCSL Driver

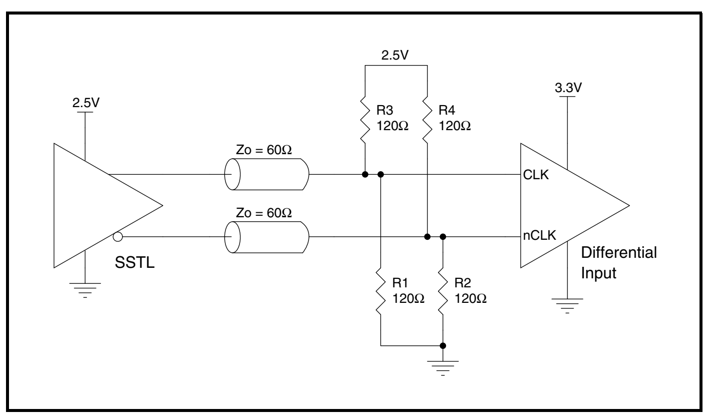


Figure 2F. CLK/nCLK Input Driven by a 2.5V SSTL Driver

Termination for 2.5V LVPECL Outputs

Figure 3A and *Figure 3B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CCO} – 2V. For V_{CCO} = 2.5V, the V_{CCO} – 2V is very close to ground level. The R3 in Figure 3B can be eliminated and the termination is shown in *Figure 3C.*

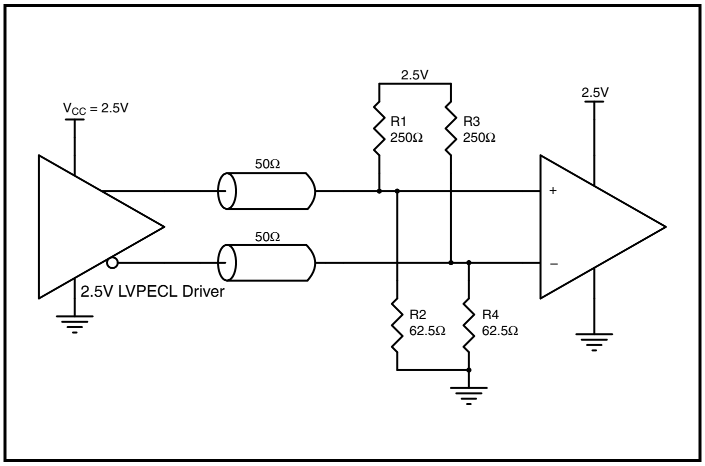


Figure 3A. 2.5V LVPECL Driver Termination Example

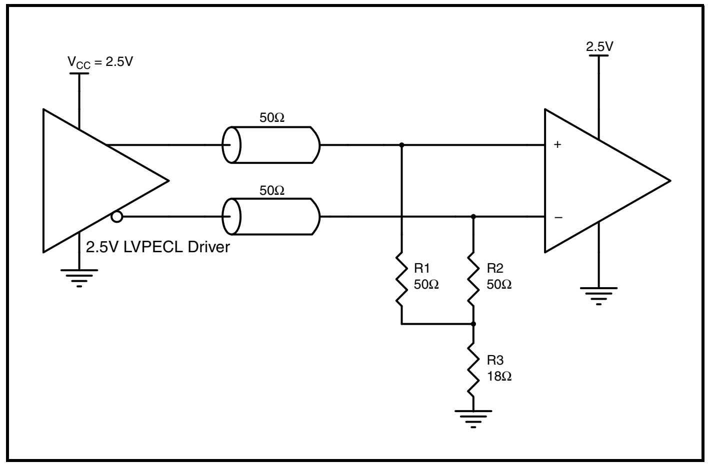


Figure 3B. 2.5V LVPECL Driver Termination Example

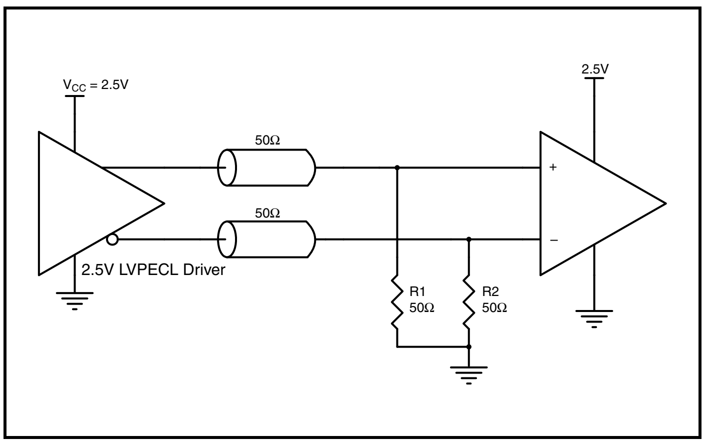


Figure 3C. 2.5V LVPECL Driver Termination Example

Power Considerations

This section provides information on power dissipation and junction temperature for the 8530.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 8530 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 150mA = **519.75mW**
- Power (outputs)$_{MAX}$ = **35mW/Loaded Output pair**
  If all outputs are loaded, the total power is 16 * 35mW = **560mW**

Total Power$_{\_MAX}$ (3.465V, with all outputs switching) = 519.75mW + 560mW = **1079.75mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and it directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 47.9°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 1.080W * 47.9°C/W = 121.7°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 48 Lead LQFP, Forced Convection

θ_{JA} by Velocity			
Linear Feet per Minute	**0**	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W
NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.			

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pairs.

LVPECL output driver circuit and termination are shown in *Figure 4.*

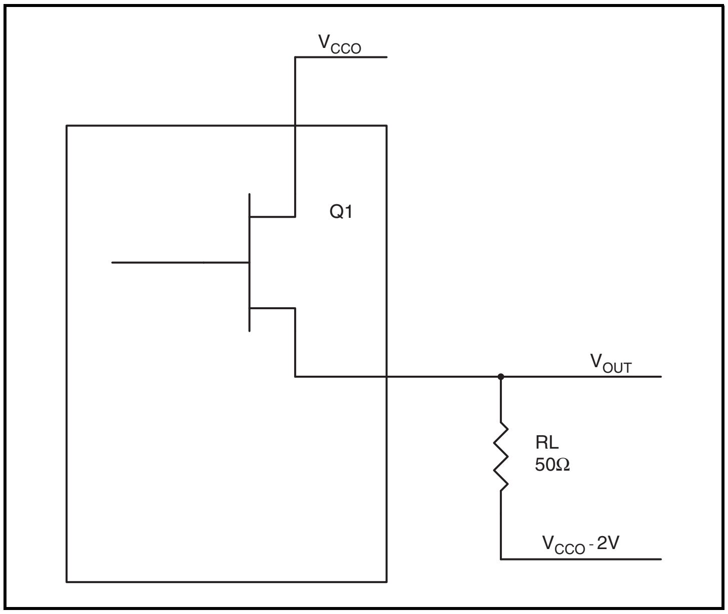


Figure 4. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CCO} – 2V$.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CCO\_MAX} – 0.7V}$
  $(V_{CCO\_MAX} – V_{OH\_MAX}) = \mathbf{0.7V}$
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CCO\_MAX} – 1.4V}$
  $(V_{CCO\_MAX} – V_{OL\_MAX}) = \mathbf{1.4V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CCO\_MAX} – 2V))/R_L] * (V_{CCO\_MAX} – V_{OH\_MAX}) = [(2V – (V_{CCO\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} – V_{OH\_MAX}) = [(2V – 0.7V)/50\Omega] * 0.7V = \mathbf{18.2mW}$

$Pd\_L = [(V_{OL\_MAX} – (V_{CCO\_MAX} – 2V))/R_L] * (V_{COC\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CCO\_MAX} – V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} – V_{OL\_MAX}) = [(2V – 1.4V)/50\Omega] * 1.4V = \mathbf{16.8mW}$

Total Power Dissipation per output pair = Pd_H + Pd_L = **35mW**

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 48 Lead LQFP

θ_{JA} vs. Air Flow			
Linear Feet per Minute	**0**	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W
NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.			

Transistor Count

The transistor count for 8530 is: 930

Package Outline and Package Dimensions

Package Outline - Y Suffix for 48 Lead LQFP

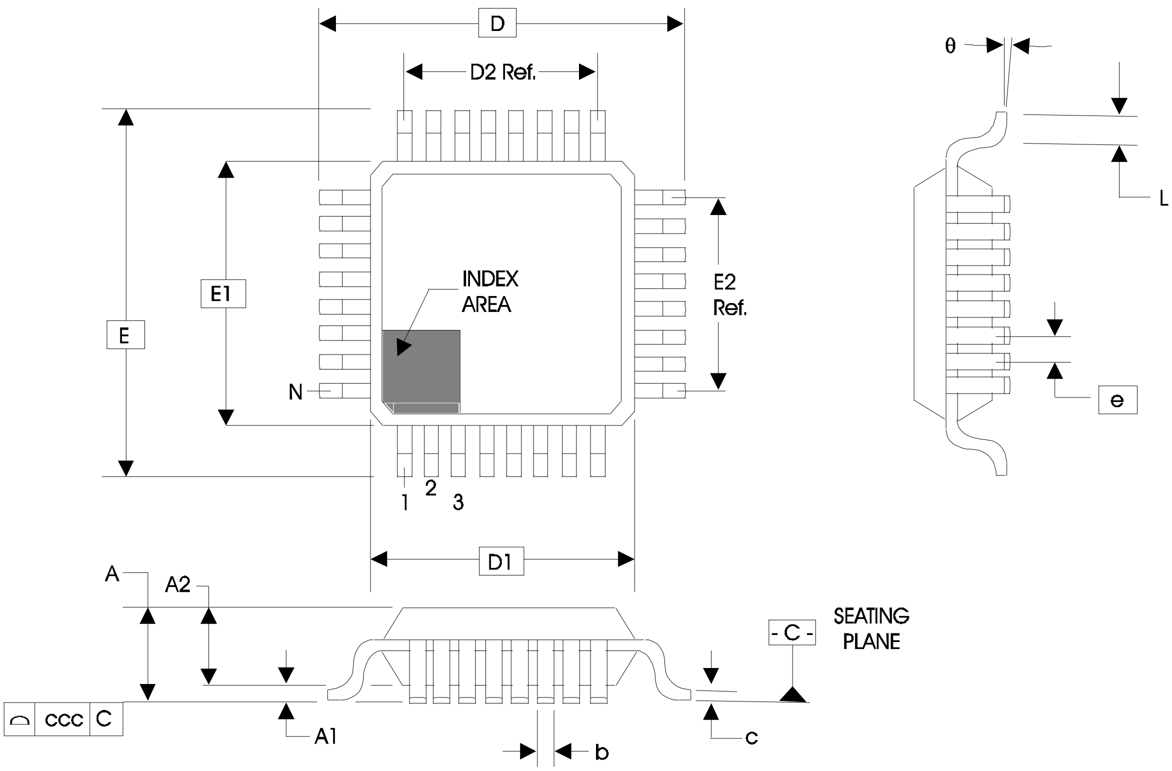


Table 8. Package Dimensions for 48 Lead LQFP

JEDEC Variation: BCB - HD All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		48	
A			1.60
A1	0.05	0.10	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09		0.20
D & E		9.00 Basic	
D1 & E1		7.00 Basic	
D2 & E2		5.50 Ref.	
e		0.5 Basic	
L	0.45	0.60	0.75
θ	0°		7°
ccc			0.08

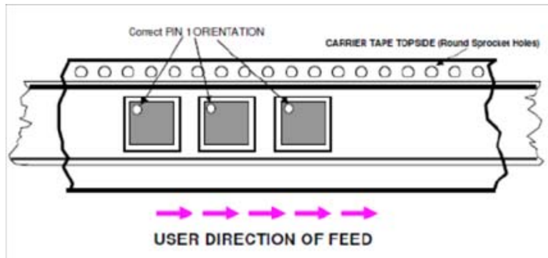
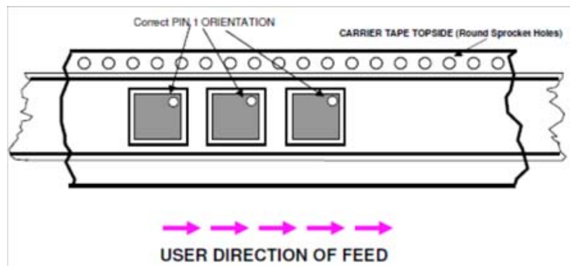
Reference Document: JEDEC Publication 95, MS-026

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8530DYLF	ICS8530DYLF	Lead-Free, 48 Lead LQFP	Tray	0°C to 70°C
8530DYLFT	ICS8530DYLF	Lead-Free, 48 Lead LQFP	2500 Tape & Reel, pin 1 orientation: EIA-481-C	0°C to 70°C
8530DYLF/W	ICS8530DYLF	Lead-Free, 48 Lead LQFP	2500 Tape & Reel, pin 1 orientation EIA-481-D	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Table 10. Pin 1 Orientation in Tape and Reel Packaging

Part Number Suffix	Pin 1 Orientation	Illustration
8	Quadrant 1 (EIA-481-C)	
/W	Quadrant 2 (EIA-481-D)	

Revision History Sheet

Rev	Table	Page	Description of Change	Date
C		5-6 7	Updated figures. Added Termination for LVPECL Outputs section.	5/28/02
C		5	Output Load Test Circuit - corrected VEE equation to read: ""V_{EE} = -0.5V ± 0.165V"" from ""V_{EE} = -0.5V ± 0.135V"".	10/2/02
D	T2 T4C	2 3 5 6 6 7 8-9	Pin Characteristics - changed C_{IN} 4pF max. to 4pF typical. LVPECL Characteristics - changed V_{OH} from V_{CCO} - 1.4V min. to V_{CCO} - 1.1V min. Changed V_{CCO} - 1.0V max. to V_{CCO} - 0.7V max. Changed V_{OL} from V_{CCO} - 1.7V max. to V_{CCO} - 1.4V max. Output Load Test Circuit - corrected V_{EE} equation to read: ""V_{EE} = -0.5V ± 0.125V"" from ""V_{EE} = -0.5V ± 0.165V"". Corrected V_{CC} equation to read ""V_{CC} = 2.8V ± 0.04V"" from ""V_{CC} = 2.8V"". Updated Figure 1, Single Ended Signal Driving Differential Input diagram. Updated Figures 2A and 2B, LVPECL Output Termination diagrams. Added Differential Clock Input Interface section. Adjusted worse case power dissipation to reflect V_{OH}/V_{OL}. Updated format throughout datasheet.	11/20/03
E	T4A	3	Power Supply Table - changed I_{EE} max. from 115mA to 125mA.	12/2/03
E	T4B T9	4 6 7 9 14	Differential DC Characteristics Table - updated notes. Added *Recommendations for Unused Output Pins section.* Updated *Wiring the Differential Input to Accept Single-ended Levels section.* Updated *Termination for LVPECL Outputs section.* Ordering Information Table - deleted “ICS” prefix from part/order column. Added lead-free marking. Converted datasheet format.	9/15/10
F	T4A	3 10	Power Supply DC Characteristics Table - changed I_{EE} spec to 150mA maximum. Power Considerations, updated calculations to coincide with new I_{EE} spec.	10/11/11
G	T10	14	Added Pin 1 Orientation in Tape and Reel Packaging Table.	6/26/15

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