8:1 Differential-to-3.3V or 2.5V LVPECL/ECL Clock Multiplexer

853S058

DATA SHEET

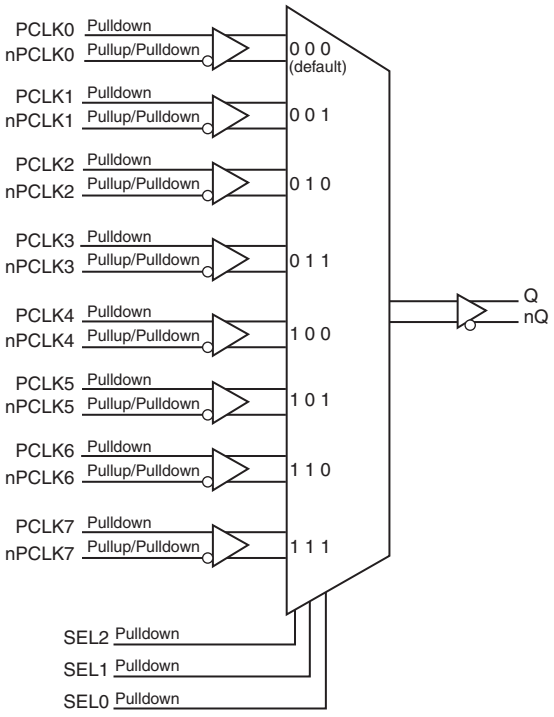
General Description

The 853S058 is an 8:1 Differential-to-3.3V or 2.5V LVPECL / ECL Clock Multiplexer which can operate up to 2.5 GHz. The 853S058 has 8 differential selectable clock inputs. The PCLK, nPCLK input pairs can accept LVPECL, LVDS, SSTL or CML levels. The fully differential architecture and low propagation delay make it ideal for use in clock distribution circuits. The select pins have internal pulldown resistors. The SEL2 pin is the most significant bit and the binary number applied to the select pins will select the same numbered data input (i.e., 000 selects PCLK0, nPCLK0).

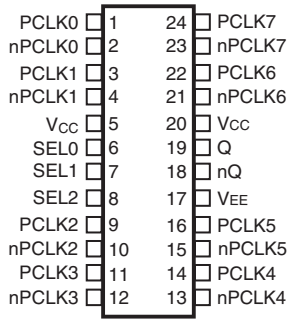
Features

- High speed 8:1 differential muliplexer
- One differential 3.3V or 2.5V LVPECL output pair
- Eight selectable differential PCLKx, nPCLKx input pairs
- Differential PCLKx, nPCLKx pairs can accept the following interface levels: LVPECL, LVDS, SSTL,CML
- Maximum output frequency: 2.5GHz
- Translates any single ended input signal to LVPECL levels with resistor bias on nPCLKx input
- Additive phase jitter, RMS: 0.075ps (typical)
- Part-to-part skew: 350ps (maximum)
- Propagation delay: 600ps (maximum)
- LVPECL mode operating voltage supply range: V_{CC} = 2.375V to 3.465V, V_{EE} = 0V
- ECL mode operating voltage supply range: V_{CC} = 0V, V_{EE} = -3.465V to -2.375V
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Block Diagram



Pin Assignment



853S058

24-Lead TSSOP, 173-MIL
4.4mm x 7.8mm x 0.925mm
package body
G Package
Top View

Pin Descriptions and Pin Characteristics Tables

Table 1. Pin Descriptions

Number	Name	Type		Description
1	PCLK0	Input	Pulldown	Non-inverting differential clock input.
2	nPCLK0	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{CC}/2$ default when left floating.
3	PCLK1	Input	Pulldown	Non-inverting differential clock input.
4	nPCLK1	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{CC}/2$ default when left floating.
5, 20	V_{CC}	Power		Positive supply pins.
6, 7, 8	SEL0, SEL1, SEL2	Input	Pulldown	Clock select input pins. LVCMOS/LVTTL interface levels.
9	PCLK2	Input	Pulldown	Non-inverting differential clock input.
10	nPCLK2	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{CC}/2$ default when left floating.
11	PCLK3	Input	Pulldown	Non-inverting differential clock input.
12	nPCLK3	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{CC}/2$ default when left floating.
13	nPCLK4	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{CC}/2$ default when left floating.
14	PCLK4	Input	Pulldown	Non-inverting differential clock input.
15	nPCLK5	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{CC}/2$ default when left floating.
16	PCLK5	Input	Pulldown	Non-inverting differential clock input.
17	V_{EE}	Power		Negative supply pin.
18, 19	nQ, Q	Output		Differential output pair. LVPECL interface levels.
21	nPCLK6	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{CC}/2$ default when left floating.
22	PCLK6	Input	Pulldown	Non-inverting differential clock input.
23	nPCLK7	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{CC}/2$ default when left floating.
24	PCLK7	Input	Pulldown	Non-inverting differential clock input.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			2		pF
$R_{PULLDOWN}$	Pulldown Resistor			75		kΩ
$R_{VCC}/2$	RPullup/Pulldown Resistor			50		kΩ

Function Tables

Table 3. Control Input Function Table

Inputs			Outputs	
SEL2	**SEL1**	**SEL0**	**Q**	**nQ**
0 (default)	0	0	PCLK0	nPCLK0
0	0	1	PCLK1	nPCLK1
0	1	0	PCLK2	nPCLK2
0	1	1	PCLK3	nPCLK3
1	0	0	PCLK4	nPCLK4
1	0	1	PCLK5	nPCLK5
1	1	0	PCLK6	nPCLK6
1	1	1	PCLK7	nPCLK7

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	**Rating**
Supply Voltage, V_{CC}	4.6V (LVPECL mode, V_{EE} = 0V)
Negative Supply Voltage, V_{EE}	-4.6V (ECL mode, V_{CC} = 0V)
Inputs, V_I (LVPECL mode)	-0.5V to V_{CC} + 0.5V
Inputs, V_I (ECL mode)	0.5V to V_{EE} – 0.5V
Outputs, I_O Continuous Current Surge Current	 50mA 100mA
Operating Temperature Range, T_A	-40°C to +85°C
Package Thermal Impedance, θ_{JA}	85.1°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{CC} = 2.375V to 3.465V; V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	**Parameter**	**Test Conditions**	**Minimum**	**Typical**	**Maximum**	**Units**
V_{CC}	Positive Supply Voltage		2.375	3.3	3.465	V
I_{EE}	Power Supply Current				55	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{CC} = 2.375V to 3.465V; V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{CC} = 3.3V	2.2		V_{CC} + 0.3	V
			V_{CC} = 2.5V	1.7		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		V_{CC} = 3.3V	-0.3		0.8	V
			V_{CC} = 2.5V	-0.3		0.7	V
I_{IH}	Input High Current	SEL[0:2]	V_{CC} = V_{IN} = 3.465V or 2.625V			150	µA
I_{IL}	Input Low Current	SEL[0:2]	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-10			µA

Table 4C. LVPECL DC Characteristics, V_{CC} = 2.375V to 3.465V; V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	PCLK[0:7], nPCLK[0:7]	V_{CC} = V_{IN} = 3.465V or 2.625V			150	µA
I_{IL}	Input Low Current	PCLK[0:7]	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-10			µA
		nPCLK[0:7]	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage; NOTE 1			0.15		1.2	V
V_{CMR}	Common Mode Range; NOTE 1, 2			1.2		V_{CC}	V
V_{OH}	Output High Voltage; NOTE 3			V_{CC} – 1.125		V_{CC} – 0.875	V
V_{OL}	Output Low Voltage; NOTE 3			V_{CC} – 1.895		V_{CC} – 1.62	V
V_{SWING}	Peak-to-Peak Output Voltage Swing			0.6		1.0	V

NOTE 1: V_{IL} should not be less than V_{EE} – 0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.
NOTE 3: Outputs terminated with 50Ω to V_{CC} – 2V.

Table 4D. ECL DC Characteristics, V_{CC} = 0V, V_{EE} = -3.465V to -2.375V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1			-1.225		-0.935	V
V_{OL}	Output Low Voltage; NOTE 1			-1.895		-1.67	V
V_{PP}	Peak-to-Peak Input Voltage; NOTE 2			0.15		1.2	V
V_{CMR}	Input High Voltage Common Mode Range; NOTE 2, 3			V_{EE} + 1.2		V_{CC}	V
I_{IH}	Input High Current	PCLK[0:7], nPCLK[0:7]	V_{CC} = V_{IN} = 3.465V or 2.625V			150	µA
I_{IL}	Input Low Current	PCLK[0:7]	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-10			µA
		nPCLK[0:7]		-150			µA

NOTE 1: Outputs terminated with 50Ω to V_{CC} – 2V.
NOTE 2: V_{IL} should not be less than V_{EE} – 0.3V.
NOTE 3: Common mode voltage is defined as V_{IH}.

AC Electrical Characteristics

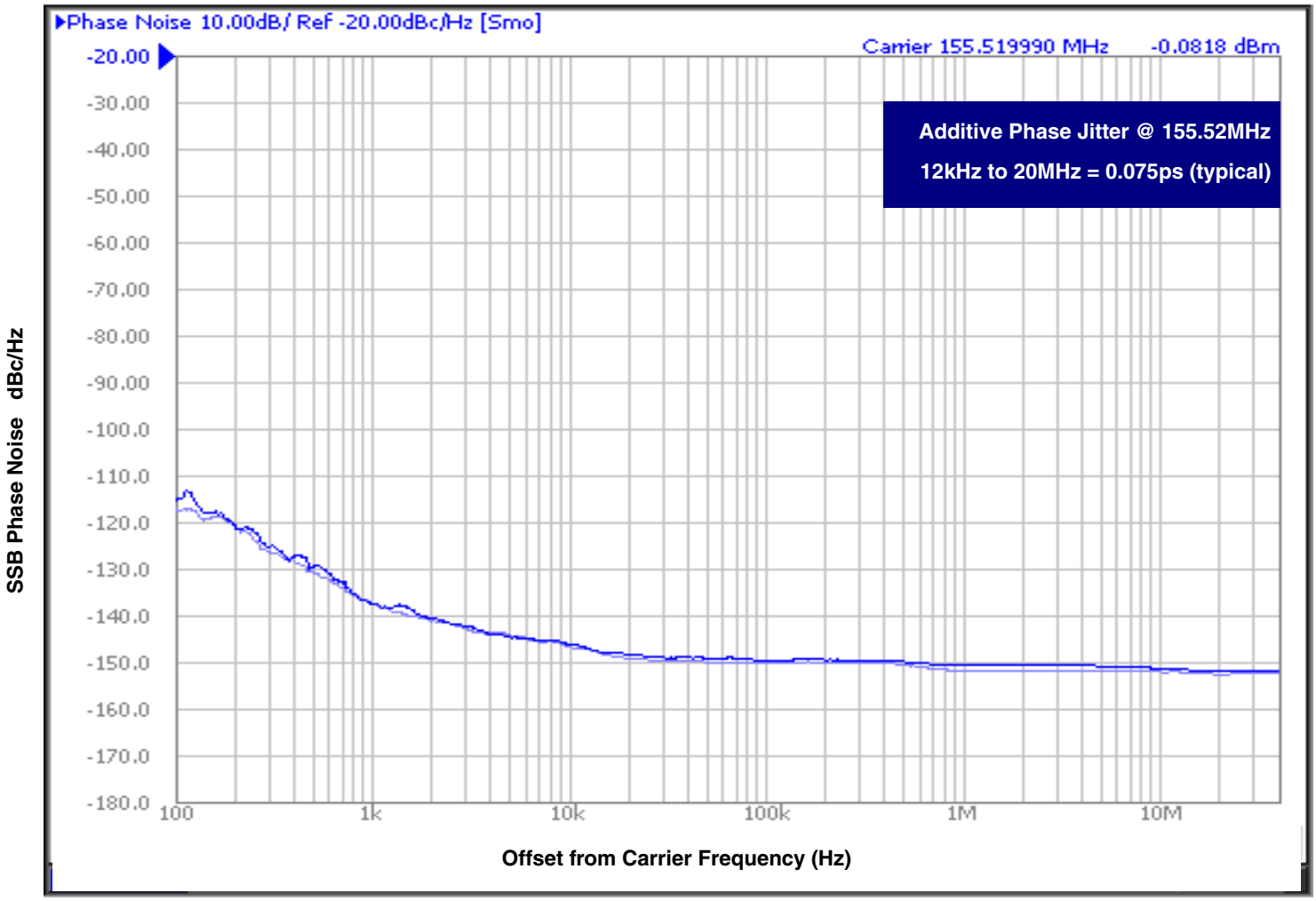
Table 5. AC Characteristics, V_{CC} = 0V, V_{EE} = -3.465V to -2.375V or V_{CC} = 2.375 to 3.465V, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency				2.5	GHz
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section	155.52MHz, Integration Range: 12kHz – 20MHz		0.075		ps
t_{PD}	Propagation Delay; NOTE 1		250		600	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 3				350	ps
*t*sk(i)	Input Skew				75	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	75		250	ps
$MUX_{ISOLATION}$	MUX Isolation; NOTE 4	155.52MHz, Input Peak-to-Peak = 800mV		90		dB

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: All parameters measured ≤ 1.0GHz, unless otherwise noted.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltage and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 3: This parameter is defined according with JEDEC Standard 65.
NOTE 4: Q, nQ output measured differentially. See *Parameter Measurement Information* for MUX Isolation diagram.

Additive Phase Jitter

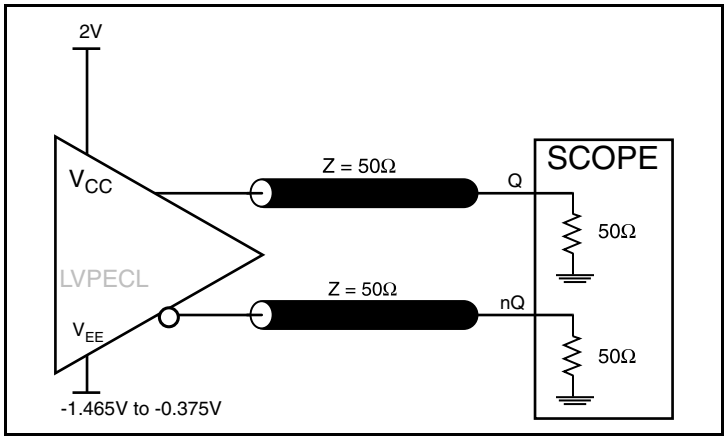
The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



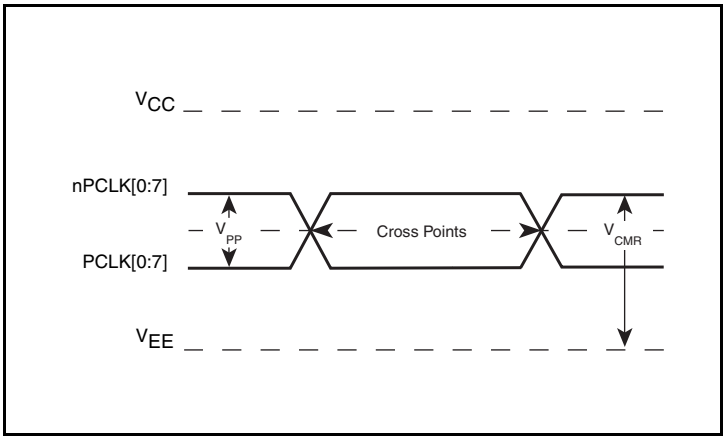
As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

The source generator "Rohde & Schwarz SMA100A Signal Generator 9kHz - 6GHz as external input to an Agilent 8133A 3GHz Pulse Generator".

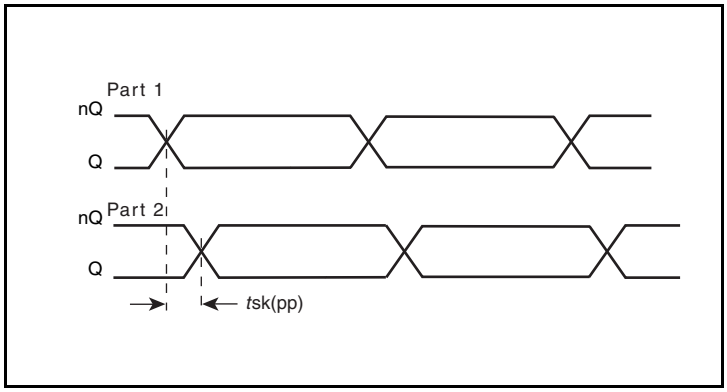
Parameter Measurement Information



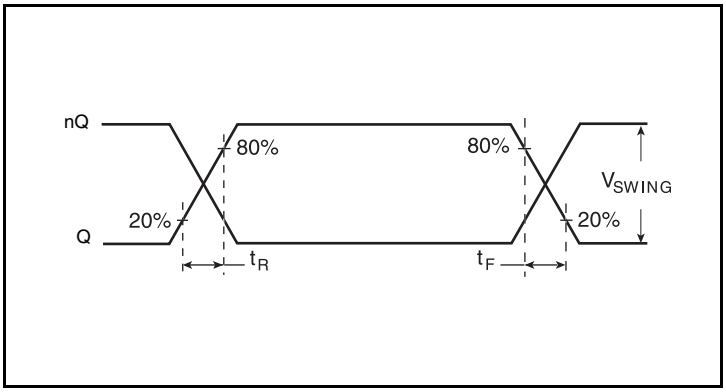
LVPECL Output Load AC Test Circuit



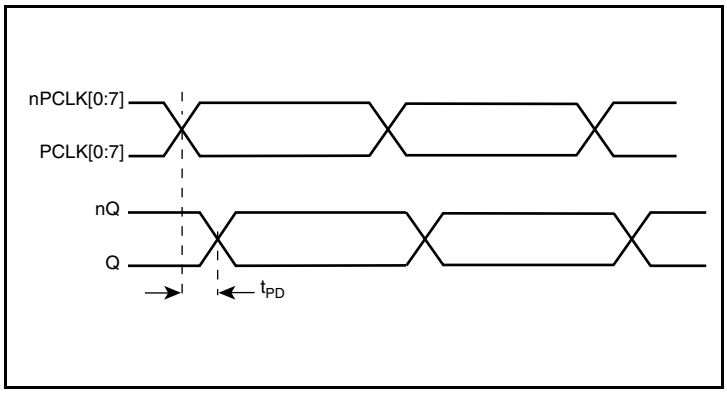
Differential Input Level



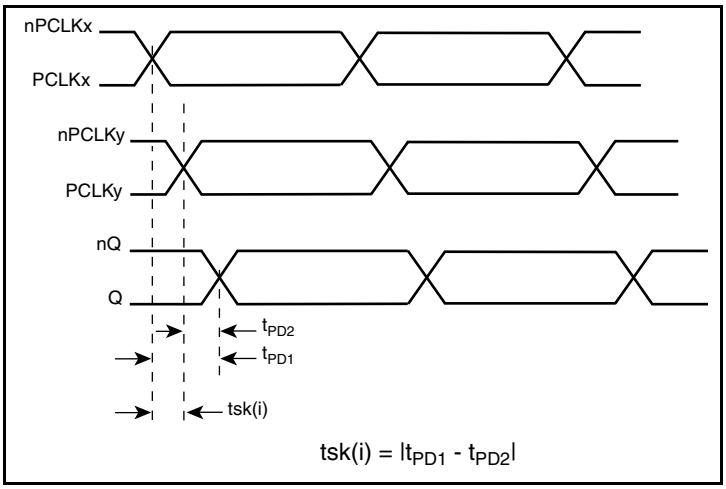
Part-to-Part Skew



Output Rise/Fall Time

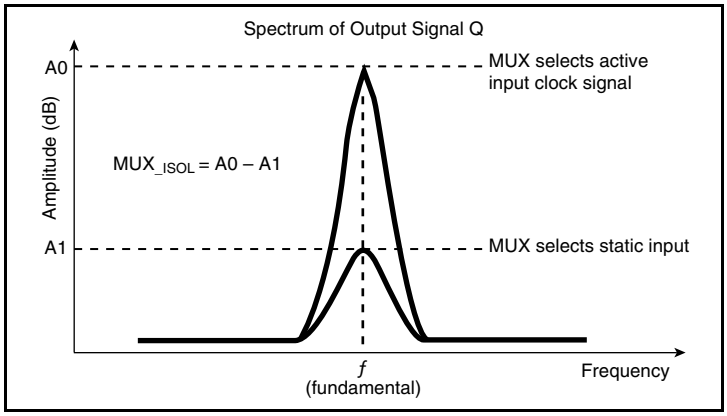


Propagation Delay



Input Skew

Parameter Measurement Information, continued



MUX Isolation

Applications Information

Recommendations for Unused Input Pins

Inputs:

PCLK/nPCLK Inputs

For applications not requiring the use of the differential input, both PCLK and nPCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

LVCMOS Control Pins

All control pins have internal pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{DD}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{DD} = 3.3V, R1 and R2 value should be adjusted to set V_{REF} at 1.25V. The values below are for when both the single ended swing and V_{DD} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{DD} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

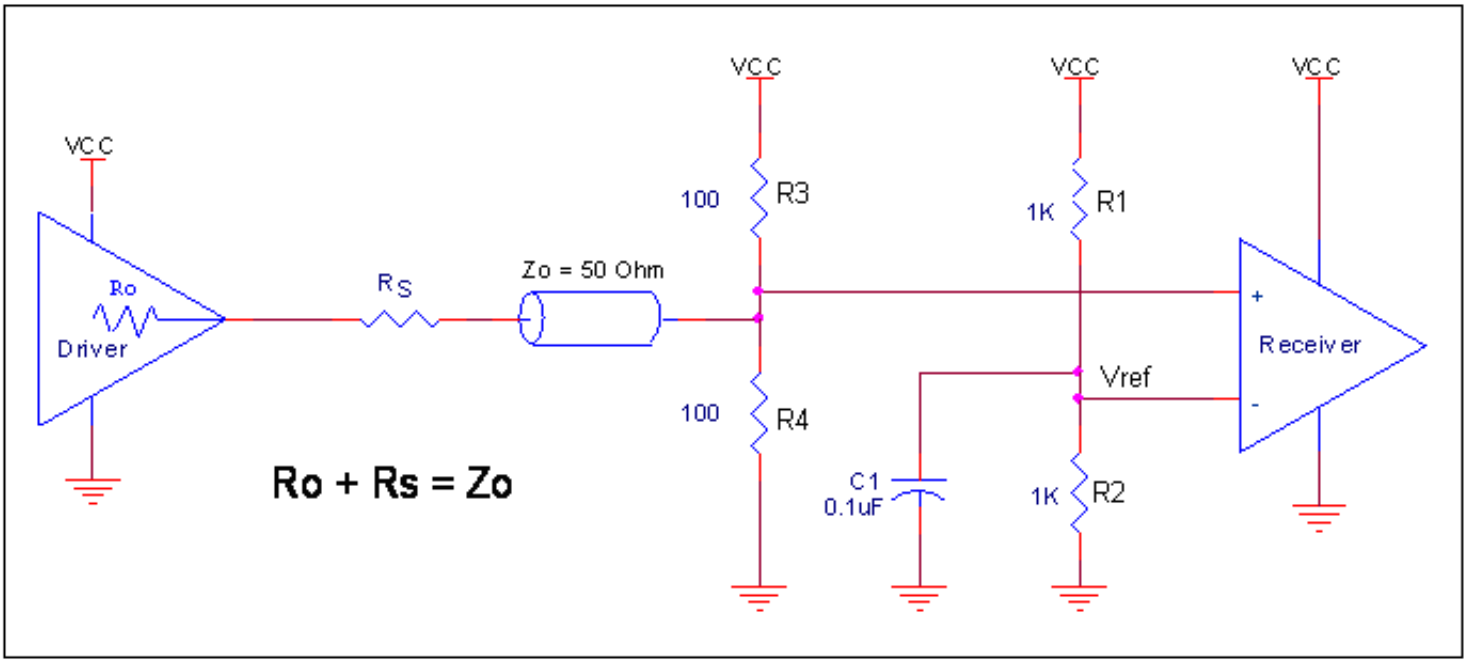


Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

LVPECL Clock Input Interface

The PCLK /nPCLK accepts LVPECL, LVDS, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2E* show interface examples for the PCLK/nPCLK input driven by the most common driver types.

The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

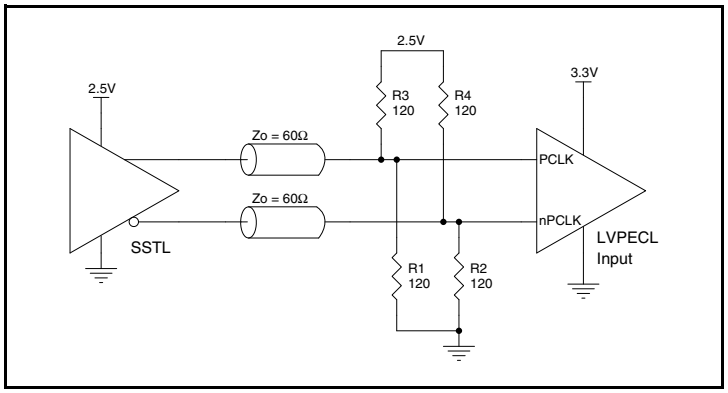


Figure 2A. PCLK/nPCLK Input Driven by an SSTL Driver

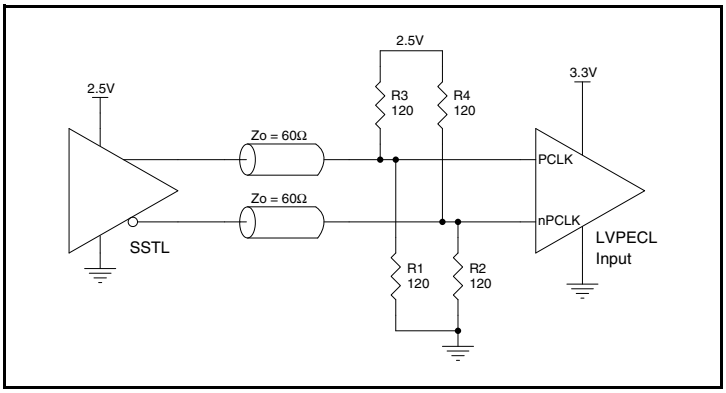


Figure 2B. PCLK/nPCLK Input Driven by a 3.3V LVDS Driver

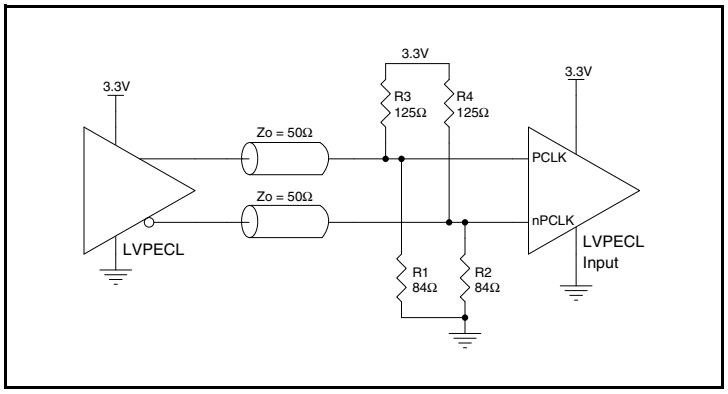


Figure 2C. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver

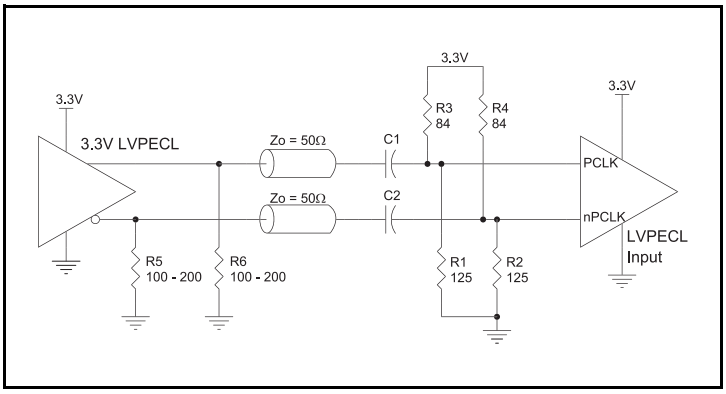


Figure 2D. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Couple

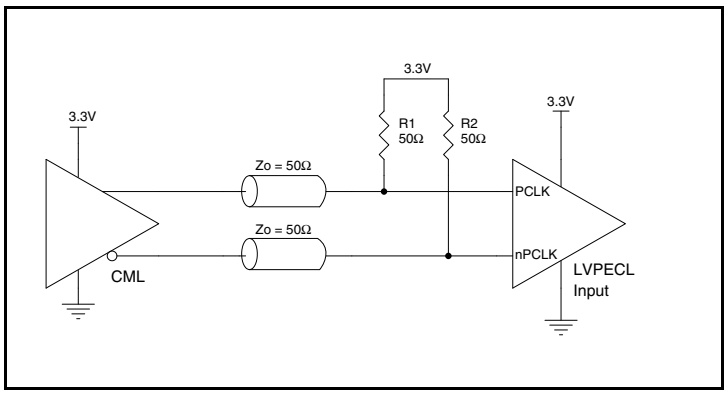


Figure 2E. PCLK/nPCLK Input Driven by a CML Driver

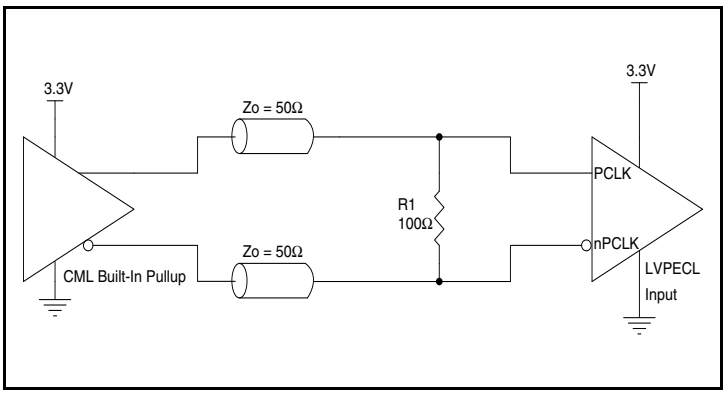


Figure 3F. PCLK/nPCLK Input Driven by a Built-In Pullup CML Driver

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 3A and 3B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

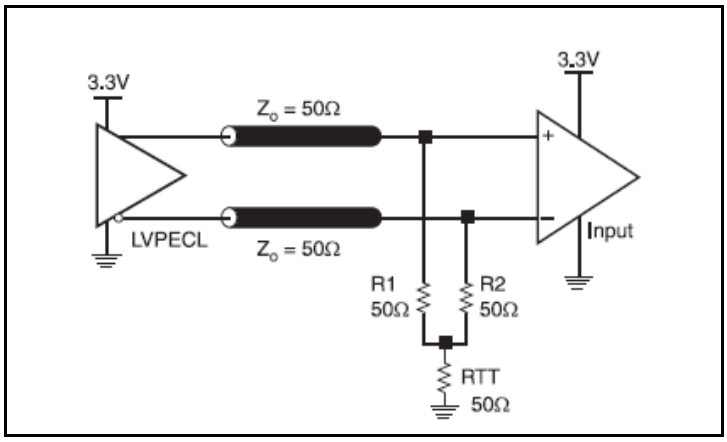


Figure 3A. 3.3V LVPECL Output Termination

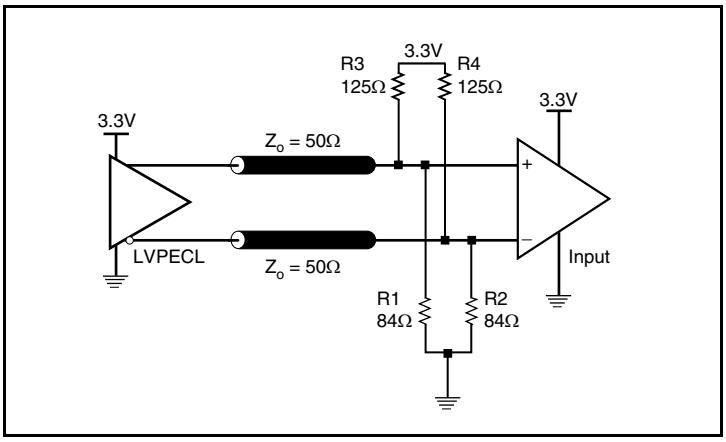


Figure 3B. 3.3V LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 4A and *Figure 4B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} – 2V. For V_{CC} = 2.5V, the V_{CC} – 2V is very close to ground level. The R3 in Figure 4B can be eliminated and the termination is shown in *Figure 4C.*

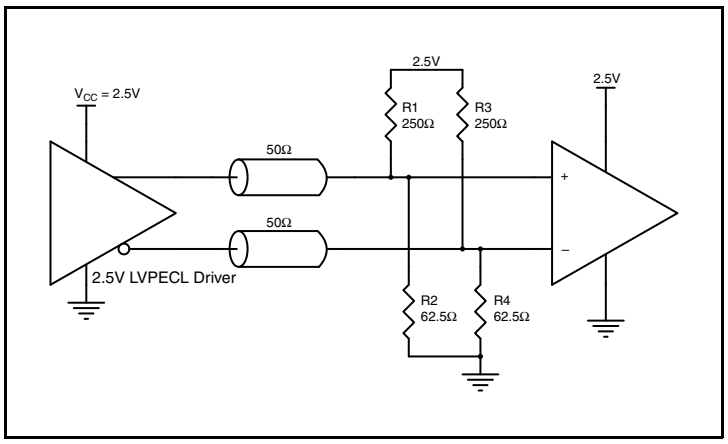


Figure 4A. 2.5V LVPECL Driver Termination Example

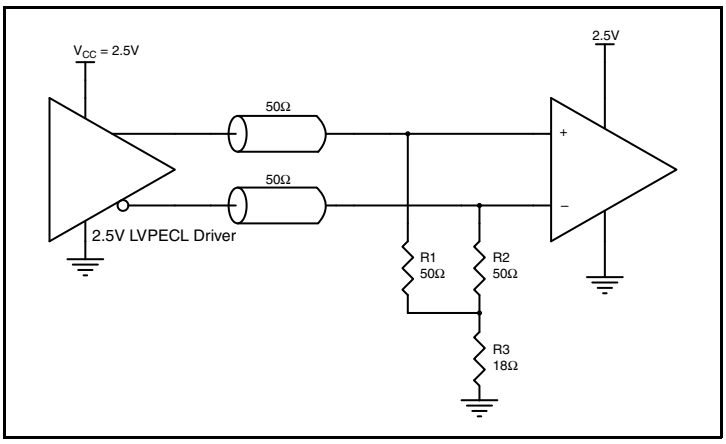


Figure 4B. 2.5V LVPECL Driver Termination Example

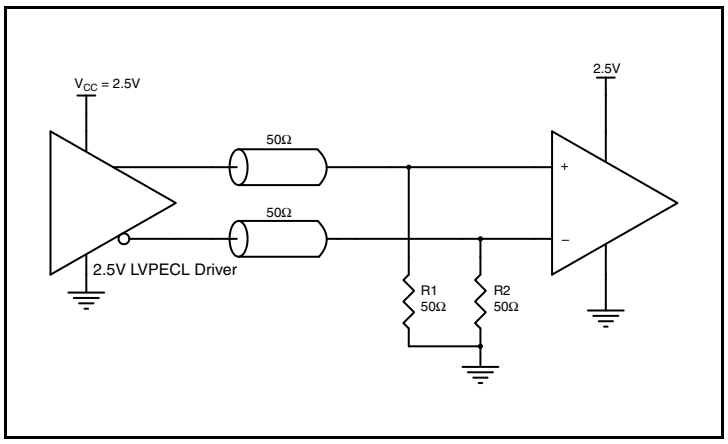


Figure 4C. 2.5V LVPECL Driver Termination Example

Schematic Example

An application schematic example of 853S058 is shown in *Figure 5*. The inputs can accept various types of differential signals. In this example, the inputs are driven by LVPECL drivers. The 853S058 output is an LVPECL driver. An example of LVPECL terminations is shown in this schematic. Other termination approaches are available in the LVPECL Termination Application Note. It is recommended at least one decoupling capacitor per power pin. The decoupling capacitor should be low ESR and located as close as possible to the power pin.

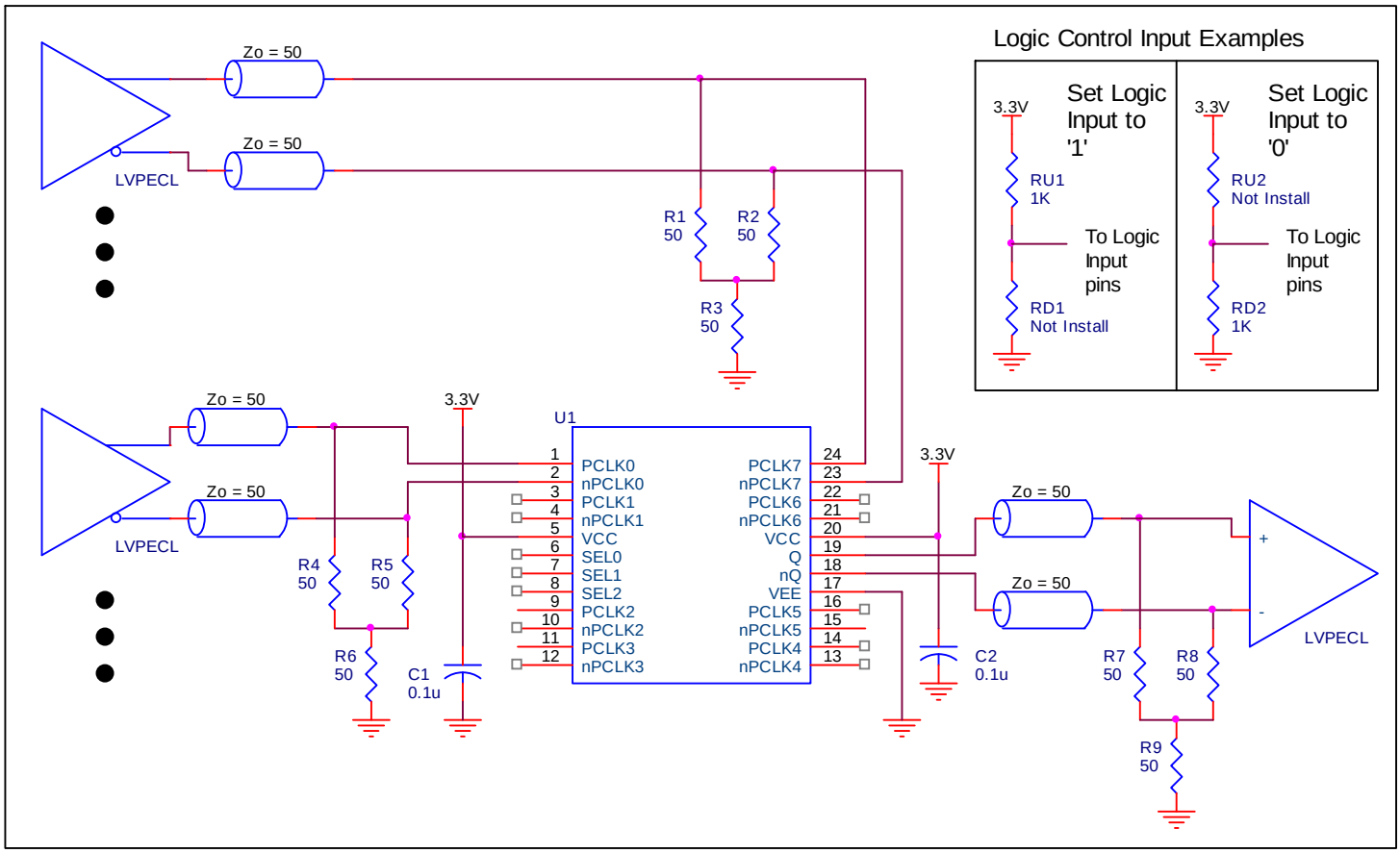


Figure 5. 853S058 Schematic Example

Power Considerations

This section provides information on power dissipation and junction temperature for the 853S058.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 853S058 is the sum of the core power plus the power dissipation into the load.
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipation into the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 55mA = **190.58mW**
- Power (outputs)$_{MAX}$ = **32mW/Loaded Output pair**

Total Power$_{\_MAX}$ (3.3V, with all outputs switching) = 190.58mW + 32mW = **222.58mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 85.1°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.223W * 85.1°C/W = 104.0°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance θ_{JA} for 24 Lead TSSOP, Forced Convection

θ_{JA} **by Velocity**			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	85.1°C/W	79.7°C/W	76.5°C/W

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair.

The LVPECL output driver circuit and termination are shown in *Figure 6.*

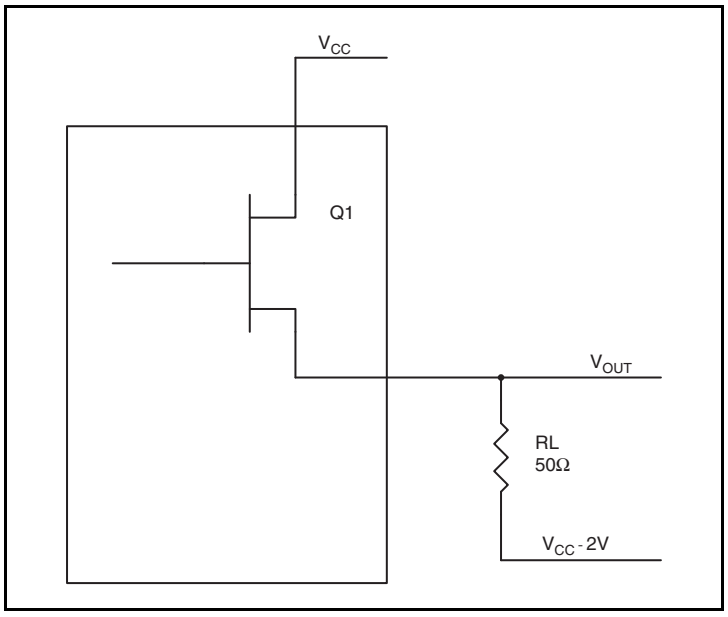


Figure 6. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} – 0.875V}$
  $(V_{CC\_MAX} – V_{OH\_MAX}) = \mathbf{0.875V}$
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} – 1.62V}$
  $(V_{CC\_MAX} – V_{OL\_MAX}) = \mathbf{1.62V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) =$
$[(2V – 0.875V)/50\Omega] * 0.875V =$ **19.69mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) =$
$[(2V – 1.62V)/50\Omega] * 1.62V =$ **12.31mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **32mW**

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for a 24 Lead TSSOP

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	85.1°C/W	79.7°C/W	76.5°C/W

Transistor Count

The transistor count for 853S058 is: 436

This is a suggested replacement for 853058

Package Outline and Package Dimensions

Package Outline - G Suffix for 24 Lead TSSOP

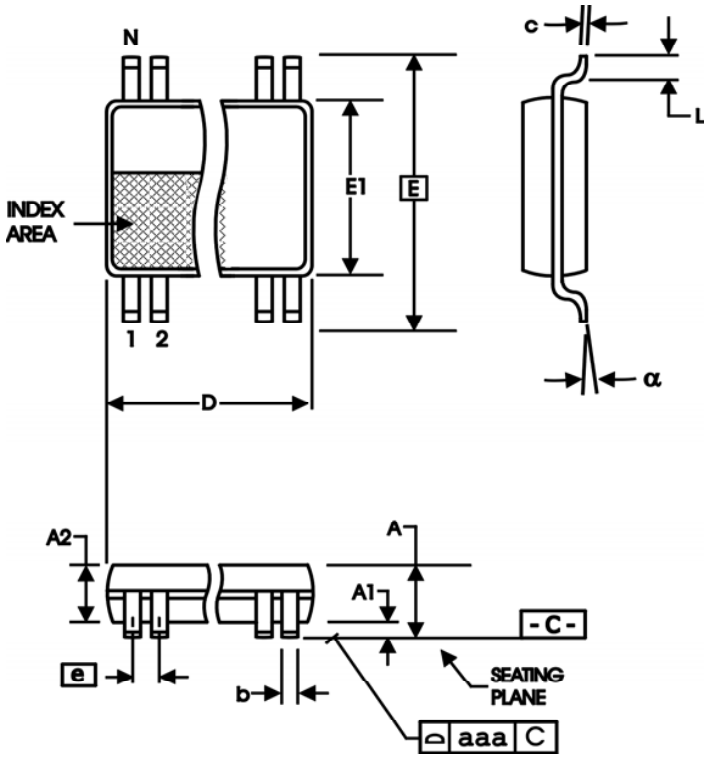


Table 9. Package Dimensions

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	24	
A		1.20
A1	0.5	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
853S058AGILF	ICS853S058AIL	24 Lead TSSOP, Lead-Free	Tube	-40°C to 85°C
853S058AGILFT	ICS853S058AIL	24 Lead TSSOP, Lead-Free	Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A		1	Deleted HiperClockS Logo. Updated GD paragraph to include CML. Added CML to 3rd bullet.	10/29/12
		9	Added figures 2E and 2F.	
	T10	16	Deleted quantity from tape and reel.	
A		1	Added PCN label: Per PCN# N1409-01, Effective Date 12/25/2014.	10/03/14
		9	Updated Application Note, *Wiring the Differential Inputs to Accept Single-ended Levels.*	
		11	Termination for 3.3V LVPECL Outputs - corrected Figure 3A.	
			Updates throughout the datasheet: - header/ footer to new format - deleted “IDT” prefix from part number.	
B	T4A	1	Removed PCN banner. PCN N1409-01 expired.	1/6/15
		3	Updated IEE spec upper limit from 51 to 55.	
		14	Power Considerations - Updated Power (core)max, Total power_max and Tj calculations.	

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