

### General Description

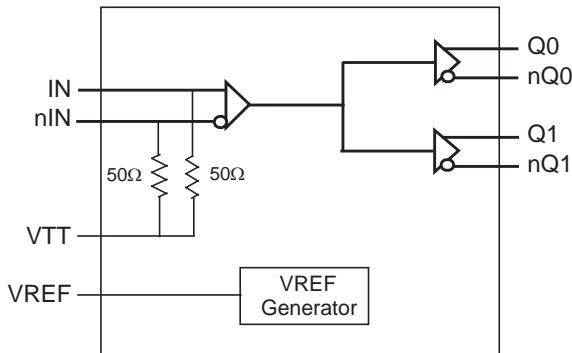
The ICS853S9252I is a 2.5V/3.3V ECL/LVPECL fanout buffer designed for high-speed, low phase-noise wireless infrastructure applications. The device fanouts a differential input signal to two ECL/LVPECL outputs. Optimized for low additive phase-noise, sub-100ps output rise and fall times, low output skew and high-frequencies, the ICS853S9252I is an effective solution for high-performance clock and data distribution applications, for instance driving the reference clock inputs of ADC/DAC circuits. Internal input termination, a bias voltage output ( $V_{REF}$ ) for AC-coupling and small packaging (3.0mm x 3.0mm 16-lead VFQFN) supports space-efficient board designs.

The ICS853S9252I operates from a full 2.5V or 3.3V power supply and supports the industrial temperature range of -40°C to 85°C. The extended temperature range also supports wireless infrastructure, tele-communication and networking end equipment requirements.

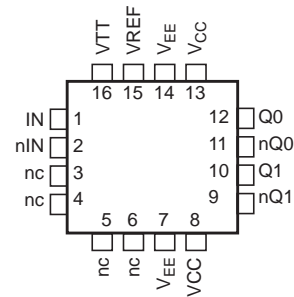
### Features

- 1:2 differential clock/data fanout buffer
- Clock frequency: 3GHz (maximum)
- Two differential 2.5V/3.3V ECL/LVPECL clock output
- Differential input accepts ECL/LVPECL, LVDS and CML levels
- Additive phase jitter, RMS @ 122.88MHz: 45fs (typical)
- Propagation delay: 175ps (maximum),  $V_{CC} = 3.3V$
- Output rise/fall time: 135ps (maximum),  $V_{CC} = 3.3V$
- Internal input signal termination
- Supply voltage: 2.5V-5% to 3.3V+10%
- Lead-free (RoHS 6) packaging
- -40°C to 85°C ambient operating temperature

### Block Diagram



### Pin Assignment



### ICS853S9252I

16 lead VFQFN  
 3.0mm x 3.0mm x 0.925mm  
 package body  
 K Package  
 Top View

## Pin Descriptions

Table 1. Pin Descriptions

Number	Name	Type	Description
1, 2	IN, nIN	Input	Non-inverting and inverting clock input. ECL/LVPECL, LVDS and CML interface levels. 50Ω to $V_{TT}$ or 100Ω input termination.
3, 4, 5, 6	nc	Unused	No connect.
7, 14	$V_{EE}$	Power	Negative supply pins.
8, 13	$V_{CC}$	Power	Power supply pins.
9, 10	nQ1, Q1	Output	Differential clock output. ECL/LVPECL interface levels.
11, 12	nQ0, Q0	Output	Differential clock output. ECL/LVPECL interface levels.
15	$V_{REF}$	Output	Bias voltage reference for AC-coupling of the differential inputs.
16	$V_{TT}$		Center tap for input termination. Leave floating for LVDS inputs, connect 50Ω to GND for 3.3V LVPECL inputs and to the $V_{REF}$ output for AC-coupled applications.

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, $V_{CC}$	4.6V (LVPECL mode, $V_{EE} = 0V$ )
Negative Supply Voltage, $V_{EE}$	-4.6V (ECL mode, $V_{CC} = 0V$ )
Inputs, $V_I$ (LVPECL mode)	-0.5V to $V_{CC} + 0.5V$
Inputs, $V_I$ (ECL mode)	0.5V to $V_{EE} - 0.5V$
Outputs, $I_O$ Continuous Current Surge Current	50mA 100mA
Input Current, IN, nIN	±25mA
$V_T$ Current, $I_{VT}$	±50mA
Input Sink/Source, $I_{REF}$	±2mA
Operating Temperature Range, $T_A$	-40°C to +85°C
Package Thermal Impedance, $\theta_{JA}$ , (Junction-to-Ambient)	74.7°C/W (0 mps)
Storage Temperature, $T_{STG}$	-65°C to 150°C

## DC Electrical Characteristics

**Table 2A. Power Supply DC Characteristics,  $V_{CC} = 2.5V-5\%$  to  $V_{CC} = 3.3V+10\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Power Supply Voltage		2.375	3.3	3.63	V
$I_{CC}$	Power Supply Current	Includes load current		79	99	mA
$I_{EE}$	Output Supply Current			26	33	mA

**Table 2B. DC Characteristics,  $V_{CC} = 2.5V-5\%$  to  $V_{CC} = 3.3V+10\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$R_{IN}$	Input Resistance	IN to $V_{TT}$ , nIN to $V_{TT}$		50		$\Omega$
$V_{IH}$	Input High Voltage		1.2		$V_{CC}$	V
$V_{IL}$	Input Low Voltage		0		$V_{IH} - 0.1$	V
$V_{IN}$	Input Voltage Swing		0.1		1.4	V
$V_{DIFF\_IN}$	Differential Input Voltage Swing		0.2		2.8	V
$V_{REF}$	Bias Voltage Reference			$V_{CC} - 1.3$		V
$C_{IN}$	Input Capacitance			2		pF

**Table 2C. LVPECL DC Characteristics,  $V_{CC} = 3.3V \pm 10\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OH}$	Output High Voltage; NOTE 1		$V_{CC} - 1.4$		$V_{CC} - 0.76$	V
$V_{OL}$	Output Low Voltage; NOTE 1		$V_{CC} - 2.0$		$V_{CC} - 1.6$	V
$V_{SWING}$	Peak-to-Peak Output Voltage Swing		0.6		1.1	V

NOTE 1: The outputs are terminated with  $50\Omega$  to  $V_{CC} - 2V$ .

**Table 2D. LVPECL DC Characteristics,  $V_{CC} = 2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OH}$	Output High Voltage; NOTE 1		$V_{CC} - 1.4$		$V_{CC} - 0.56$	V
$V_{OL}$	Output Low Voltage; NOTE 1		$V_{CC} - 2.0$		$V_{CC} - 1.5$	V
$V_{SWING}$	Peak-to-Peak Output Voltage Swing		0.4		1.1	V

NOTE 1: The outputs are terminated with  $50\Omega$  to  $V_{CC} - 2V$ .

## AC Characteristics

**Table 3. AC Characteristics**,  $V_{CC} = 2.5V-5\%$  to  $V_{CC} = 3.3V+10\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{REF}$	Input Reference Frequency				3	GHz
$t_{PD}$	Propagation Delay, NOTE 1	$V_{CC} = 3.3V$	75	135	175	ps
		$V_{CC} = 2.5V$	85	130	200	ps
$t_{sk(p)}$	Output Pulse Skew				15	ps
$t_{sk(o)}$	Output Skew, NOTE 2, 3	$V_{CC} = 3.3V$			10	ps
		$V_{CC} = 2.5V$			17	ps
$t_{sk(pp)}$	Part-to-Part Skew, NOTE 3, 4				50	ps
odc	Output Duty Cycle		47		53	%
$f_{jit}$	Buffer Additive Phase Jitter, RMS; Refer to Additive Phase Jitter Section	122.88MHz, Integration Range:10Hz – 10MHz		45		fs
	Phase Noise Frequency Offset	122.88MHz, Offset: 10Hz		-98		dBc/Hz
		122.88MHz, Offset: 100Hz		-128		dBc/Hz
		122.88MHz, Offset: 1kHz		-150		dBc/Hz
		122.88MHz, Offset: 10kHz		-158		dBc/Hz
		122.88MHz, Offset: 100kHz		-161		dBc/Hz
		122.88MHz, Offset: >1MHz		-161		dBc/Hz
	Power Supply Rejection; NOTE 5	$V_{CC} = 3.3V$		3		ps/V
$t_R / t_F$	Output Rise/Fall Time	$V_{CC} = 3.3V$ , 20% to 80%		90	135	ps
		$V_{CC} = 2.5V$ , 20% to 80%		110	170	ps

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE: All parameters characterized at  $f_{REF} \leq 2GHz$ , unless noted otherwise.

NOTE 1: Measured from the differential input crossing point to the differential output crosspoint.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential crosspoints.

NOTE 3: This parameter is defined according with JEDEC Standard 65.

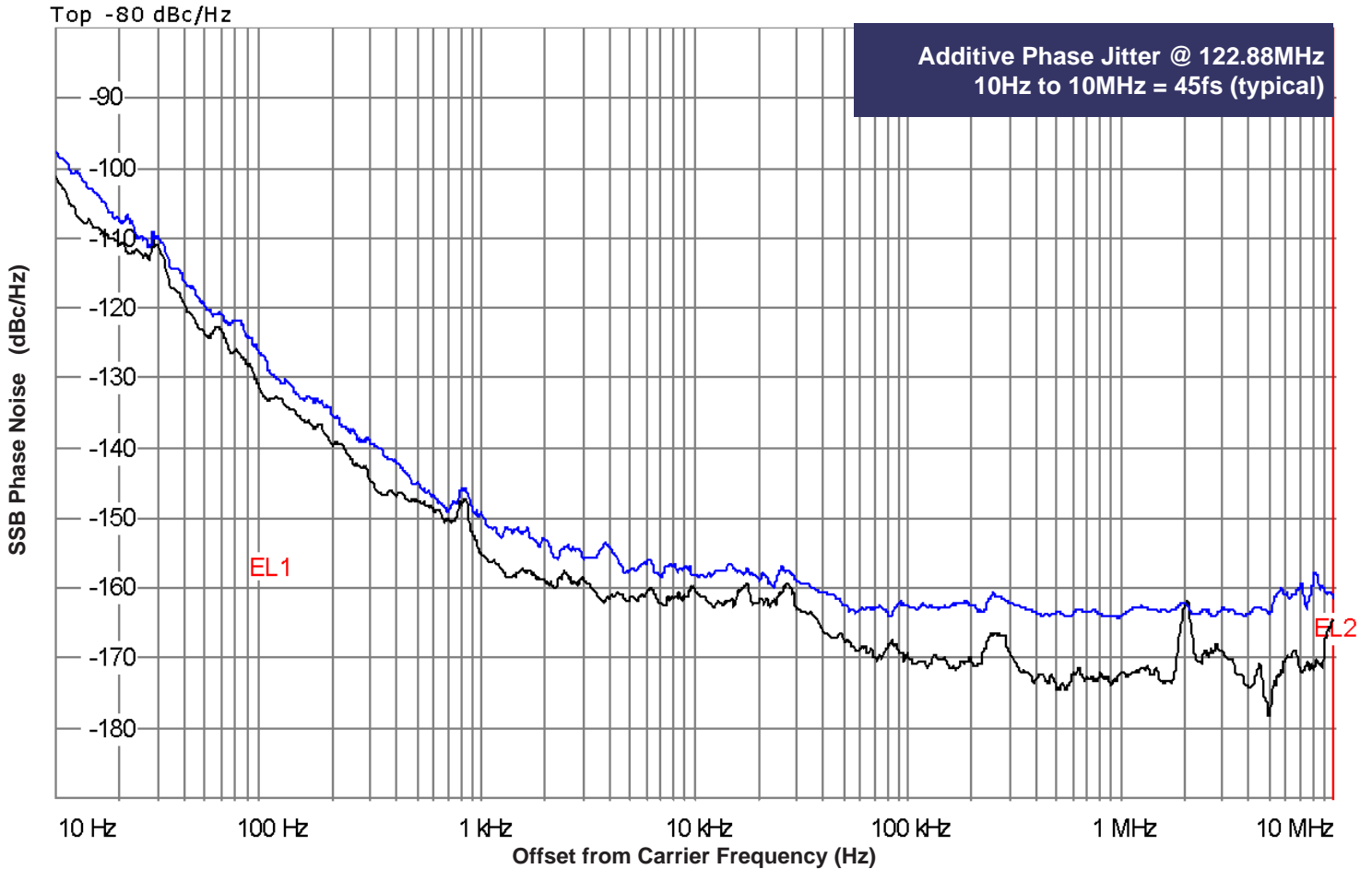
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential crosspoints.

NOTE 5: Change in  $t_{PD}$  per change in  $V_{CC}$ .

## Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the **dBc Phase Noise**. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio

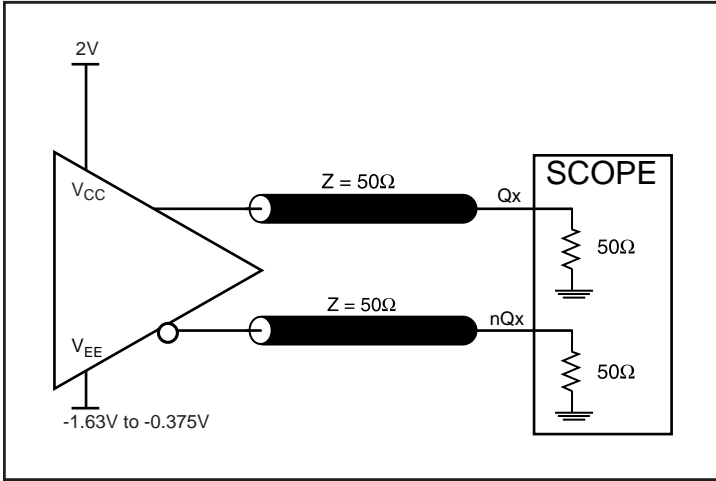
of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a **dBc** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



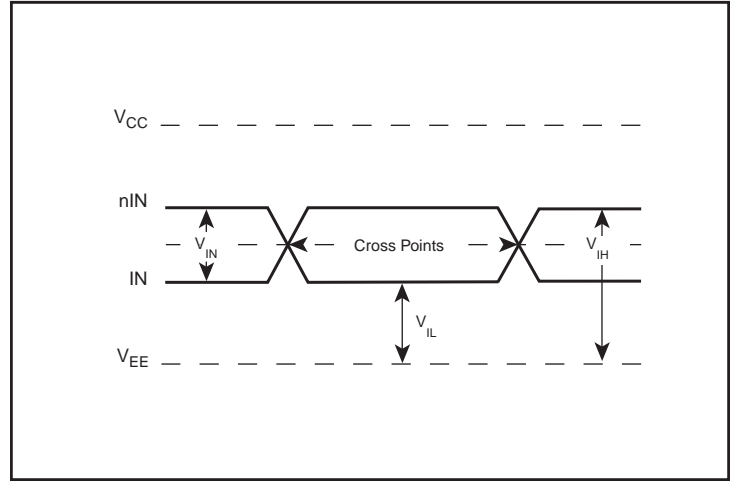
As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

The source generator used is, low noise Wenzel Oscillator at 122.88MHz.

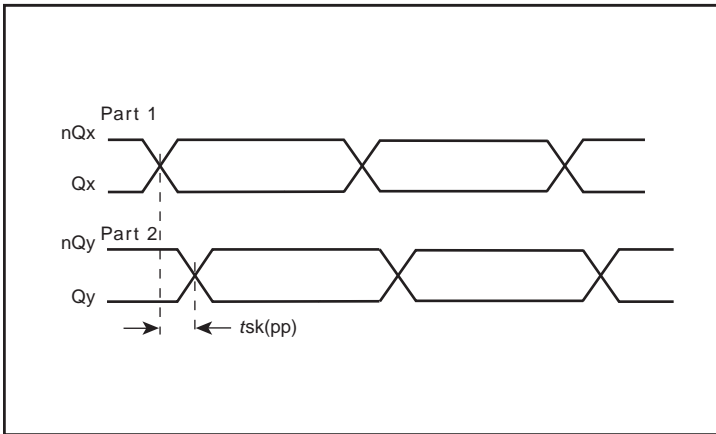
## Parameter Measurement Information



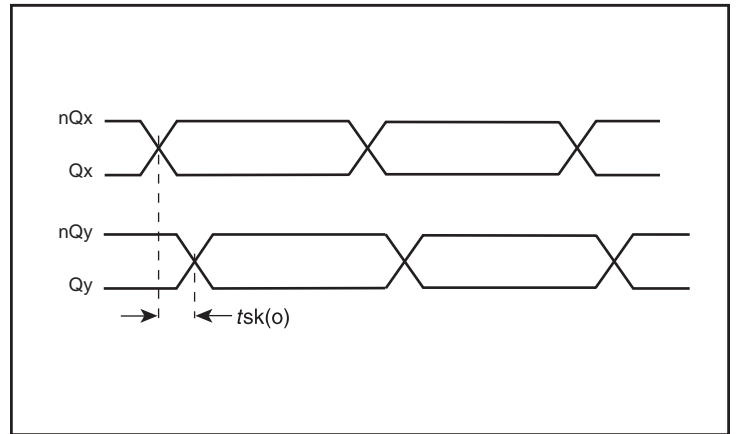
Output Load AC Test Circuit



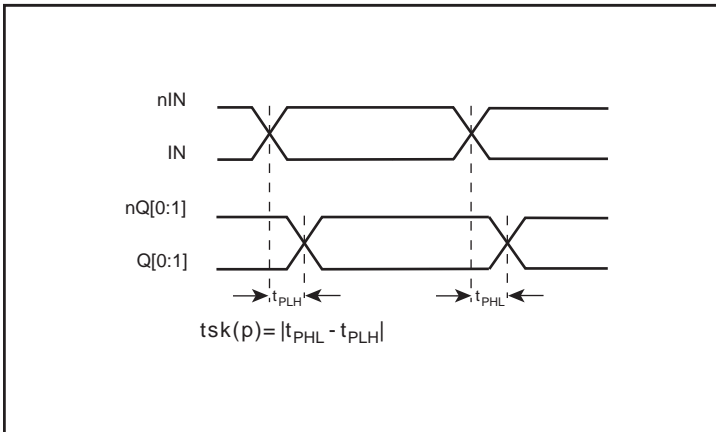
Differential Input Level



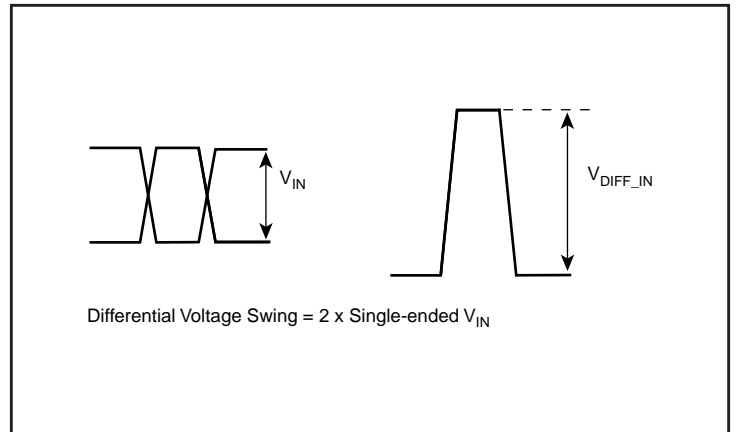
Part-to-Part Skew



Output Skew

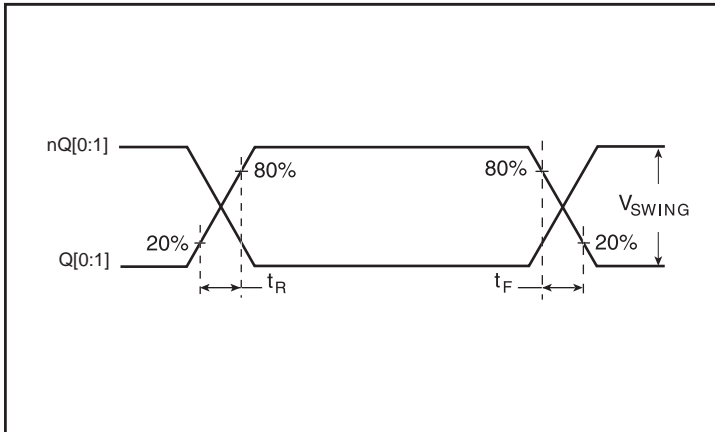


Pulse Skew

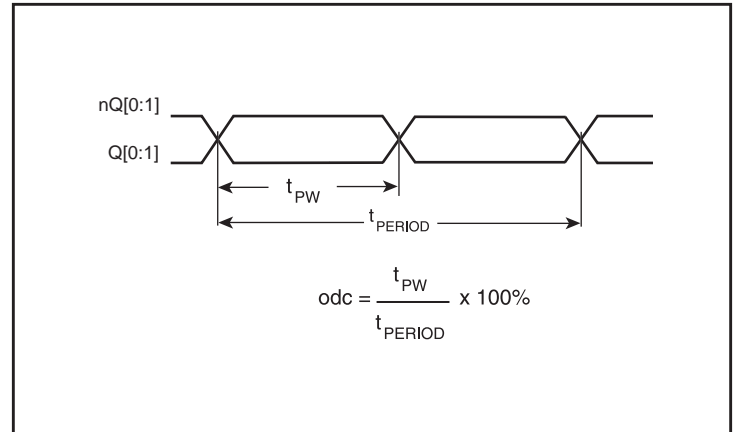


Single-ended & Differential Input Voltage Swing

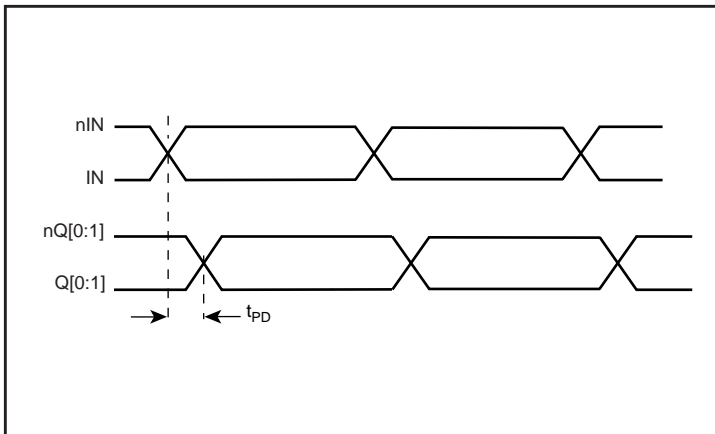
## Parameter Measurement Information, continued



Output Rise/Fall Time



Output Duty Cycle/Pulse Width/Period



Propagation Delay

## Applications Information

### Recommendations for Unused Output Pins

#### Outputs:

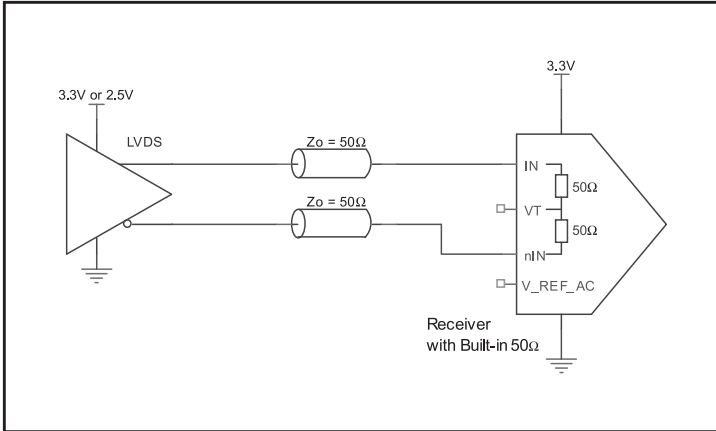
##### LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

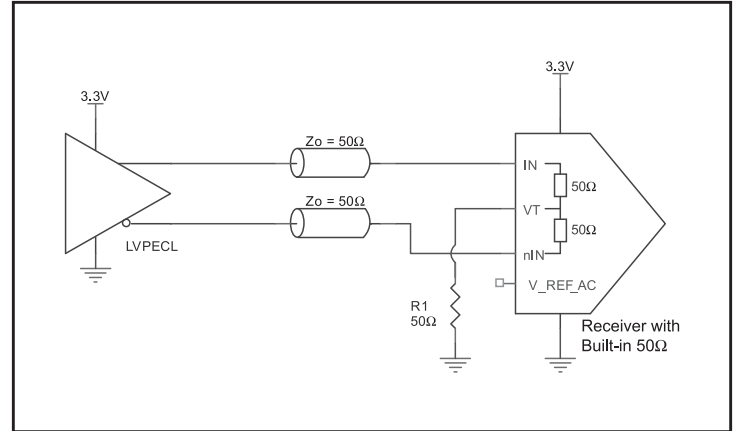
### 3.3V Differential Input with Built-In 50Ω Termination Interface

The IN/nIN with built-in 50Ω terminations accept LVDS, LVPECL, CML and other differential signals. Both differential signals must meet the  $V_{IN}$  and  $V_{IH}$  input requirements. *Figures 2A to 2C* show interface examples for the IN/nIN input with built-in 50Ω terminations driven by the most common driver types. The input interfaces

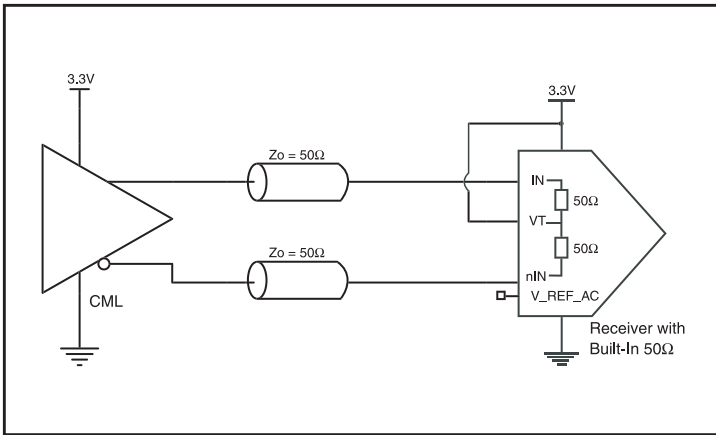
suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.



**Figure 2A. IN/nIN Input with Built-In 50Ω Driven by an LVDS Driver**



**Figure 2B. IN/nIN Input with Built-In 50Ω Driven by an LVPECL Driver**



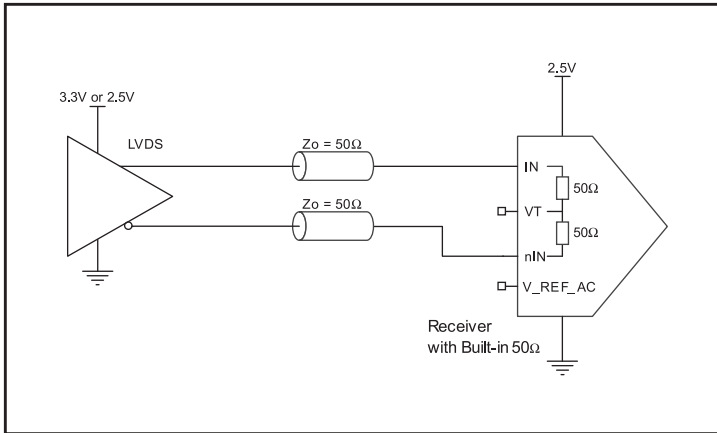
**Figure 2C. IN/nIN Input with Built-In 50Ω Driven by a CML Driver**



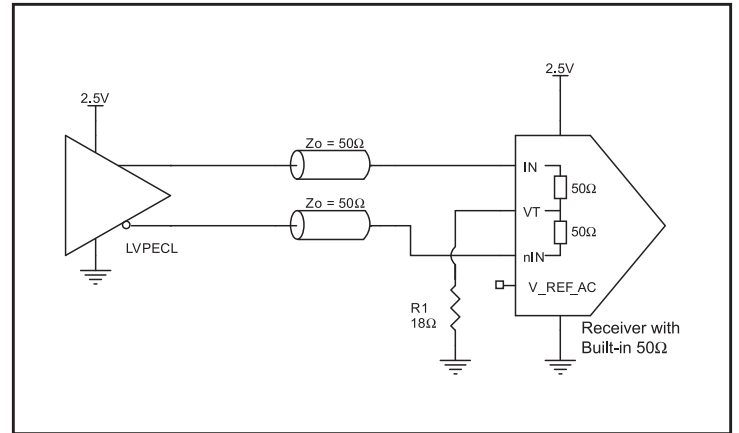
## 2.5V LVPECL Input with Built-In 50Ω Termination Interface

The IN/nIN with built-in 50Ω terminations accept LVDS, LVPECL, CML and other differential signals. Both differential signals must meet the  $V_{IN}$  and  $V_{IH}$  input requirements. *Figures 3A to 3C* show interface examples for the IN/nIN with built-in 50Ω termination input driven by the most common driver types. The input interfaces

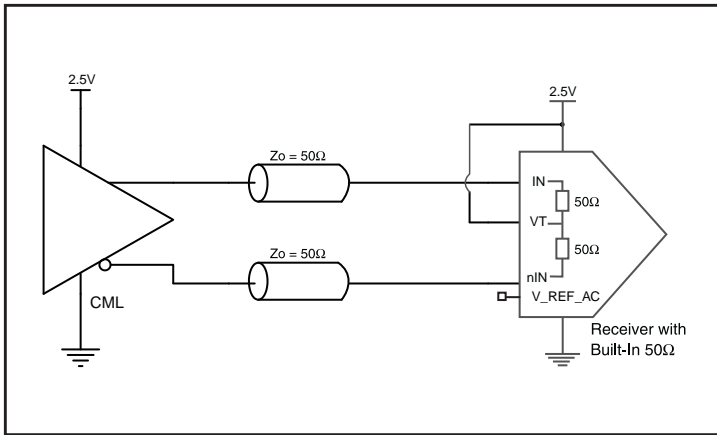
suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.



**Figure 3A. IN/nIN Input with Built-In 50Ω Driven by an LVDS Driver**



**Figure 3B. IN/nIN Input with Built-In 50Ω Driven by an LVPECL Driver**



**Figure 3C. IN/nIN Input with Built-In 50Ω Driven by a CML Driver**

### 2.5V Differential Input with Built-In 50Ω Termination Unused Input Handling

To prevent oscillation and to reduce noise, it is recommended to have pullup and pulldown connect to true and compliment of the unused input as shown in Figure 4A.

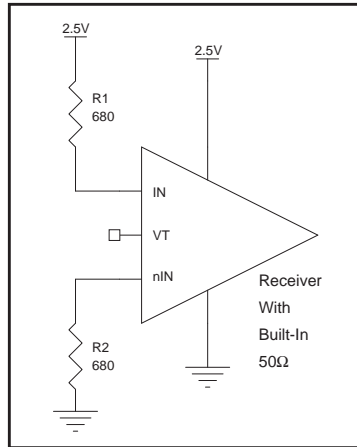


Figure 4A. Unused Input Handling

### 3.3V Differential Input with Built-In 50Ω Termination Unused Input Handling

To prevent oscillation and to reduce noise, it is recommended to have pullup and pulldown connect to true and compliment of the unused input as shown in Figure 4B.

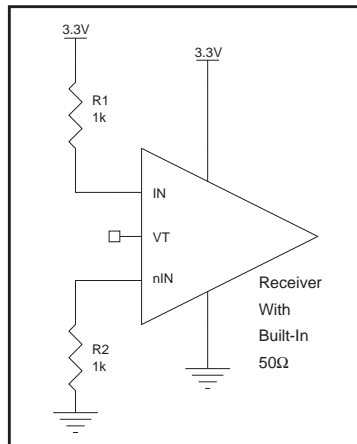


Figure 4B. Unused Input Handling

## Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω

transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion.

Figures 5A and 5B show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

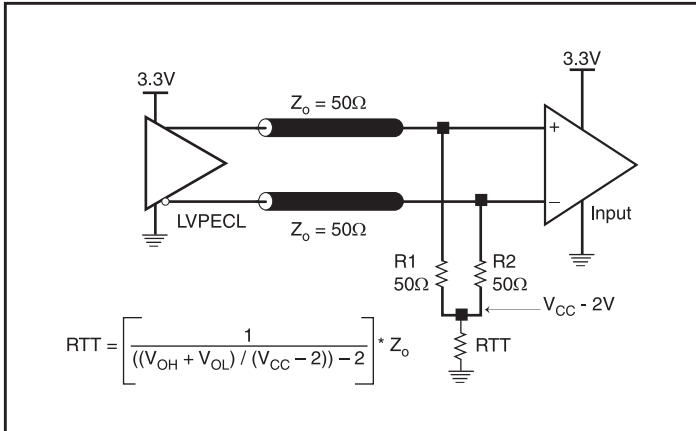


Figure 5A. 3.3V LVPECL Output Termination

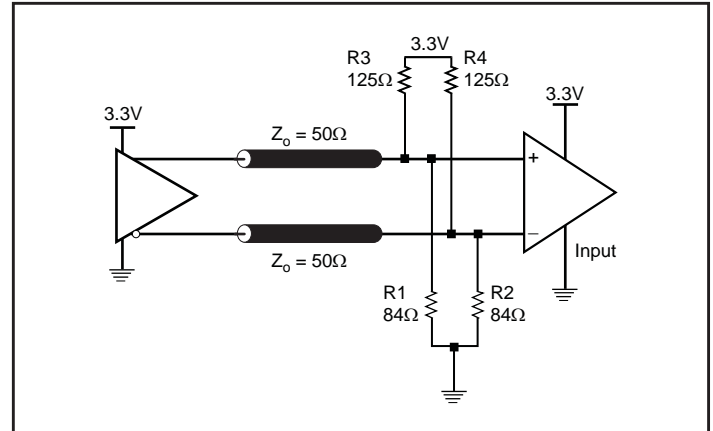


Figure 5B. 3.3V LVPECL Output Termination

## Termination for 2.5V LVPECL Outputs

Figure 6A and Figure 6B show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating  $50\Omega$  to  $V_{CC} - 2V$ . For  $V_{CC} = 2.5V$ , the  $V_{CC} - 2V$  is very close to ground

level. The R3 in Figure 6B can be eliminated and the termination is shown in Figure 6C.

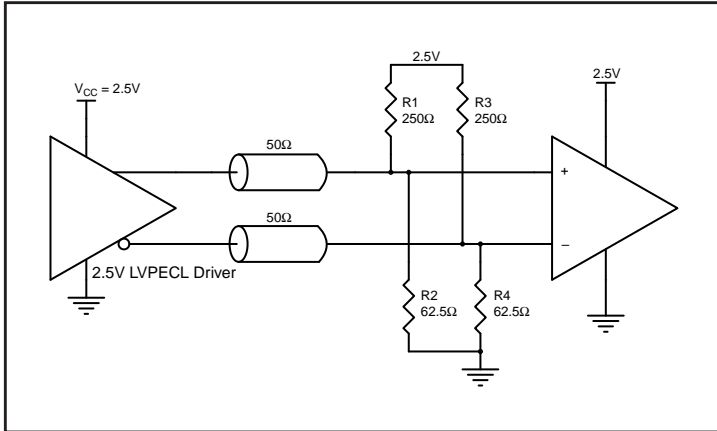


Figure 6A. 2.5V LVPECL Driver Termination Example

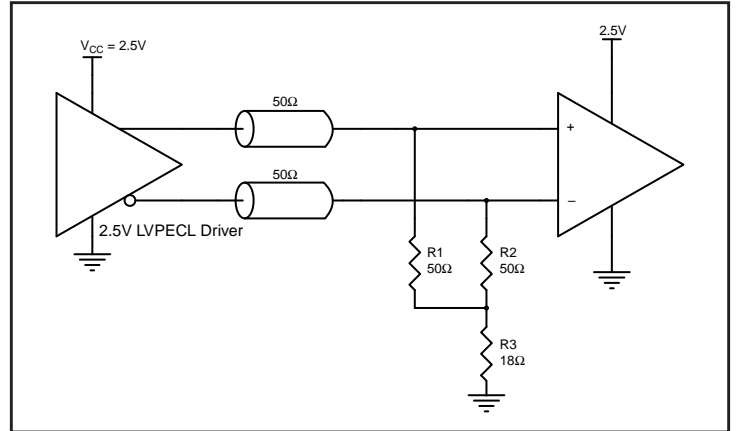


Figure 6B. 2.5V LVPECL Driver Termination Example

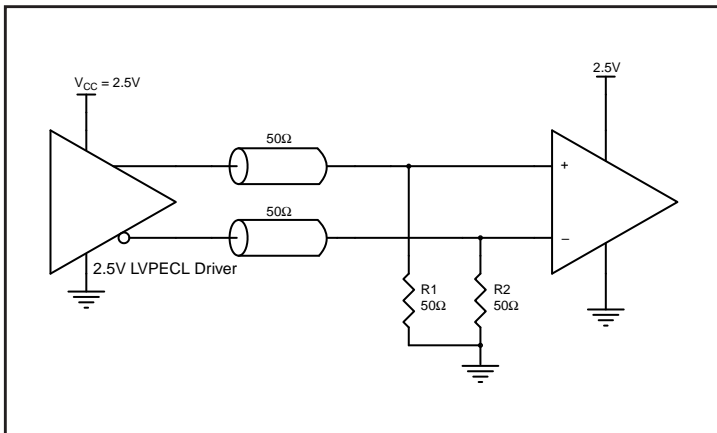


Figure 6C. 2.5V LVPECL Driver Termination Example

## VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 7*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific

and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.

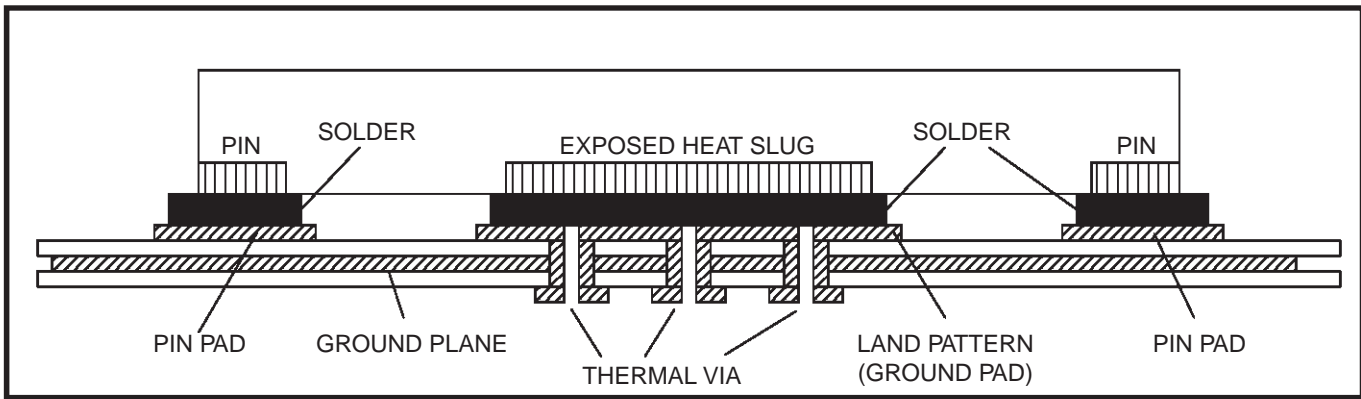


Figure 7. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

## Power Considerations

This section provides information on power dissipation and junction temperature for the ICS853S9252I. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS853S9252I is the sum of the core power plus the power dissipation in the load(s). The following is the power dissipation for  $V_{CC} = 3.3V + 10\% = 3.63V$ , which gives worst case results.

- Power (core)<sub>MAX</sub> =  $V_{CC\_MAX} * I_{EE\_MAX} = 3.63V * 33mA = 119.8mW$
- Power (outputs)<sub>MAX</sub> = **30mW/Loaded Output pair**  
If all outputs are loaded, the total power is  $2 * 31.6mW = 63.2mW$
- Power Dissipation for internal termination  $R_T$   
Power (R<sub>T</sub>)<sub>MAX</sub> =  $(V_{IN\_MAX})^2 / R_{T\_MIN} = (1.4V)^2 / 50\Omega = 39.2mW$

**Total Power** = Power (core)<sub>MAX</sub> + Power (output)<sub>MAX</sub> + Power (R<sub>T</sub>)<sub>MAX</sub> =  $119.8mW + 63.2mW + 39.2mW = 222.2mW$

### 2. Junction Temperature.

Junction temperature, T<sub>j</sub>, is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, T<sub>j</sub>, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for T<sub>j</sub> is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

T<sub>j</sub> = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

Pd<sub>total</sub> = Total Device Power Dissipation (example calculation is in section 1 above)

T<sub>A</sub> = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is 74.7°C/W per Table 4 below.

Therefore, T<sub>j</sub> for an ambient temperature of 85°C with all outputs switching is:

$85^\circ C + 0.222W * 74.7^\circ C/W = 101.6^\circ C$ . This is below the limit of 125°C.

This calculation is only an example. T<sub>j</sub> will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

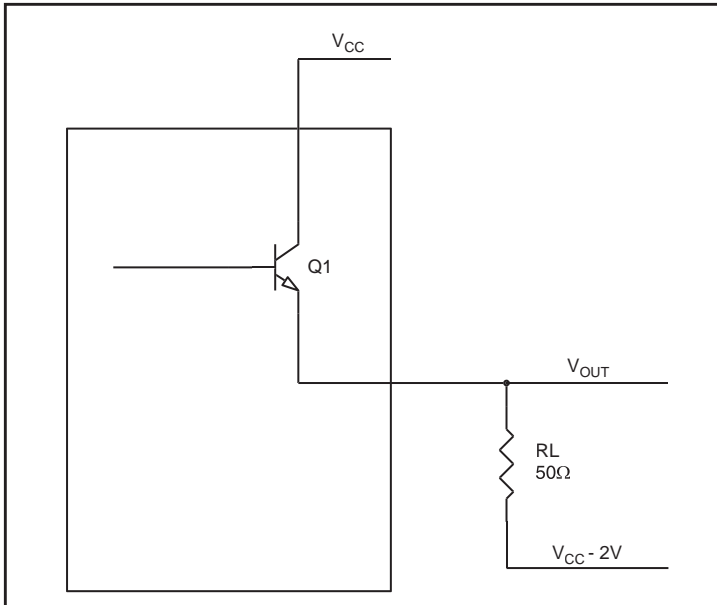
**Table 4. Thermal Resistance  $\theta_{JA}$  for 16 Lead VFQFN, Forced Convection**

Meters per Second	$\theta_{JA}$ by Velocity		
	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	74.7°C/W	65.3°C/W	58.5°C/W

### 3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pairs.

The LVPECL output driver circuit and termination are shown in *Figure 8*.



**Figure 8. LVPECL Driver Circuit and Termination**

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V<sub>CC</sub> - 2V.

- For logic high, V<sub>OUT</sub> = V<sub>OH\_MAX</sub> = V<sub>CC\_MAX</sub> - 0.76V  
(V<sub>CC\_MAX</sub> - V<sub>OH\_MAX</sub>) = 0.76V
- For logic low, V<sub>OUT</sub> = V<sub>OL\_MAX</sub> = V<sub>CC\_MAX</sub> - 1.6V  
(V<sub>CC\_MAX</sub> - V<sub>OL\_MAX</sub>) = 1.6V

Pd<sub>H</sub> is power dissipation when the output drives high.

Pd<sub>L</sub> is the power dissipation when the output drives low.

$$Pd_H = [(V_{OH\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - 0.76V)/50\Omega] * 0.76V = \mathbf{18.8mW}$$

$$Pd_L = [(V_{OL\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - 1.6V)/50\Omega] * 1.6V = \mathbf{12.8mW}$$

Total Power Dissipation per output pair = Pd<sub>H</sub> + Pd<sub>L</sub> = **31.6mW**

## Reliability Information

**Table 5.  $\theta_{JA}$  vs. Air Flow Table for a 16 Lead VFQFN**

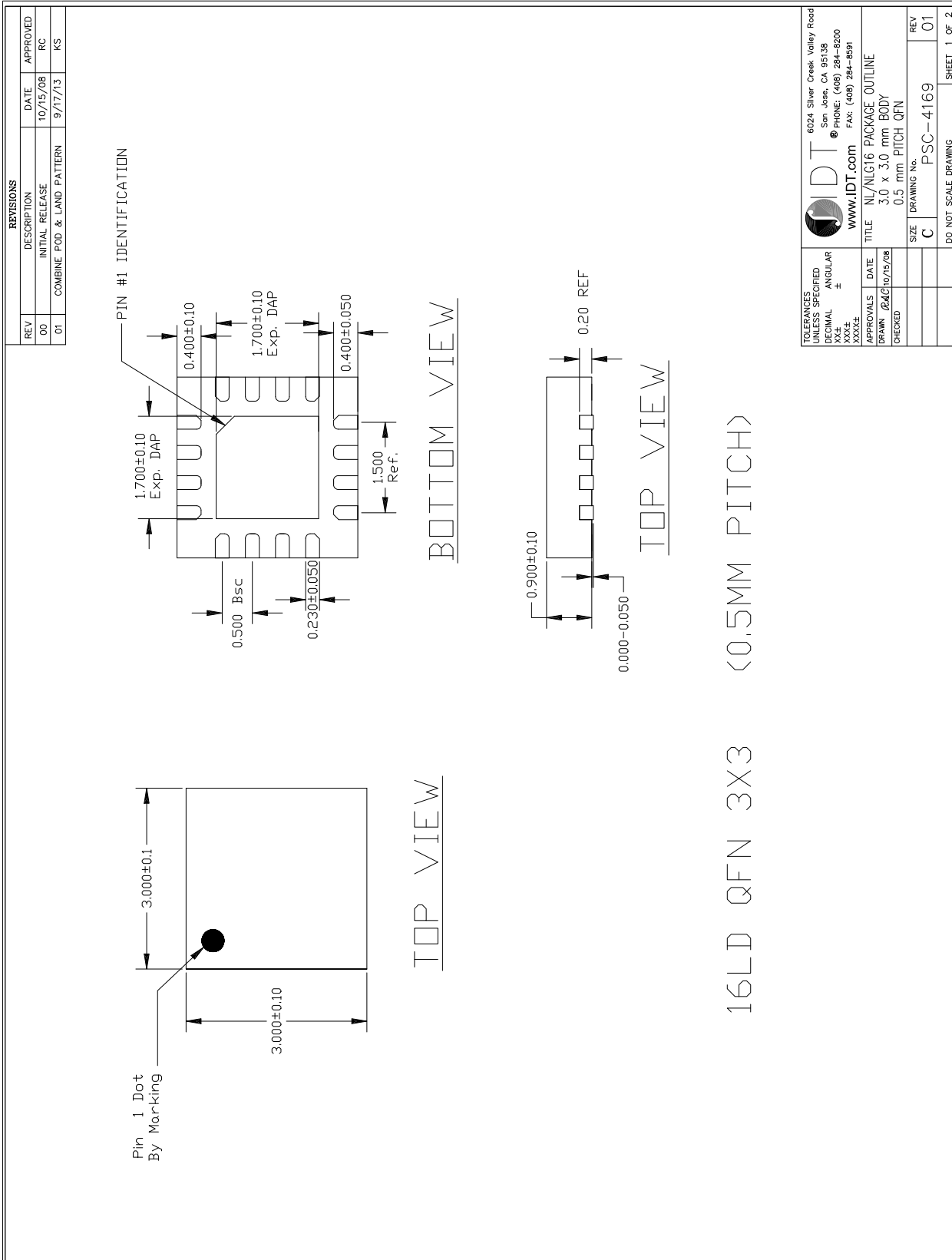
$\theta_{JA}$ by Velocity			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	74.7°C/W	65.3°C/W	58.5°C/W

## Transistor Count

The transistor count for ICS853S9252I is: 190



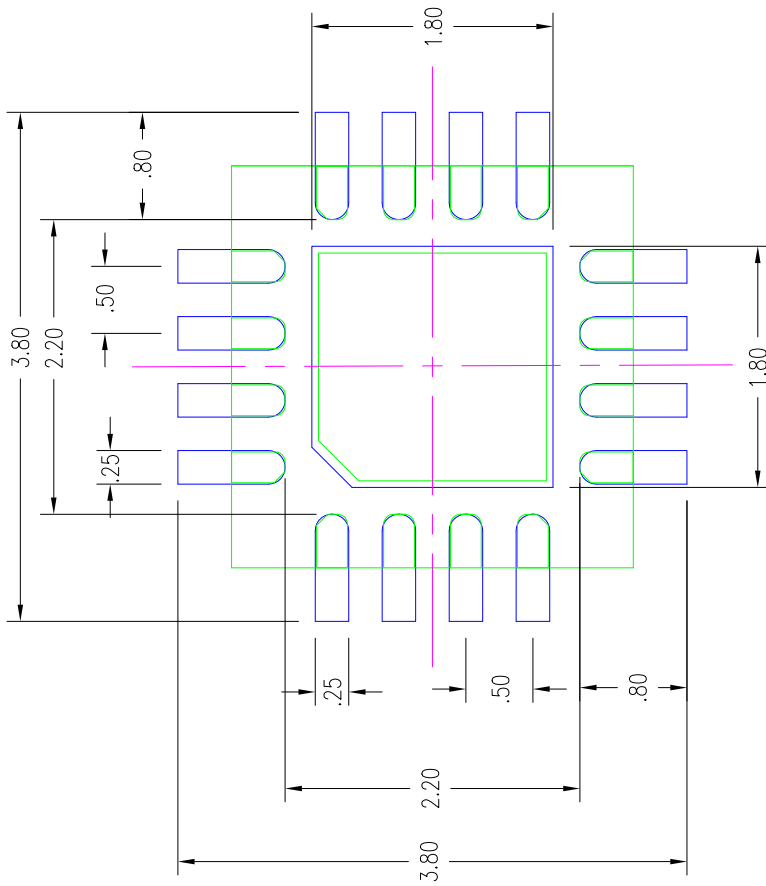
# 16 Lead VFQFN Package Outline and Package Dimensions – Sheet 1



TOLERANCES UNLESS SPECIFIED	6024 Silver Creek Valley Road
ANGULAR	San Jose, CA 95138
XXX	PHONE: (408) 284-8200
XXXX	FAX: (408) 284-8591
XXXXX	
APPROVALS	WWW.IDT.COM
DRAWN @JAC/10/15/08	TITLE NL/NLIG16 PACKAGE OUTLINE
CHECKED	3.0 x 3.0 mm BODY
	0.5 mm PITCH QFN
SIZE	DRAWING No. PSC-4169
C	REV 01
	DO NOT SCALE DRAWING
	SHEET 1 OF 2

# 16 Lead VFQFN Package Outline and Package Dimensions – Sheet 2

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	10/15/08	RC
01	COMBINE POD & LAND PATTERN	9/17/13	KS



**NOTES:**

1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW, AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

TOLERANCES UNLESS SPECIFIED	DECIMAL	ANGULAR	±
DRAWN	02/21/15/08	DATE	
CHECKED		APPROVALS	
6024 Silver Creek Valley Road San Jose, CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-8591 www.IDT.com			
TITLE: N/16G16 PACKAGE OUTLINE 3.0 x 3.0 mm BODY 0.5 mm PITCH QFN			
SIZE	C	DRAWING No.	PSC-4169
REV	01	DO NOT SCALE DRAWING	SHEET 2 OF 2

## Ordering Information

Table 6. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
853S9252BKILF	252B	"Lead-Free" 16 Lead VFQFN	Tube	-40°C to 85°C
853S9252BKILFT	252B	"Lead-Free" 16 Lead VFQFN	Tape & Reel, Pin 1 Orientation: EIA-481-C	-40°C to 85°C
853S9252BKILF/W	252B	"Lead-Free" 16 Lead VFQFN	Tape & Reel, Pin 1 Orientation: EIA-481-D	-40°C to 85°C

Table 7. Pin 1 Orientation in Tape and Reel Packaging

Part Number Suffix	Pin 1 Orientation	Illustration
T	Quadrant 1 (EIA-481-C)	
/W	Quadrant 2 (EIA-481-D)	

## Revision History Sheet

Date	Description of Change
6/14/2017	Updated the packaging diagrams
7/17/2013	Ordering Information Table - added additional row. Added Orientation Packaging Table.



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(Rev.1.0 Mar 2020)

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