

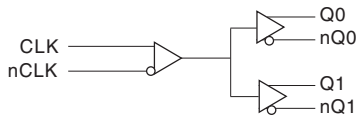
## GENERAL DESCRIPTION

The 854111 is a low skew, high performance 1-to-2 Differential-to-LVDS Fanout Buffer and a member of the family of High Performance Clock Solutions from IDT. The CLK, nCLK pair can accept most standard differential input levels. The 854111 is characterized to operate from a 3.3V power supply. Guaranteed output and part-to-part skew characteristics make the 854111 ideal for those clock distribution applications demanding well defined performance and repeatability.

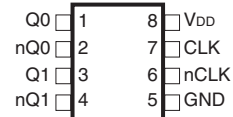
## FEATURES

- Two differential LVDS outputs
- One differential CLK, nCLK clock input
- CLK, nCLK pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Maximum output frequency: 650MHz
- Translates any single ended input signal to LVDS levels with resistor bias on nCLK input
- Output skew: 25ps (maximum)
- Part-to-part skew: 300ps (maximum)
- Additive phase jitter, RMS: 0.05ps (typical)
- Propagation delay: 2.5ns (maximum)
- 3.3V operating supply
- -40°C to 85°C ambient operating temperature
- Available in lead free (RoHS 6) package

## BLOCK DIAGRAM



## PIN ASSIGNMENT



**854111**  
**8-Lead SOIC**  
 3.90mm x 4.90mm x 1.37mm package body  
**M Package**  
 Top View

**TABLE 1. PIN DESCRIPTIONS**

Number	Name	Type		Description
1, 2	Q0, nQ0	Output		Differential output pair. LVDS interface levels.
3, 4	Q1, nQ1	Output		Differential output pair. LVDS interface levels.
5	GND	Power		Power supply ground.
6	nCLK	Input	Pulldown	Inverting differential clock input.
7	CLK	Input	Pullup	Non-inverting differential clock input.
8	V <sub>DD</sub>	Power		Positive supply pin.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**TABLE 2. PIN CHARACTERISTICS**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
R <sub>PULLUP</sub>	Input Pullup Resistor			51		kΩ
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			51		kΩ

### ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $V_{DD}$	4.6V
Inputs, $V_I$	-0.5V to $V_{DD} + 0.5V$
Outputs, $I_O$	
Continuous Current	10mA
Surge Current	15mA
Package Thermal Impedance, $\theta_{JA}$	112.7°C/W (0 lfpm)
Storage Temperature, $T_{STG}$	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 3A. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 10\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Positive Supply Voltage		2.97	3.3	3.63	V
$I_{DD}$	Power Supply Current				50	mA

**TABLE 3B. DIFFERENTIAL DC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 10\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$I_{IH}$	Input High Current	CLK	$V_{DD} = V_{IN} = 3.63V$		5	$\mu\text{A}$
		nCLK	$V_{DD} = V_{IN} = 3.63V$		150	$\mu\text{A}$
$I_{IL}$	Input Low Current	CLK	$V_{DD} = 3.63, V_{IN} = 0V$	-150		$\mu\text{A}$
		nCLK	$V_{DD} = 3.63V, V_{IN} = 0V$	-5		$\mu\text{A}$
$V_{PP}$	Peak-to-Peak Input Voltage; NOTE 1		0.15		1.3	V
$V_{CMR}$	Common Mode Input Voltage; NOTE 1, 2		0.5		$V_{DD} - 0.85$	V

NOTE 1:  $V_{IL}$  should not be less than -0.3V.

NOTE 2: Common mode voltage is defined as  $V_{IH}$ .

**TABLE 3C. LVDS DC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 10\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OD}$	Differential Output Voltage		247	325	454	mV
$\Delta V_{OD}$	VOD Magnitude Change			0	50	mV
$V_{OS}$	Offset Voltage		1.325	1.45	1.575	V
$\Delta V_{OS}$	VOS Magnitude Change			5	50	mV
$I_{OFF}$	Power Off Leakage		-20	$\pm 1$	+20	$\mu\text{A}$
$I_{OSD}$	Differential Output Short Circuit Current			-3.5	-5	mA
$I_{OS}$	Output Short Circuit Current			-3.5	-5	mA

**TABLE 4. AC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 10\%$   $T_A = -40^\circ C$  TO  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Output Frequency				650	MHz
$t_{PD}$	Propagation Delay; NOTE 1		1.5		2.5	ns
$t_{sk(o)}$	Output Skew; NOTE 2, 4				25	ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 3, 4				300	ps
$t_{jit}$	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	(12kHz to 20MHz)		0.05		ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80% @ 50MHz	150		350	ps
odc	Output Duty Cycle	$f > 500MHz$	46		54	%
		$f \leq 500MHz$	48		52	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

All parameters measured at  $f \leq 650MHz$  unless noted otherwise.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.

Measured at the output differential cross points.

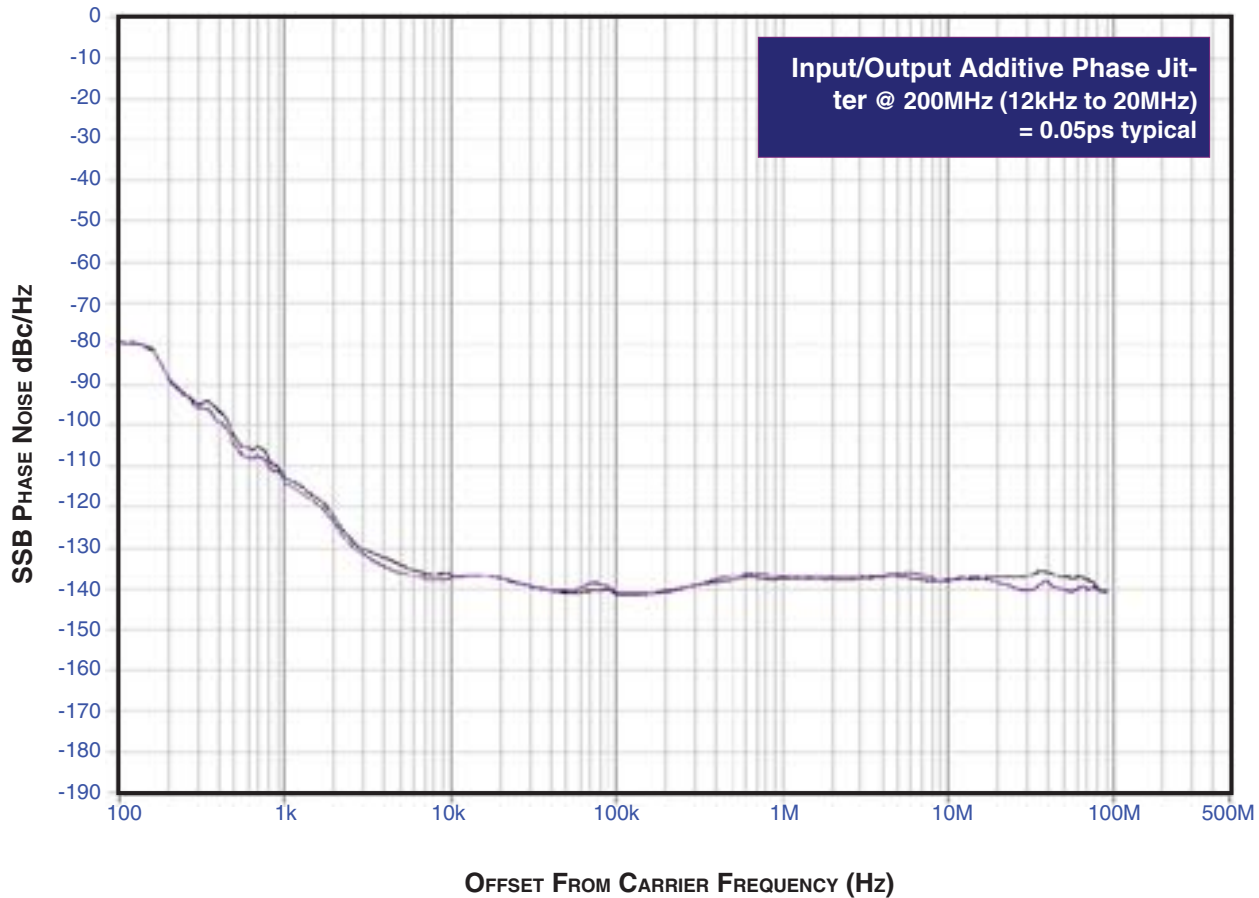
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

## ADDITIVE PHASE JITTER

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the **dBc Phase Noise**. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels

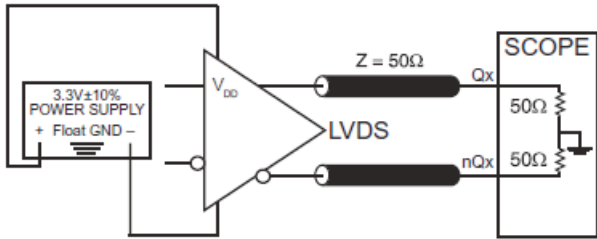
(dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a **dBc** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



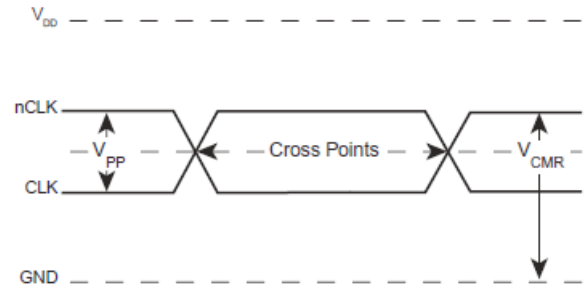
As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device.

This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

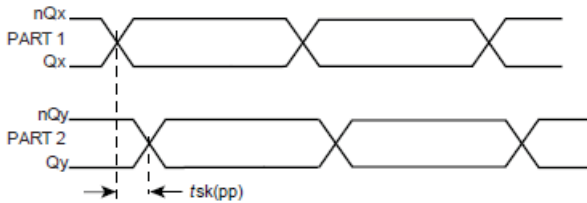
# PARAMETER MEASUREMENT INFORMATION



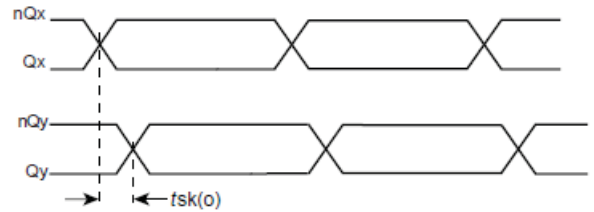
3.3V OUTPUT LOAD AC TEST CIRCUIT



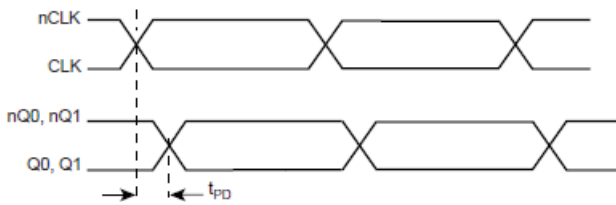
DIFFERENTIAL INPUT LEVEL



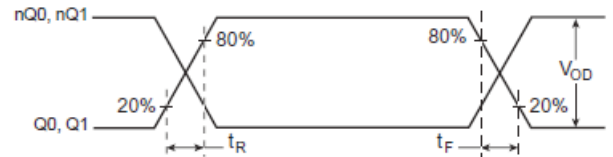
PART-TO-PART SKEW



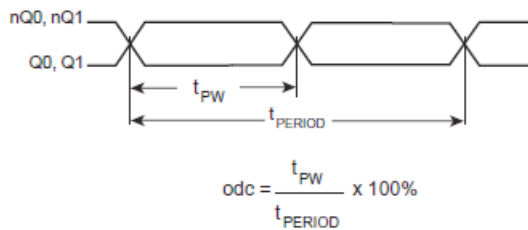
OUTPUT SKEW



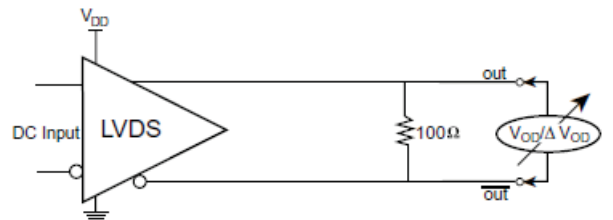
PROPAGATION DELAY



OUTPUT RISE/FALL TIME

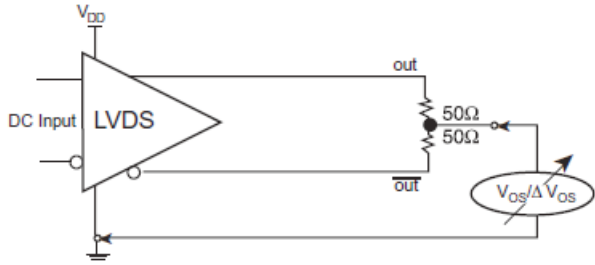


OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

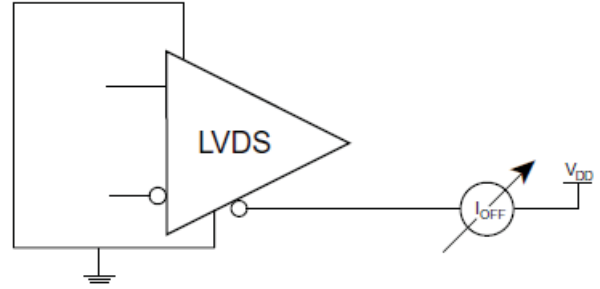


DIFFERENTIAL OUTPUT VOLTAGE SETUP

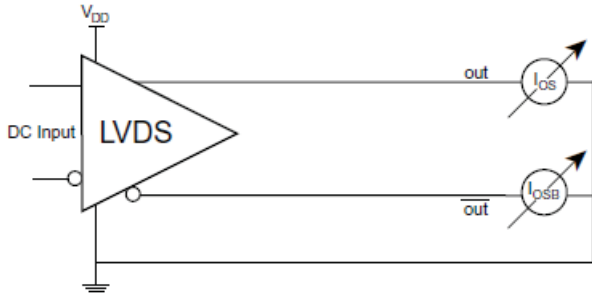
## PARAMETER MEASUREMENT INFORMATION, CONTINUED



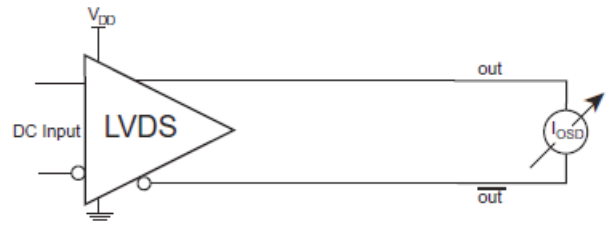
OFFSET VOLTAGE SETUP



POWER OFF LEAKAGE SETUP



OUTPUT SHORT CIRCUIT CURRENT SETUP



DIFFERENTIAL OUTPUT SHORT CIRCUIT CURRENT SETUP

## APPLICATION INFORMATION

### WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage  $V_{REF} = V_{DD}/2$  is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio

of R1 and R2 might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and  $V_{DD} = 3.3V$ ,  $V_{REF}$  should be 1.25V and  $R2/R1 = 0.609$ .

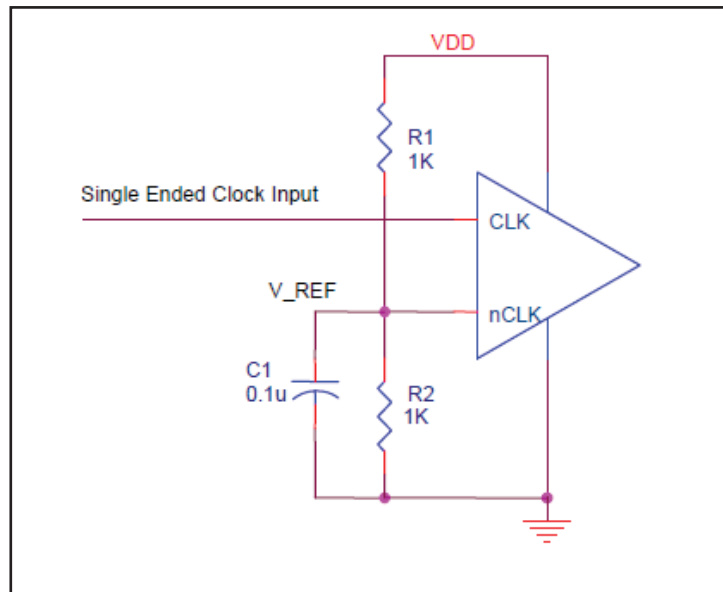


FIGURE 1. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

### RECOMMENDATIONS FOR UNUSED OUTPUT PINS

#### OUTPUTS:

##### LVDS

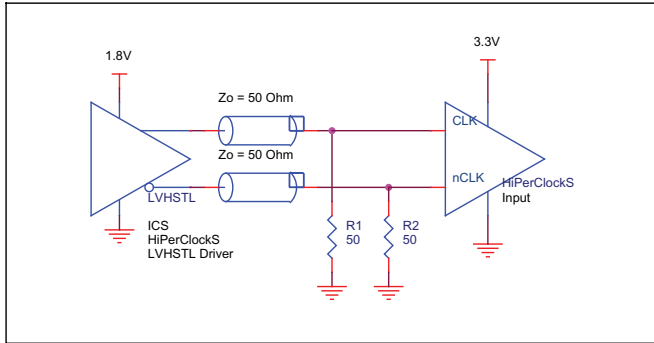
All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.



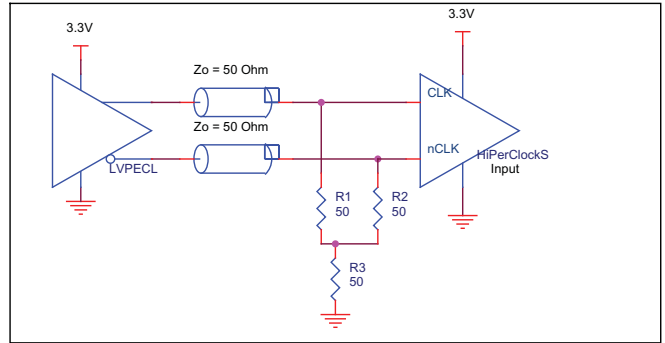
## DIFFERENTIAL CLOCK INPUT INTERFACE

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both signals must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. Figures 2A to 2E show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only.

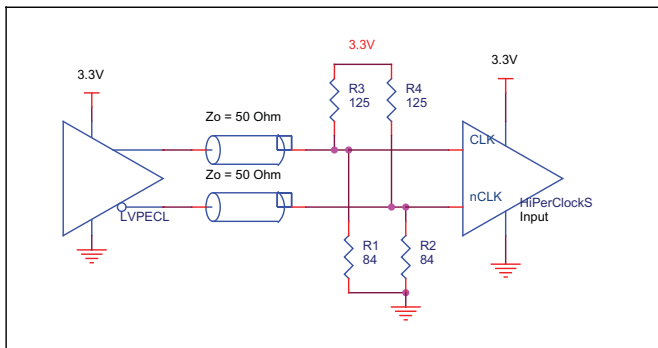
Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 2A*, the input termination applies for IDT HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.



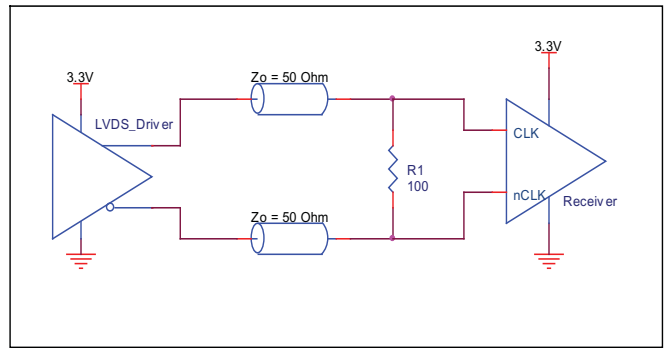
**FIGURE 2A. HiPerClockS CLK/nCLK INPUT DRIVEN BY IDT HiPerClockS LVHSTL DRIVER**



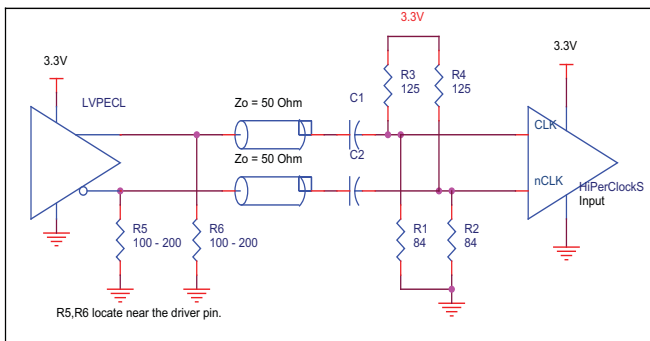
**FIGURE 2B. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER**



**FIGURE 2C. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER**



**FIGURE 2D. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVDS DRIVER**

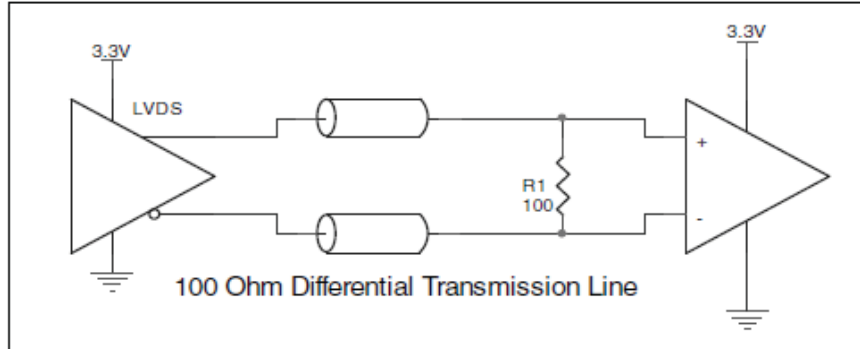


**FIGURE 2E. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER WITH AC COUPLE**

**LVDS DRIVER TERMINATION**

A general LVDS interface is shown in *Figure 3*. In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near

the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.



**FIGURE 3. TYPICAL LVDS DRIVER TERMINATION**

## POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the854111. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the854111 is the sum of the core power plus the power dissipated in the load(s).

The following is the power dissipation for  $V_{DD} = 3.3V + 10\% = 3.63V$ , which gives worst case results.

- $\text{Power (core)}_{MAX} = V_{DD\_MAX} * I_{DD\_MAX} = 3.63V * 50mA = \mathbf{181.5mW}$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 103.3°C/W per Table 5 below.

Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ\text{C} + 0.182\text{W} * 103.3^\circ\text{C/W} = 103.8^\circ\text{C}. \text{ This is below the limit of } 125^\circ\text{C}.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (multi-layer).

**TABLE 5. THERMAL RESISTANCE  $\theta_{JA}$  FOR 8-LEAD SOIC, FORCED CONVECTION**

$\theta_{JA}$ by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	153.3°C/W	128.5°C/W	115.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	112.7°C/W	103.3°C/W	97.1°C/W

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

## RELIABILITY INFORMATION

TABLE 6.  $\theta_{JA}$  vs. AIR FLOW TABLE FOR 8 LEAD SOIC

$\theta_{JA}$ by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	153.3°C/W	128.5°C/W	115.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	112.7°C/W	103.3°C/W	97.1°C/W

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

### TRANSISTOR COUNT

The transistor count for 854111 is: 636

## PACKAGE OUTLINE & DIMENSIONS

PACKAGE OUTLINE - M SUFFIX FOR 8 LEAD SOIC

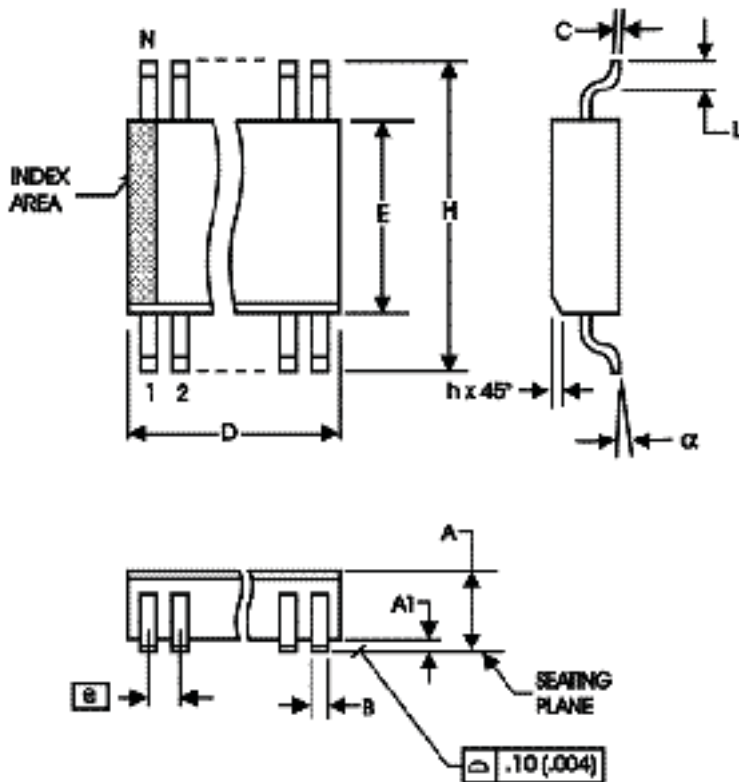


TABLE 7. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	MINIMUM	MAXIMUM
N	8	
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BASIC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
$\alpha$	0°	8°

**TABLE 8. ORDERING INFORMATION**

<b>Part/Order Number</b>	<b>Marking</b>	<b>Package</b>	<b>Shipping Packaging</b>	<b>Temperature</b>
85411AMILF	85411AIL	8 lead "Lead Free" SOIC	Tray	-40°C to +85°C
85411AMILFT	85411AIL	8 lead "Lead Free" SOIC	Tape and Reel	-40°C to +85°C

REVISION HISTORY SHEET				
Rev	Table	Page	Description of Change	Date
B	T3C	3 8 11	<p>Changed <math>V_{DD}</math> from <math>\pm 5\%</math> to <math>\pm 10\%</math> throughout datasheet.</p> <p>LVDS DC Characteristics Table - changed <math>V_{OD}</math> range from 200mV min./360mV max. to 247mV min./454mV max.</p> <p>Changed <math>\Delta V_{OD}</math> from 40mV max. to 50mV max.</p> <p>Changed <math>V_{OS}</math> from 1.125mV min./1.375mV max. to 1.325mV min./1.575mV max.</p> <p>Changed <math>\Delta V_{OS}</math> from 25mV max. to 50mV max.</p> <p>Added <i>Recommendations for Unused Output Pins</i>.</p> <p>Added <i>Power Considerations</i>.</p>	9/25/06
B	3x, 4	3, 4	Corrected temperature in tables.	11/7/07
B	T3C	3	LVDS DC Characteristics Table - deleted $V_{OH}$ & $V_{OL}$ rows.	1/20/09
B	T8	1 1 13	<p>Removed ICS from the part number where needed.</p> <p>General Description - Removed ICS Chip and HiPerClockS.</p> <p>Features section - removed reference to leaded packages.</p> <p>Ordering Information - removed quantity from tape and reel. Deleted the LF note below the table.</p> <p>Updated header and footer.</p>	1/20/16



## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:  
[www.renesas.com/contact/](http://www.renesas.com/contact/)

### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.



## X-ON Electronics

Largest Supplier of Electrical and Electronic Components

*Click to view similar products for [Clock Buffer](#) category:*

*Click to view products by [Renesas](#) manufacturer:*

Other Similar products are found below :

[MPC962309EJ-1H](#) [NB4N121KMNG](#) [IDT49FCT805ASO](#) [MK2308S-1HILF](#) [PL133-27GI-R](#) [NB3L02FCT2G](#) [NB3L03FCT2G](#)  
[ZL40203LDG1](#) [ZL40200LDG1](#) [ZL40205LDG1](#) [9FG1200DF-1LF](#) [9FG1001BGLF](#) [ZL40202LDG1](#) [PI49FCT20802QE](#) [SL2305SC-1T](#)  
[PI6C4931502-04LIE](#) [NB7L1008MNG](#) [NB7L14MN1G](#) [PI49FCT20807QE](#) [PI6C4931502-04LIEX](#) [ZL80002QAB1](#) [PI6C4931504-04LIEX](#)  
[PI6C10806BLEX](#) [ZL40226LDG1](#) [ZL40219LDG1](#) [8T73S208B-01NLGI](#) [SY75578LMG](#) [PI49FCT32805QEX](#) [PL133-27GC-R](#)  
[CDCV304PWG4](#) [MC10LVEP11DG](#) [MC10EP11DTG](#) [MC100LVEP11DG](#) [MC100E111FNG](#) [MC100EP11DTG](#) [NB6N11SMNG](#)  
[NB7L14MMNG](#) [NB6L11MMNG](#) [NB6L14MMNR2G](#) [NB6L611MNG](#) [PL123-02NGI-R](#) [NB3N111KMNR4G](#) [ADCLK944BCPZ-R7](#)  
[ZL40217LDG1](#) [NB7LQ572MNG](#) [HMC940LC4BTR](#) [ADCLK946BCPZ-REEL7](#) [ADCLK946BCPZ](#) [ADCLK846BCPZ-REEL7](#)  
[ADCLK854BCPZ-REEL7](#)