# Low Skew, 1-to-16 LVCMOS/LVTTL Clock Generator

# 87016

**DATASHEET**

## General Description

The 87016 is a low skew, 1:16 LVCMOS/LVTTL Clock Generator. The device has 4 banks of 4 outputs and each bank can be independently selected for ÷1 or ÷2 frequency operation. Each bank also has its own power supply pins so that the banks can operate at the following different voltage levels: 3.3V, 2.5V, and 1.8V. The low impedance LVCMOS/LVTTL outputs are designed to drive 50Ω series or parallel terminated transmission lines.

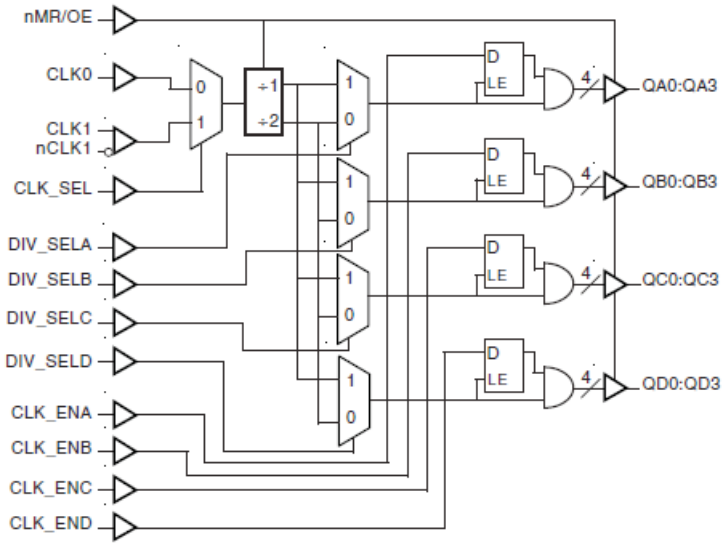
The divide select inputs, DIV_SELA:DIV_SELD, control the output frequency of each bank. The output banks can be independently selected for ÷1 or ÷2 operation. The bank enable inputs, CLK_ENA:CLK_END, support enabling and disabling each bank of outputs individually. The CLK_ENA:CLK_END circuitry has a synchronizer to prevent runt pulses when enabling or disabling the clock outputs. The master reset input, nMR/OE, resets the ÷1/÷2 flip flops and also controls the active and high impedance states of all outputs. This pin has an internal pull-up resistor and is normally used only for test purposes or in systems which use low power modes.

The 87016 is characterized to operate with the core at 3.3V and the banks at 3.3V, 2.5V, or 1.8V. Guaranteed bank, output, and part-to-part skew characteristics make the 87016 ideal for those clock applications demanding well-defined performance and repeatability.

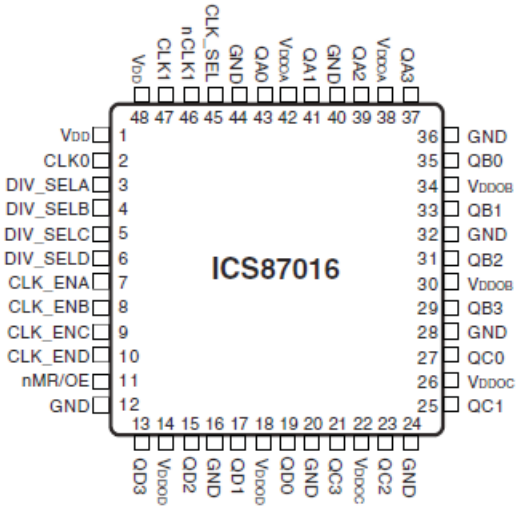
## Features

- Sixteen LVCMOS/LVTTL outputs (4 banks of 4 outputs)
- Selectable differential CLK1, nCLK1 or LVCMOS clock input
- CLK1, nCLK1 pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- CLK0 supports the following input types: LVCMOS, LVTTL
- Maximum output frequency: 250MHz
- Independent bank control for ÷1 or ÷2 operation
- Independent output bank voltage settings for 3.3V, 2.5V, or 1.8V operation
- Asynchronous clock enable/disable
- Output skew: 170ps (maximum)
- Bank skew: 30ps (maximum)
- Part-to-part skew: 750ps (maximum)
- 3.3V core, 3.3V, 2.5V, or 1.8V output operating supply
- 0°C to 85°C ambient operating temperature
- Available in lead-free RoHS compliant package

## Block Diagram




## Pin Assignment




**48-Pin LQFP**

7mm x 7mm x 1.4mm body package

**Y Package**

Top View

**TABLE 1. PIN DESCRIPTIONS**

| Number | Name | Type | | Description |
|---|---|---|---|---|
| 1, 48 | $V_{DD}$ | Power | | Positive supply pins. |
| 2 | CLK0 | Input | Pulldown | LVCMOS / LVTTL clock input. |
| 3 | DIV_SELA | Input | Pullup | Controls frequency division for Bank A outputs. LVCMOS / LVTTL interface levels. |
| 4 | DIV_SELB | Input | Pullup | Controls frequency division for Bank B outputs LVCMOS / LVTTL interface levels.. |
| 5 | DIV_SELC | Input | Pullup | Controls frequency division for Bank C outputs. LVCMOS / LVTTL interface levels. |
| 6 | DIV_SELD | Input | Pullup | Controls frequency division for Bank D outputs. LVCMOS / LVTTL interface levels. |
| 7 | CLK_ENA | Input | Pullup | Output enable for Bank A outputs. Active HIGH. If pin is LOW, outputs drive low. LVCMOS / LVTTL interface levels. |
| 8 | CLK_ENB | Input | Pullup | Output enable for Bank B outputs. Active HIGH. If pin is LOW, outputs drive low. LVCMOS / LVTTL interface levels. |
| 9 | CLK_ENC | Input | Pullup | Output enable for Bank C outputs. Active HIGH. If pin is LOW, outputs drive low. LVCMOS / LVTTL interface levels. |
| 10 | CLK_END | Input | Pullup | Output enable for Bank D outputs. Active HIGH. If pin is LOW, outputs drive low. LVCMOS / LVTTL interface levels. |
| 11 | nMR/OE | Input | Pullup | Master reset. When LOW, resets the ÷1/÷2 flip flops and sets the outputs to high impedance. LVCMOS / LVTTL interface levels. |
| 12, 16, 20, 24, 28, 32, 36, 40, 44 | GND | Power | | Power supply ground. |
| 13, 15, 17, 19 | QD3, QD2, QD1, QD0 | Output | | Bank D outputs. LVCMOS / LVTTL interface levels. |
| 14, 18 | $V_{DDOD}$ | Power | | Output Bank D power supply pins. |
| 21, 23, 25, 27 | QC3, QC2, QC1, QC0 | Output | | Bank C outputs. LVCMOS / LVTTL interface levels. |
| 22, 26 | $V_{DDOC}$ | Power | | Output Bank C power supply pins. |
| 29, 31, 33, 35 | QB3, QB2, QB1, QB0 | Output | | Bank B outputs. LVCMOS / LVTTL interface levels. |
| 30, 34 | $V_{DDOB}$ | Power | | Output Bank B power supply pins. |
| 37, 39, 41, 43 | QA3, QA2, QA1, QA0 | Output | | Bank A outputs. LVCMOS / LVTTL interface levels. |
| 38, 42 | $V_{DDOA}$ | Power | | Output Bank A power supply pins. |
| 45 | CLK_SEL | Input | Pulldown | Clock select input. When HIGH, selects CLK1, nCLK1 inputs. When LOW, selects CLK0 input. LVCMOS / LVTTL interface levels. |
| 46 | nCLK1 | Input | Pullup | Inverting differential clock input. |
| 47 | CLK1 | Input | Pulldown | Non-inverting differential clock input. |

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**TABLE 2. PIN CHARACTERISTICS**

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | | 4 | | pF |
| $R_{PULLUP}$ | Input Pullup Resistor | | | 51 | | kΩ |
| $C_{PD}$ | Power Dissipation Capacitance (per output); NOTE 1 | $V_{DD}$, $V_{DDOx}$ = 3.465V | | | 18 | pF |
| | | $V_{DD}$ = 3.465, $V_{DDOx}$ = 2.625V | | | 20 | pF |
| | | $V_{DD}$ = 3.465, $V_{DDOx}$ = 1.89V | | | 30 | pF |
| $R_{OUT}$ | Output Impedance | | | 7 | | Ω |

NOTE 1: $V_{DDOx}$ denotes $V_{DDOA}$, $V_{DDOB}$, $V_{DDOC}$, and $V_{DDOD}$.

**TABLE 3. FUNCTION TABLE**

| Inputs | | | Outputs | |
|---|---|---|---|---|
| nMR/OE | CLK_ENx | DIV_SELx | Bank X | Qx Frequency |
| 0 | X | X | Hi Z | N/A |
| 1 | 1 | 0 | Active | fIN/2 |
| 1 | 1 | 1 | Active | fIN |
| 1 | 0 | X | Low | N/A |

### Absolute Maximum Ratings

| | |
|---|---|
| Supply Voltage, $V_{DD}$ | 4.6V |
| Inputs, $V_I$ | -0.5V to $V_{DD}$ + 0.5 V |
| Outputs, $V_O$ | -0.5V to $V_{DDOx}$ + 0.5V |
| Package Thermal Impedance, $\theta_{JA}$ | 47.9°C/W (0 lfpm) |
| Storage Temperature, $T_{STG}$ | -65°C to 150°C |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**Table 4A. Power Supply DC Characteristics,** $V_{DD}$ = 3.3V±5%, TA = 0°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Positive Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{DDOx}$ | Output Supply Voltage; NOTE 1 | | 3.135 | 3.3 | 3.465 | V |
| | | | 2.375 | 2.5 | 2.625 | V |
| | | | 1.71 | 1.8 | 1.89 | V |
| $I_{DD}$ | Power Supply Current | | | | 100 | mA |
| $I_{DDOx}$ | Output Supply Current; NOTE 2 | | | | 15 | mA |

NOTE 1: $V_{DDOx}$ denotes $V_{DDOA}$, $V_{DDOB}$, $V_{DDOC}$, and $V_{DDOD}$. NOTE 2: $I_{DDOx}$ denotes $I_{DDOA}$, $I_{DDOB}$, $I_{DDOC}$, and $I_{DDOD}$.

**Table 4B. LVCMOS/LVTTL DC Characteristics,** $V_{DD}$ = 3.3V±5%, TA = 0°C to 85°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | **DIV_SELA:DIV_SELD, CLK_ENA:CLK_END, nMR/OE, CLK_SEL** | | 2 | | V + 0.3 | V |
| | | **CLK0** | | 2 | | V + 0.3 | V |
| $V_{IL}$ | Input Low Voltage | **DIV_SELA:DIV_SELD, CLK_ENA:CLK_END, nMR/OE, CLK_SEL** | | -0.3 | | 0.8 | V |
| | | **CLK0** | | -0.3 | | 1.3 | V |
| $I_{IH}$ | **Input High Current** | **CLK_ENA:CLK_END, DIV_SELA:DIV_SELD, nMR/OE** | V = V = 3.465V | | | 5 | µA |
| | | **CLK0, CLK_SEL** | V = V = 3.465V | | | 150 | µA |
| $I_{IL}$ | Input Low Current | **CLK_ENA:CLK_END, DIV_SELA:DIV_SELD, nMR/OE** | V = 3.465V, V = 0V | -150 | | | µA |
| | | **CLK0, CLK_SEL** | V = 3.465V, V = 0V | -5 | | | µA |
| $V_{OH}$ | **Output High Voltage; NOTE 1** | | V = 3.3V ± 5%; NOTE 2 | 2.6 | | | V |
| | | | V = 2.5V ± 5%; NOTE 2 | 1.8 | | | V |
| | | | V = 1.8V ± 5%; NOTE 2 I = -2mA | $V_{DDOx}$ - 0.45 | | | V |
| $V_{OL}$ | **Output Low Voltage; NOTE 1** | | V = 3.3V ± 5%; NOTE 2 | | | 0.5 | V |
| | | | V = 2.5V ± 5%; NOTE 2 | | | 0.5 | V |
| | | | V = 1.8V ± 5%; NOTE 2 I = 2mA | | | 0.45 | V |
| $I_{OZL}$ | **Output Tristate Current Low** | | | -5 | | | µA |
| $I_{OZH}$ | **Output Tristate Current High** | | | | | 5 | µA |

NOTE 1: Outputs terminated with 50W to $V_{DDOX}$/2. See Parameter Measurement Information, Output Load Test Circuit.
NOTE 2: $V_{DDOx}$ denotes $V_{DDOA}$, $V_{DDOB}$, $V_{DDOC}$ and $V_{DDOD}$.

**TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS,** $V_{DD}$ = 3.3V±5%, $T_A$ = 0°C TO 85°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $I_{IH}$ | Input High Current | nCLK1 | $V_{IN} = V_{DD}$ = 3.465V | | | 5 | µA |
| | | CLK1 | $V_{IN} = V_{DD}$ = 3.465V | | | 150 | µA |
| $I_{IL}$ | Input Low Current | nCLK1 | $V_{IN}$ = 0V, $V_{DD}$ = 3.465V | -150 | | | µA |
| | | CLK1 | $V_{IN}$ = 0V, $V_{DD}$ = 3.465V | -5 | | | µA |
| $V_{PP}$ | Peak-to-Peak Input Voltage | | | 0.15 | | 1.3 | V |
| $V_{CMR}$ | Common Mode Input Voltage; NOTE 1, 2 | | | GND + 0.5 | | $V_{DD}$ - 0.85 | V |

NOTE 1: For single ended applications, the maximum input voltage for CLK1, nCLK1 is $V_{DD}$ + 0.3V.
NOTE 2: Common mode voltage is defined as $V_{IH}$.

**TABLE 5A. AC CHARACTERISTICS,** $V_{DD} = V_{DDOx}$ = 3.3V±5%, $T_A$ = 0°C TO 85°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $f_{MAX}$ | Output Frequency | | | | | 250 | MHz |
| $tp_{LH}$ | Propagation Delay, Low to High | CLK0; NOTE 1A | | 2.8 | 3.2 | 3.7 | ns |
| | | CLK1, nCLK1; NOTE 1B | | 2.9 | 3.4 | 3.9 | ns |
| *t*sk(b) | Bank Skew; NOTE 2, 7 | | Measured on the Rising Edge | | | 30 | ps |
| *t*sk(o) | Output Skew; NOTE 3, 7 | | Measured on the Rising Edge | | | 150 | ps |
| *t*sk(pp) | Part-to-Part Skew; NOTE 5, 7 | | | | | 750 | ps |
| $t_R$ / $t_F$ | Output Rise/Fall Time; NOTE 6 | | 20% to 80% | 200 | | 700 | ps |
| odc | Output Duty Cycle | | f < 175MHz | 45 | | 55 | % |
| | | | f ≥ 175MHz | 40 | | 60 | % |
| $t_{EN}$ | Output Enable Time; NOTE 6 | | | | | 10 | ns |
| $t_{DIS}$ | Output Disable Time; NOTE 6 | | | | | 10 | ns |

All parameters measured at 250MHz unless noted otherwise.
NOTE 1A: Measured from the $V_{DD}$/2 of the input to $V_{DDOX}$/2 of the output.
NOTE 1B: Measured from the differential input crossing point to $V_{DDOX}$/2 of the output.
NOTE 2: Defined as skew within a bank with equal load conditions.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDOX}$/2.
NOTE 4: Defined as skew across banks of outputs switching in the same direction operating at different frequencies with the same supply voltages and equal load conditions. Measured at $V_{DDOX}$/2.
NOTE 5: Defined as skew between outputs on different devices operating a the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDOX}$/2.
NOTE 6: These parameters are guaranteed by characterization. Not tested in production.
NOTE 7: This parameter is defined in accordance with JEDEC Standard 65.

**TABLE 5B. AC CHARACTERISTICS,** $V_{DD}$ = 3.3V±5%, $V_{DDOx}$ = 2.5V±5%, $T_A$ = 0°C TO 85°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $f_{MAX}$ | Output Frequency | | | | | 250 | MHz |
| $tp_{LH}$ | Propagation Delay, Low to High | CLK0; NOTE 1A | | 2.9 | 3.3 | 3.8 | ns |
| | | CLK1, nCLK1; NOTE 1B | | 3 | 3.5 | 4 | ns |
| *t*sk(b) | Bank Skew; NOTE 2, 7 | | Measured on the Rising Edge | | | 30 | ps |
| *t*sk(o) | Output Skew; NOTE 3, 7 | | Measured on the Rising Edge | | | 160 | ps |
| *t*sk(pp) | Part-to-Part Skew; NOTE 5, 7 | | | | | 750 | ps |
| $t_R$ / $t_F$ | Output Rise/Fall Time; NOTE 6 | | 20% to 80% | 200 | | 700 | ps |
| odc | Output Duty Cycle | | f < 175MHz | 45 | | 55 | % |
| | | | f ≥ 175MHz | 40 | | 60 | % |
| $t_{EN}$ | Output Enable Time; NOTE 6 | | | | | 10 | ns |
| $t_{DIS}$ | Output Disable Time; NOTE 6 | | | | | 10 | ns |

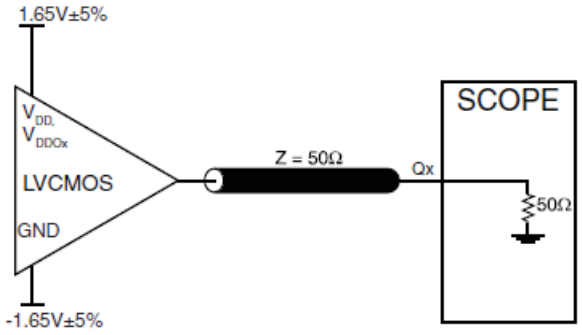
All parameters measured at 250MHz unless noted otherwise.
NOTE 1A: Measured from the $V_{DD}$/2 of the input to $V_{DDOX}$/2 of the output.
NOTE 1B: Measured from the differential input crossing point to $V_{DDOX}$/2 of the output.
NOTE 2: Defined as skew within a bank with equal load conditions.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDOX}$/2.
NOTE 4: Defined as skew across banks of outputs switching in the same direction operating at different frequencies with the same supply voltages and equal load conditions. Measured at $V_{DDOX}$/2.
NOTE 5: Defined as skew between outputs on different devices operating a the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDOX}$/2.
NOTE 6: These parameters are guaranteed by characterization. Not tested in production.
NOTE 7: This parameter is defined in accordance with JEDEC Standard 65.

**TABLE 5C. AC CHARACTERISTICS,** $V_{DD}$ = 3.3V±5%, $V_{DDOx}$ = 1.8V±5%, $T_A$ = 0°C TO 85°C

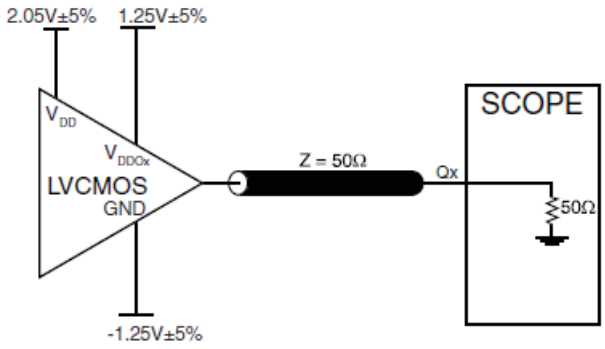
| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $f_{MAX}$ | Output Frequency | | | | | 250 | MHz |
| $tp_{LH}$ | Propagation Delay, Low to High | CLK0; NOTE 1A | | 3.1 | 3.8 | 4.5 | ns |
| | | CLK1, nCLK1; NOTE 1B | | 3.1 | 3.8 | 4.5 | ns |
| *t*sk(b) | Bank Skew; NOTE 2, 7 | | Measured on the Rising Edge | | | 30 | ps |
| *t*sk(o) | Output Skew; NOTE 3, 7 | | Measured on the Rising Edge | | | 170 | ps |
| *t*sk(pp) | Part-to-Part Skew; NOTE 5, 7 | | | | | 750 | ps |
| $t_R$ / $t_F$ | Output Rise/Fall Time; NOTE 6 | | 20% to 80% | 200 | | 700 | ps |
| odc | Output Duty Cycle | | f < 175MHz | 45 | | 55 | % |
| | | | f ≥ 175MHz | 40 | | 60 | % |
| $t_{EN}$ | Output Enable Time; NOTE 6 | | | | | 10 | ns |
| $t_{DIS}$ | Output Disable Time; NOTE 6 | | | | | 10 | ns |

All parameters measured at 250MHz unless noted otherwise.
NOTE 1A: Measured from the $V_{DD}$/2 of the input to $V_{DDOX}$/2 of the output.
NOTE 1B: Measured from the differential input crossing point to $V_{DDOX}$/2 of the output.
NOTE 2: Defined as skew within a bank with equal load conditions.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDOX}$/2.
NOTE 4: Defined as skew across banks of outputs switching in the same direction operating at different frequencies with the same supply voltages and equal load conditions. Measured at $V_{DDOX}$/2.
NOTE 5: Defined as skew between outputs on different devices operating a the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDOX}$/2.
NOTE 6: These parameters are guaranteed by characterization. Not tested in production.
NOTE 7: This parameter is defined in accordance with JEDEC Standard 65.

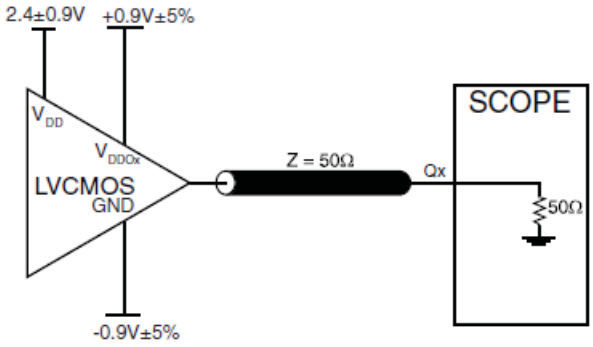
# PARAMETER MEASUREMENT INFORMATION



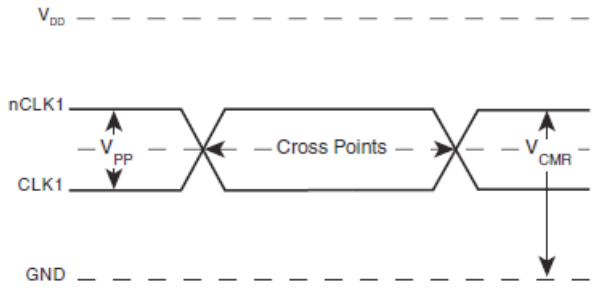

3.3V OUTPUT LOAD AC TEST CIRCUIT



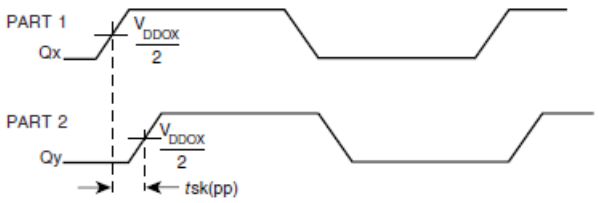

3.3V/2.5V OUTPUT LOAD AC TEST CIRCUIT



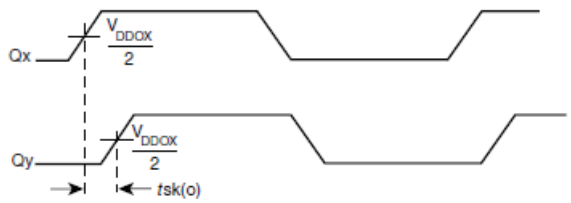

3.3V/1.8V OUTPUT LOAD AC TEST CIRCUIT



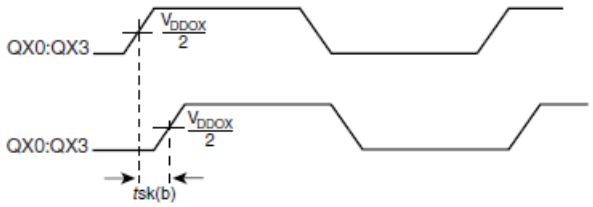

DIFFERENTIAL INPUT LEVEL



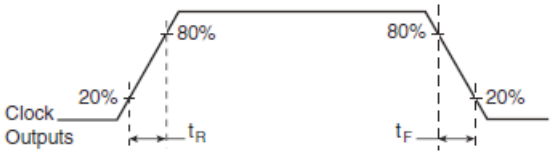

PART-TO-PART SKEW



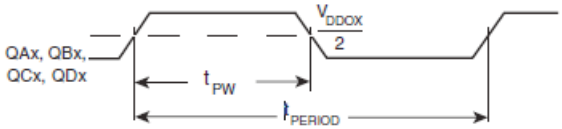

OUTPUT SKEW




**BANK SKEW (where X denotes outputs in the same bank)**

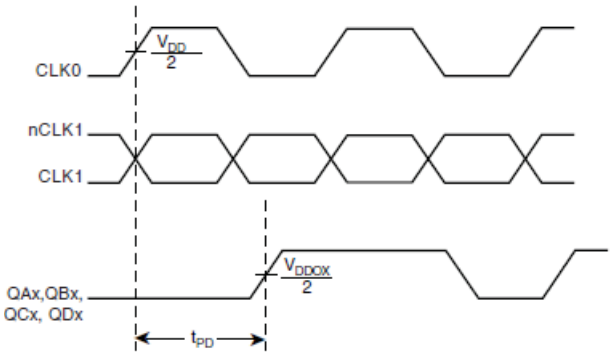



**OUTPUT RISE/FALL TIME**




$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

**OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD**




**PROPAGATION DELAY**

# Application Information

## Wiring the Differential Input to Accept Single Ended Levels

*Figure 1* shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = $V_{DD}$/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and $V_{DD}$ = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

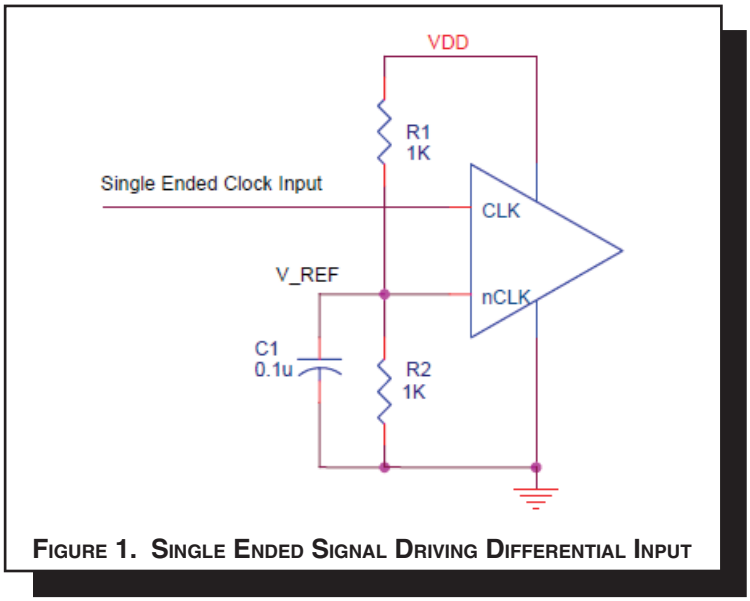



**Figure 1. Single Ended Signal Driving Differential Input**

## Recommendations for Unused Input and Output Pins

### Inputs:

#### CLK Input:

For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the CLK input to ground.

#### CLK/nCLK Input:

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

#### LVCMOS Control Pins:

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

### Outputs:

#### LVCMOS Output:

All unused LVCMOS output can be left floating. We recommend that there is no trace attached.

## Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both $V_{SWING}$ and $V_{OH}$ must meet the $V_{PP}$ and $V_{CMR}$ input requirements. Figures 4A to 4E show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 2A,* the input termination applies for LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

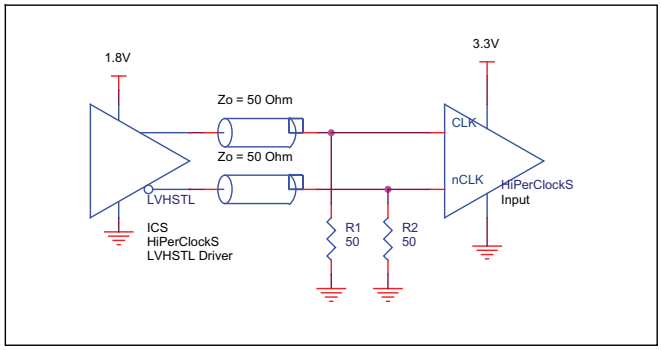



**Figure 2A. CLK/nCLK Input Driven by LVHSTL Driver**

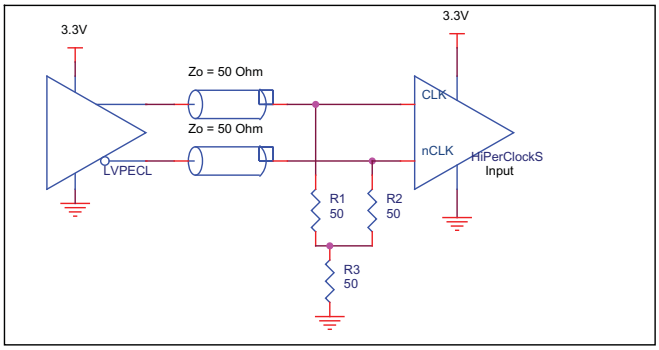



**Figure 2B. CLK/nCLK Input Driven by 3.3V LVPECL Driver**

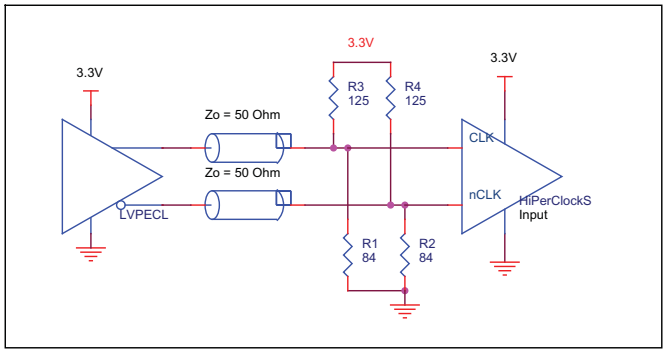



**Figure 2C. CLK/nCLK Input Driven by 3.3V LVPECL Driver**

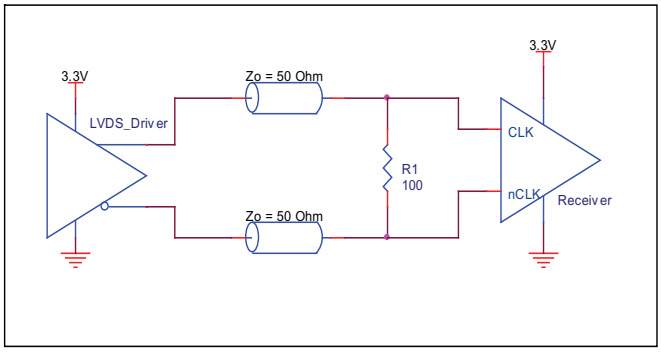



**Figure 2D. CLK/nCLK Input Driven by 3.3V LVDS Driver**

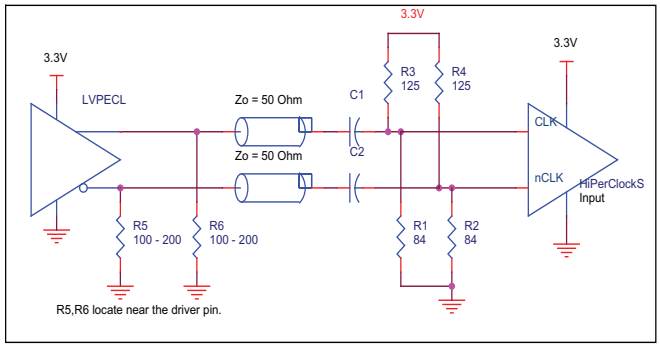



**Figure 2E. CLK/nCLK Input Driven by 3.3V LVPECL Driver with AC Couple**

## Schematic Example

*Figure 3* shows an application schematic example of the 87016. This schematic provides examples of input and output handling. The differential CLK1/nCLK1 input can accept various types of differential signal. This example shows the 87016 input driven by a 3.3V LVPECL driver. Additional examples for the input driven by other types of drivers are shown in the application section of this data sheet. The single ended input CLK0 is driven by a 7Ω LVMCOS driver through series termination. The 87016 outputs are LVCMOS drivers. Series termination is shown in this schematic. Additional LVCMOS termination approaches are shown in the LVCMOS Termination Application Note.

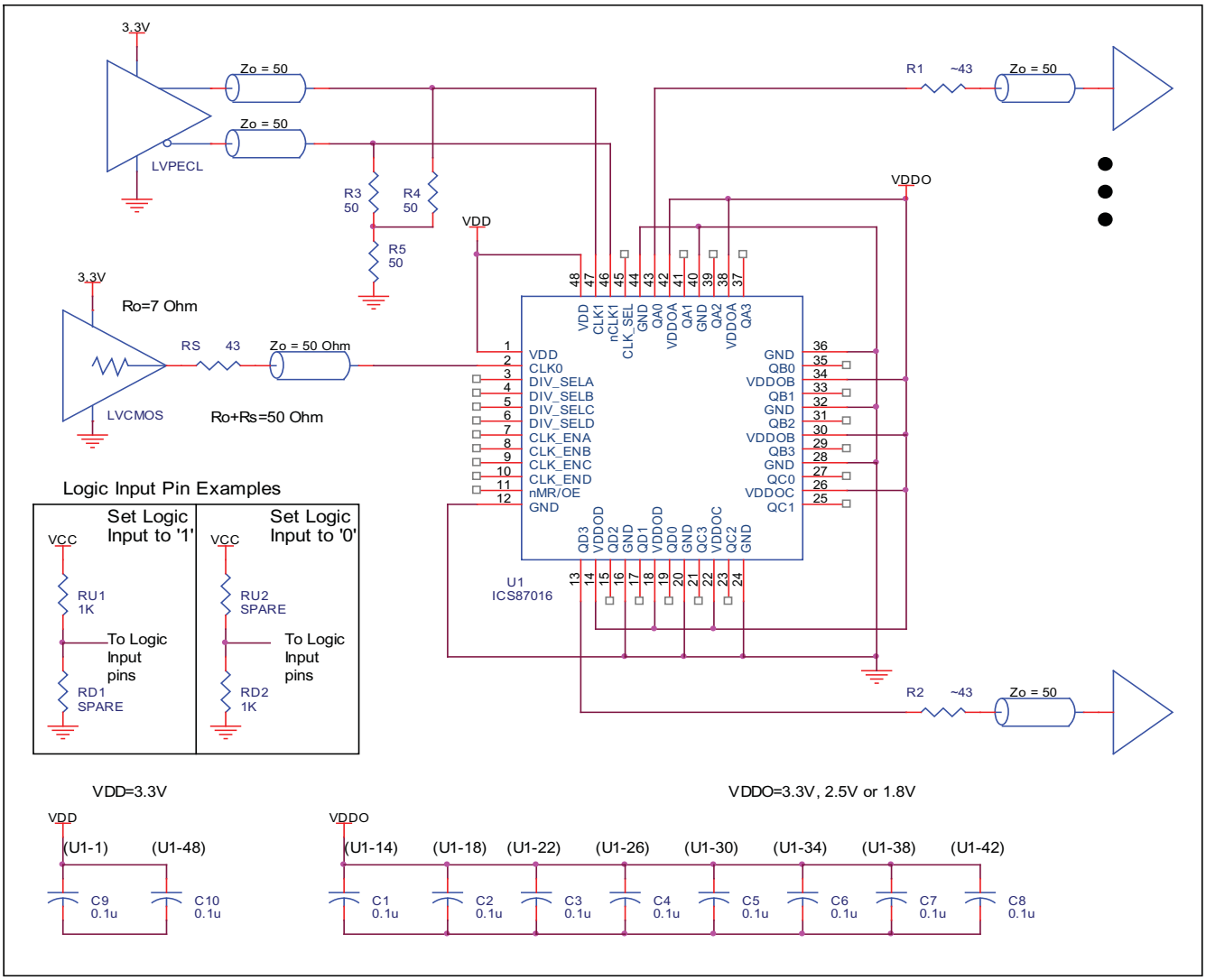



**Figure 3. Application Schematic Example**

# Reliability Information

**Table 6. $\theta_{JA}$ vs. Air Flow Table for 48 Lead LQFP**

| $\theta_{JA}$ by Velocity (Linear Feet per Minute) | 0 | 200 | 500 |
|---|---|---|---|
| Single-Layer PCB, JEDEC Standard Test Boards | 67.8°C/W | 55.9°C/W | 50.1°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 47.9°C/W | 42.1°C/W | 39.4°C/W |

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

### Transistor Count

The transistor count for 87016 is: 2034

## Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

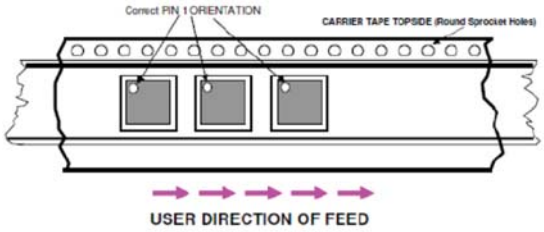
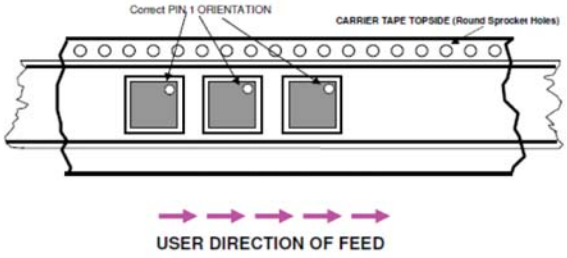
www.idt.com/us/en/document/cpt/prprg-package-outline-70-x-70-x-14-mm-tqfp-10010-form

**TABLE 8. ORDERING INFORMATION**

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|---|---|---|---|---|
| 87016AYLF | ICS87016AYLF | 48 Lead “Lead-Free” LQFP | tray | 0°C to 85°C |
| 87016AYLFT | ICS87016AYLF | 48 Lead “Lead-Free” LQFP | tape & reel, pin 1 orientation: EIA-481-C | 0°C to 85°C |
| 87016AYLF/W | ICS87016AYLF | 48 Lead “Lead-Free” LQFP | tape & reel, pin 1 orientation EIA-481-D | 0°C to 85°C |

NOTE: Parts that are ordered with an “LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

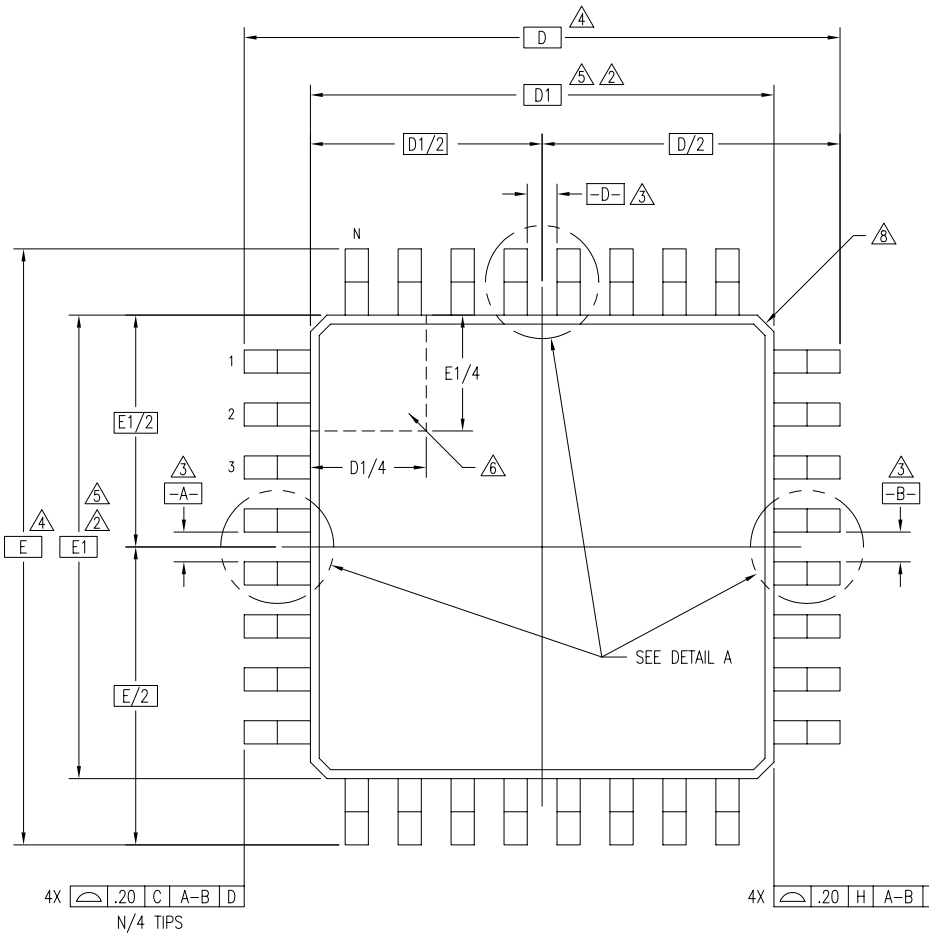
**TABLE 9. PIN 1 ORIENTATION IN TAPE AND REEL PACKAGING**

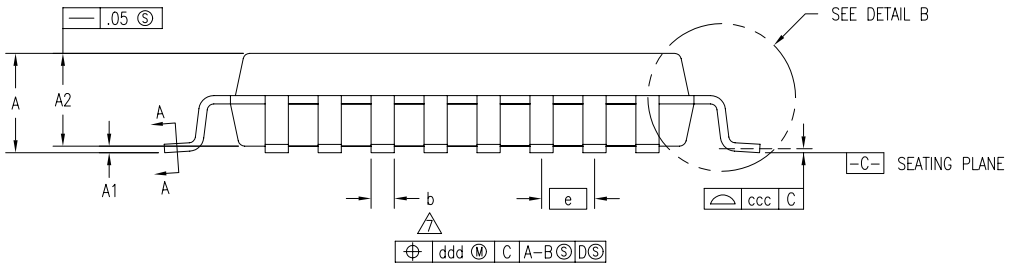
| Part Number Suffix | Pin 1 Orientation | Illustration |
|---|---|---|
| 8 | Quadrant 1 (EIA-481-C) |   |
| W | Quadrant 2 (EIA-481-D) |   |

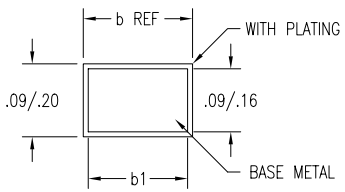
**REVISION HISTORY SHEET**

| Rev | Table | Page | Description of Change | Date |
|---|---|---|---|---|
| A | T5A, T5B, T5C | 6, 7, 8 | AC Characteristics Table - corrected the first line in the Notes section, from "All parameters measured at 150MHz..." to 250MHz. | 7/31/02 |
| A | | | Revised part description title from "Differential-to-LVCMOS Clock Generator" to "LVCMOS Clock Generator". | 8/9/02 |
| A | T5A & T5B | 6 & 7<br><br>12 | AC Characteristics Table - switched prop delay values for CLK0 and CLK1, nCLK1.<br>Added Differential Clock Input Interface section.<br>Updated format. | 5/05/03 |
| A | | 1 | Modified Block Diagram, corrected latch block. | 6/4/03 |
| A | | 12 | Added Schematic Example | 12/10/04 |
| A | <br><br><br>T8 | 1<br>10<br><br>15 | Features Section - added Lead-Free bullet.<br>Application Section - added *Recommendations for Unused Input and Output Pins.*<br>Ordering Information Table - add Lead-Free part number, marking and note. | 2/28/06 |
| A | T8 | <br>15<br>17 | Updated datasheet's header/footer with IDT from ICS.<br>Removed ICS prefix from Part/Order Number column.<br>Added Contact Page. | 7/29/10 |
| B | T4B | 4 | LVCMOS DC Characteristics Table - corrected typo for 1.8V $V_{OH}$ min. spec from $V_{DD}$ - 0.45 to $V_{DDOx}$ - 0.45. | 4/4/13 |
| C | <br><br>T8 | <br>1<br>15 | Updated datasheet format.<br>Features section - removed reference to leaded device.<br>Ordering Information - removed leaded devices - PDN CQ-13-02. | 1/12/15 |
| C | T9 | 15 | Added Pin 1 Orientation in Tape and Reel Packaging Table. | 6/26/15 |
| | | | Updated Package Outline Drawings section; added link. | 01/21/20 |

| REVISIONS | | | |
|---|---|---|---|
| REV | DESCRIPTION | DATE | APPROVED |
| 00 | INITIAL RELEASE | 10/15/95 | TU VU |
| 01 | ADD "GREEN" PRG NOMENCLATURE | 10/08/04 | TU VU |
| 02 | ADDED 48 LEAD | 10/13/06 | PKP |
| 03 | ADDED PACKAGE CODE | 12/12/12 | RC |

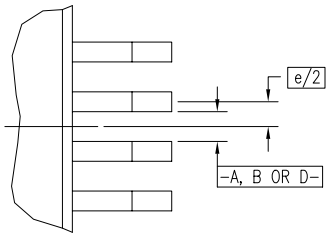


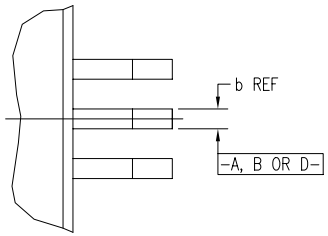




SECTION A-A

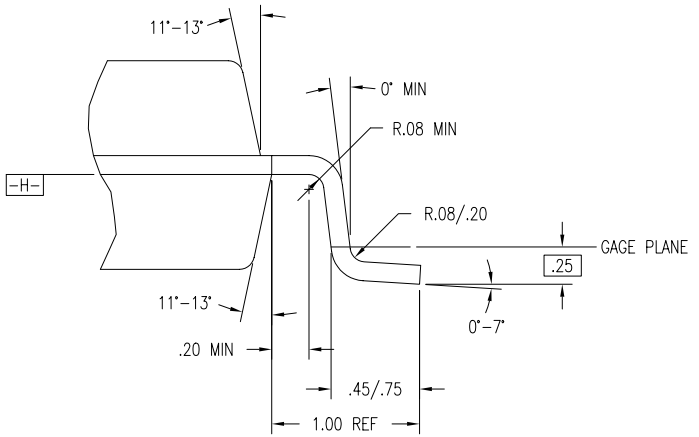
EVEN LEAD SIDES




ODD LEAD SIDES




DETAIL A




DETAIL B

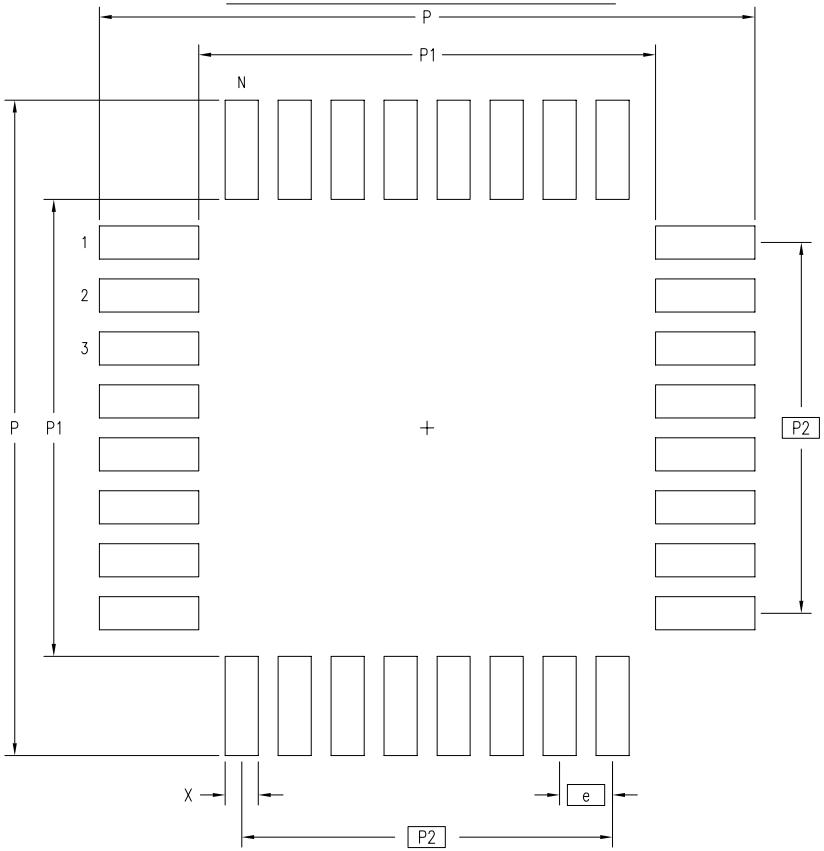
| | | | |
|---|---|---|---|
| TOLERANCES UNLESS SPECIFIED<br>DECIMAL ANGULAR<br>XX± ±<br>XXX±<br>XXXX± | IDT™ www.IDT.com | 6024 Silver Creek Valley Rd<br>San Jose, CA 95138<br>PHONE: (408) 284-8200<br>FAX: (408) 284-3572 | |
| APPROVALS | DATE | TITLE: PR/PRG PACKAGE OUTLINE<br>7.0 X 7.0 X 1.4 mm TQFP<br>1.00/.10 FORM | |
| DRAWN TU | 10/15/95 | | |
| CHECKED | | | |
| | | SIZE: C | DRAWING No.: PSC-4052 |
| | | REV: 03 | |
| | | DO NOT SCALE DRAWING | SHEET 1 OF 2 |

| REVISIONS | | | |
|---|---|---|---|
| REV | DESCRIPTION | DATE | APPROVED |
| 00 | INITIAL RELEASE | 10/15/95 | TU VU |
| 01 | ADD "GREEN" PRG NOMENCLATURE | 10/08/04 | TU VU |
| 02 | ADDED 48 LEAD | 10/13/06 | PKP |
| 03 | ADDED PACKAGE CODE | 12/12/12 | RC |

| PR/PRG32 | | | | |
|---|---|---|---|---|
| SYMBOL | JEDEC VARIATION BBA | | | NOTE |
| | MIN | NOM | MAX | |
| A | – | – | 1.60 | |
| A1 | .05 | .10 | .15 | |
| A2 | 1.35 | 1.40 | 1.45 | |
| D | 9.00 BSC | | | 4 |
| D1 | 7.00 BSC | | | 5,2 |
| E | 9.00 BSC | | | 4 |
| E1 | 7.00 BSC | | | 5,2 |
| N | 32 | | | |
| e | .80 BSC | | | |
| b | .30 | .37 | .45 | 7 |
| b1 | .30 | .35 | .40 | |
| ccc | – | – | .10 | |
| ddd | – | – | .20 | |

| PR/PRG48 | | | | |
|---|---|---|---|---|
| SYMBOL | JEDEC VARIATION BBC | | | NOTE |
| | MIN | NOM | MAX | |
| A | – | – | 1.60 | |
| A1 | .05 | .10 | .15 | |
| A2 | 1.35 | 1.40 | 1.45 | |
| D | 9.00 BSC | | | 4 |
| D1 | 7.00 BSC | | | 5,2 |
| E | 9.00 BSC | | | 4 |
| E1 | 7.00 BSC | | | 5,2 |
| N | 48 | | | |
| e | .50 BSC | | | |
| b | .17 | .22 | .27 | 7 |
| b1 | .17 | .20 | .23 | |
| ccc | – | – | .08 | |
| ddd | – | – | .08 | |

## LAND PATTERN DIMENSIONS




| | MIN | MAX |
|---|---|---|
| P | 9.80 | 10.00 |
| P1 | 6.80 | 7.00 |
| P2 | 5.60 BSC | |
| X | .40 | .60 |
| e | .80 BSC | |
| N | 32 | |

| | MIN | MAX |
|---|---|---|
| P | 9.80 | 10.00 |
| P1 | 6.80 | 7.00 |
| P2 | 5.50 BSC | |
| X | .25 | .35 |
| e | .50 BSC | |
| N | 48 | |

## NOTES:

1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1982

2 TOP PACKAGE MAY BE SMALLER THAN BOTTOM PACKAGE BY .15 mm

3 DATUMS A–B AND –D– TO BE DETERMINED AT DATUM PLANE –H–

4 DIMENSIONS D AND E ARE TO BE DETERMINED AT SEATING PLANE –C–

5 DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS .25 mm PER SIDE. D1 AND E1 ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH

6 DETAILS OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED

7 DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

8 EXACT SHAPE OF EACH CORNER IS OPTIONAL

9 THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP

10 ALL DIMENSIONS ARE IN MILLIMETERS

11 THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS–026, VARIATIONS BBA & BBC.

TOLERANCES UNLESS SPECIFIED
DECIMAL XX± XXX± XXXX± ANGULAR ±


IDT™ www.IDT.com
6024 Silver Creek Valley Rd
San Jose, CA 95138
PHONE: (408) 284–8200
FAX: (408) 284–3572


| APPROVALS | DATE |
|---|---|
| DRAWN TU | 10/15/95 |
| CHECKED | |

TITLE: PR/PRG PACKAGE OUTLINE 7.0 X 7.0 X 1.4 mm TQFP 1.00/.10 FORM

| SIZE | DRAWING No. | REV |
|---|---|---|
| C | PSC–4052 | 03 |

DO NOT SCALE DRAWING | SHEET 2 OF 2

## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)


### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com


### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

# X-ON Electronics

Largest Supplier of Electrical and Electronic Components

***Click to view similar products for*** Clock Generators & Support Products ***category:***

***Click to view products by*** Renesas ***manufacturer:***

Other Similar products are found below :

CV183-2TPAG 950810CGLF 9DBV0741AKILF 9VRS4420DKLF CY25404ZXI226 CY25422SXI-004 MPC9893AE NB3H5150-01MNTXG PL602-20-K52TC ICS557GI-03LF PI6LC48P0101LIE 82P33814ANLG 840021AGLF ZL30244LFG7 PI6LC48C21LE ZL30245LFG7 PI6LC48P0405LIE PI6LC48P03LE MAX24505EXG+ ZL30163GDG2 5L1503L-000NVGI8 ZL30156GGG2 ZL30673LFG7 MAX24188ETK2 ZL30152GGG2 5L1503-000NVGI8 PI6C557-01BZHIEX PI6LC48C21LIE CY2542QC002 5P35023-106NLGI 5X1503L-000NLGI8 ZL30121GGG2V2 ZL30282LDG1 ZL30102QDG1 ZL30159GGG2 DS1070K ZL30145GGG2 ZL30312GKG2 MAX24405EXG2 ZL30237GGG2 SY100EL34LZG 9FGV1002BQ506LTGI AD9518-4ABCPZ MX852BB0030 PI6LC4840ZHE AD9516-0BCPZ-REEL7 AD9574BCPZ-REEL7 PL602-21TC-R ZL30105QDG1 ZL30100QDG1