General Description

The 871002I-02 is a high performance Jitter Attenuator designed for use in PCI Express™ systems. In some PCI Express systems, such as those found in desktop PCs, the PCI Express clocks are generated from a low bandwidth, high phase noise PLL frequency synthesizer. In these systems, a jitter attenuator may be required to attenuate high frequency random and deterministic jitter components from the PLL synthesizer and from the system board. The 871002I-02 has two PLL bandwidth modes: 350kHz and 2200kHz. The 350kHz mode provides the maximum jitter attenuation, but it also results in higher PLL tracking time. In this mode, the spread spectrum modulation may also be attenuated. The 2200kHz bandwidth provides the best tracking skew and will pass most spread profiles, but the jitter attenuation will not be as good as the lower bandwidth modes. The 871002I-02 can be set for different modes using the F_SELx pins as shown in Table 3C.

The 871002I-02 uses IDT 3rd Generation FemtoClock™ PLL technology to achieve the lowest possible phase noise. The device is packaged in a small 20 Lead TSSOP package, making it ideal for use in space constrained applications such as PCI Express add-in cards.

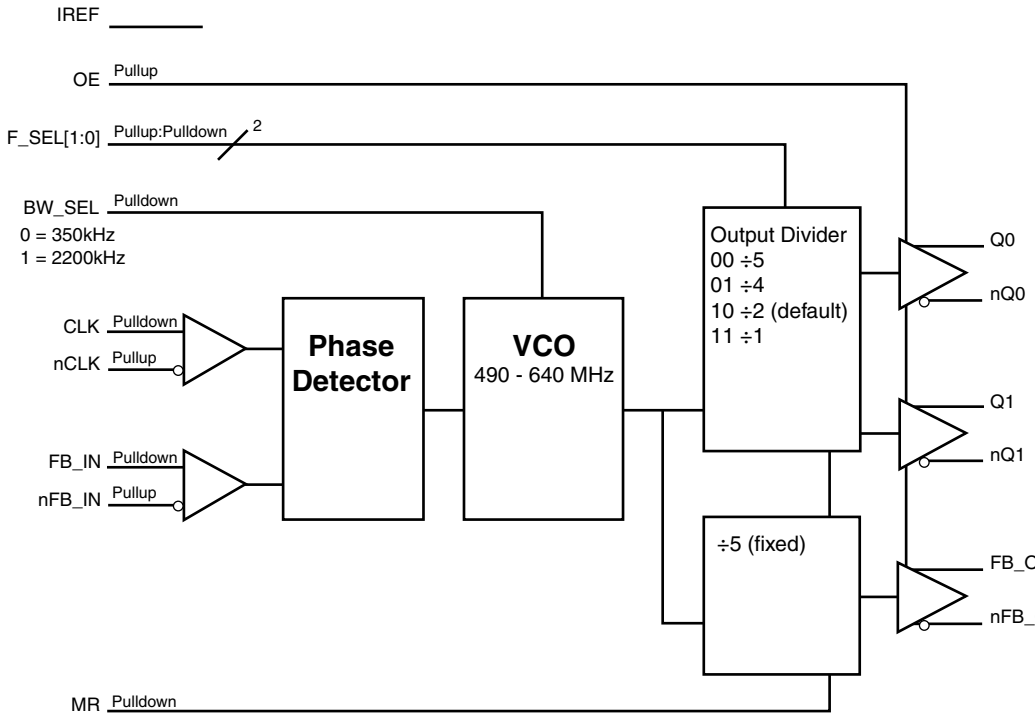
PLL Bandwidth (typical) Table

BW_SEL
0 = PLL Bandwidth: ~350kHz (default)
1 = PLL Bandwidth: ~2200kHz

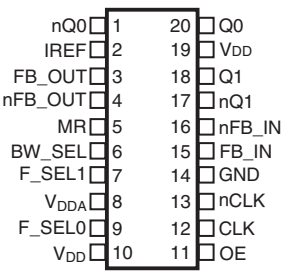
Features

- Two 0.7V HCSL differential output pairs
- One differential clock input
- CLK, nCLK can accept the following differential input levels: LVPECL, LVDS, HSTL, HCSL, SSTL
- Input frequency range: 98MHz to 128MHz
- Output frequency range: 98MHz to 640MHz
- VCO range: 490MHz - 640MHz
- Cycle-to-cycle jitter: 45ps (maximum)
- Two bandwidth modes allow the system designer to make jitter attenuation/tracking skew design trade-offs
- Full 3.3V supply mode
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Block Diagram



Pin Assignment



871002I-02
20-Lead TSSOP
6.5mm x 4.4mm x 0.925mm package body
G Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 20	nQ0, nQ0	Output		Differential output pair. HCSL interface levels.
2	IREF	Input		A fixed precision resistor (475Ω) from this pin to ground provides a reference current used for differential current-mode Qx/nQx clock outputs.
3, 4	FB_OUT, nFB_OUT	Output		Differential feedback output pair. HCSL interface levels.
5	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs (Qx, FB_OUT) to go low and the inverted outputs (nQx, nFB_OUT) to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
6	BW_SEL	Input	Pulldown	PLL Bandwidth select input. 0 = 350kHz, 1 = 2200kHz. See Table 3B.
7, 9	F_SEL1, F_SEL0	Input	Pullup Pulldown	Frequency select pins. See Table 3C. LVCMOS/LVTTL interface levels
8	V_{DDA}	Power		Analog supply pin.
10, 19	V_{DD}	Power		Core supply pins.
11	OE	Input	Pullup	Output enable pin. When HIGH, the outputs are active. When LOW, the outputs are in a high impedance state. LVCMOS/LVTTL interface levels. See Table 3A.
12	CLK	Input	Pulldown	Non-inverting differential clock input.
13	nCLK	Input	Pullup	Inverting differential clock input.
14	GND	Power		Power supply ground.
15	FB_IN	Input	Pulldown	Non-inverting differential feedback clock input.
16	nFB_IN	Input	Pullup	Inverting differential feedback clock input.
17, 18	nQ1, Q1	Output		Differential output pair. HCSL interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Function Tables

Table 3A. Output Enable Function Table

Input	Outputs	
OE	**Q[1:0], nQ[1:0]**	**FB_OUT, nFB_OUT**
0	High-Impedance	Enabled
1 (default)	Enabled	Enabled

Table 3B. PLL Bandwidth Control Table

Input	
BW_SEL	**PLL Bandwidth**
0	350kHz (default)
1	2200kHz

Table 3C. F_SELx Function Table

Input Frequency (MHz)	Inputs			Output Frequency (MHz)
	F_SEL1	**F_SEL0**	**Divider**	
100	0	0	÷5	100
100	0	1	÷4	125
100	1	0	÷2	250 (default)
100	1	1	÷1	500

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA}	86.7°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. LVDS Power Supply DC Characteristics, V_{DD} = 3.3V ± 10%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.97	3.3	3.63	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.12	3.3	V_{DD}	V
I_{DD}	Power Supply Current				75	mA
I_{DDA}	Analog Supply Current				12	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V ± 10%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	OE, F_SEL1	V_{DD} = V_{IN} = 3.63V			5	µA
		BW_SEL, F_SEL0, MR	V_{DD} = V_{IN} = 3.63V			150	µA
I_{IL}	Input Low Current	OE, F_SEL1	V_{DD} = 3.63V, V_{IN} = 0V	-150			µA
		BW_SEL, F_SEL0, MR	V_{DD} = 3.63V, V_{IN} = 0V	-5			µA

Table 4C. Differential DC Characteristics, V_{DD} = 3.3V ± 10%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK, FB_IN	V_{DD} = V_{IN} = 3.465V			150	µA
		nCLK, nFB_IN	V_{DD} = V_{IN} = 3.465V			5	µA
I_{IL}	Input Low Current	CLK, FB_IN	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		nCLK, nFB_IN	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Voltage; NOTE 1			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} – 0.85	V

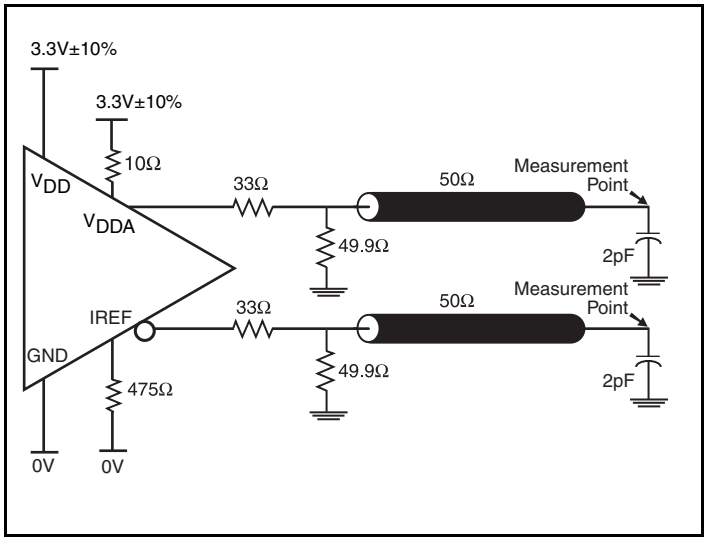
NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode input voltage is defined as V_{IH}.

Table 5. 0.7V HCSL Differential AC Characteristics, V_{DD} = 3.3V ± 10%, T_A = -40°C to 85°C

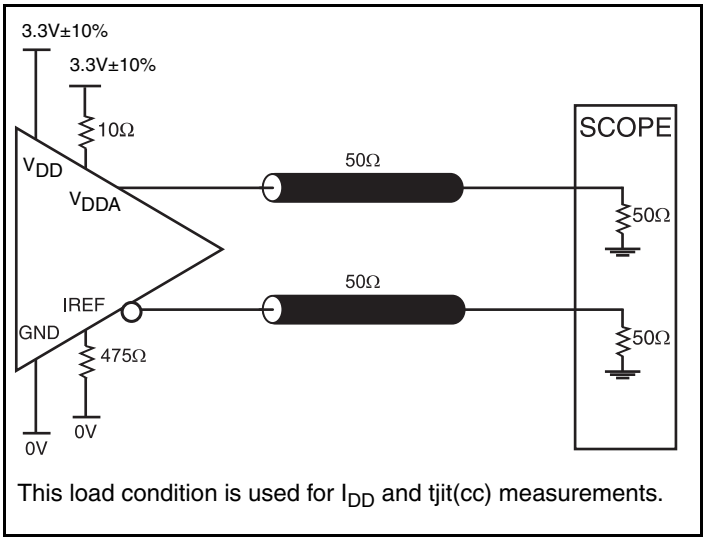
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency		98		640	MHz
t_{jit}(cc)	Cycle-to-Cycle Jitter; NOTE 1	PLL Mode			45	ps
V_{MAX}	Absolute Max. Output Voltage; NOTE 2, 3				1150	mV
V_{MIN}	Absolute Min. Output Voltage; NOTE 2, 4		-300			mV
V_{RB}	Ringback Voltage; NOTE 5, 6		-100		100	mV
V_{CROSS}	Absolute Crossing Voltage; NOTE 2, 7, 8		200		550	mV
ΔV_{CROSS}	Total Variation of V_{CROSS} over all edges; NOTE 2, 7, 9				140	mV
t_R / t_F	Output Rise/Fall Time	measured between -150mV to +150mV	0.6		4.75	V/ns
odc	Output Duty Cycle; NOTE 10		48		52	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: All parameters measured at f ≤ 250MHz unless noted otherwise.
NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 2: Measurement taken from single ended waveform.
NOTE 3: Defined as the maximum instantaneous voltage including overshoot. See Parameter Measurement Information Section.
NOTE 4: Defined as the minimum instantaneous voltage including undershoot. See Parameter Measurement Information Section.
NOTE 5: Measurement taken from differential waveform.
NOTE 6:T_{STABLE} is the time the differential clock must maintain a minimum ± 150mV differential voltage after rising/falling edges before it is allowed to drop back into the V_{RB} ±100mV differential range.
NOTE 7: Measured at crossing point where the instantaneous voltage value of the rising edge of Q equals the falling edge of nQ.
NOTE 8: Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
NOTE 9: Defined as the total variation of all crossing voltages of rising Q and falling nQ, This is the maximum allowed variance in Vcross for any particular system.
NOTE 10: Input duty cycle must be 50%.

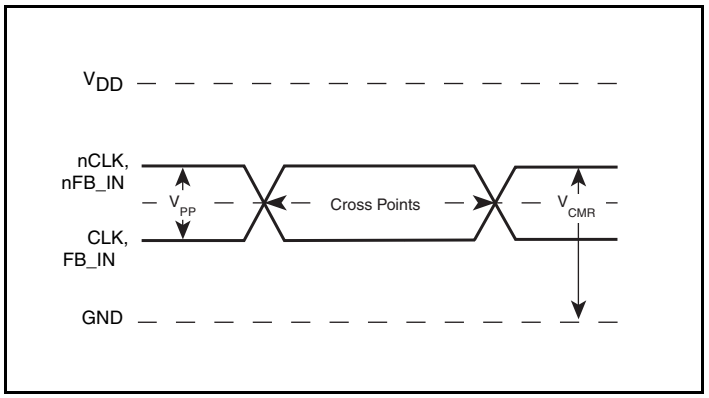
Parameter Measurement Information



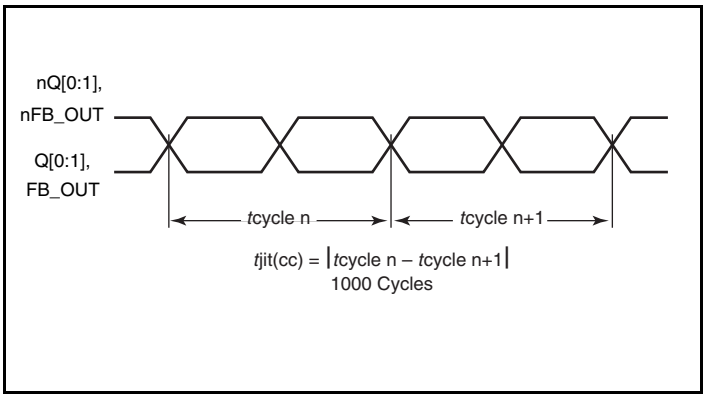
3.3V HCSL Output Load AC Test Circuit



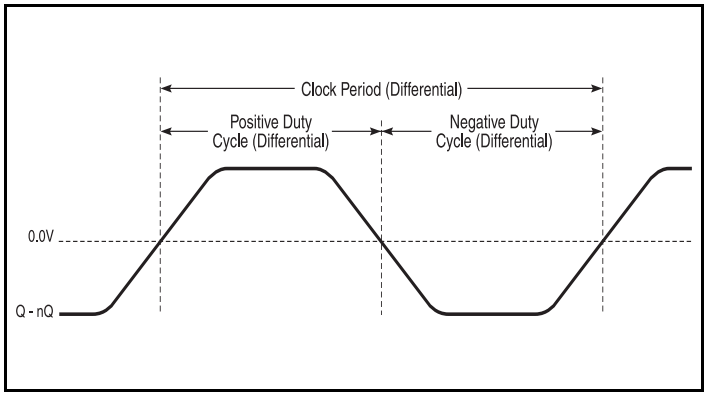
3.3V HCSL Output Load AC Test Circuit



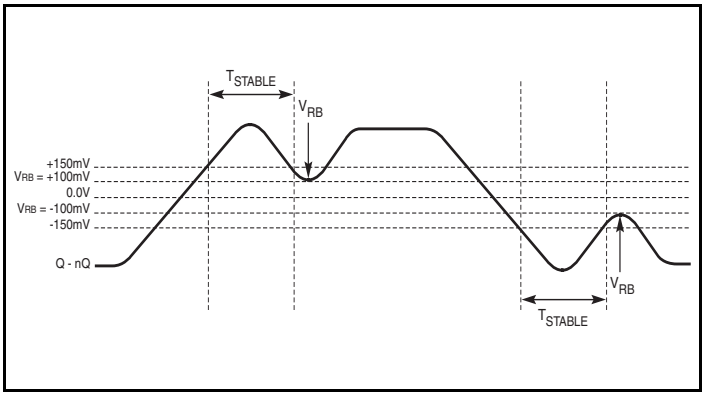
Differential Input Level



Cycle-to-Cycle Jitter

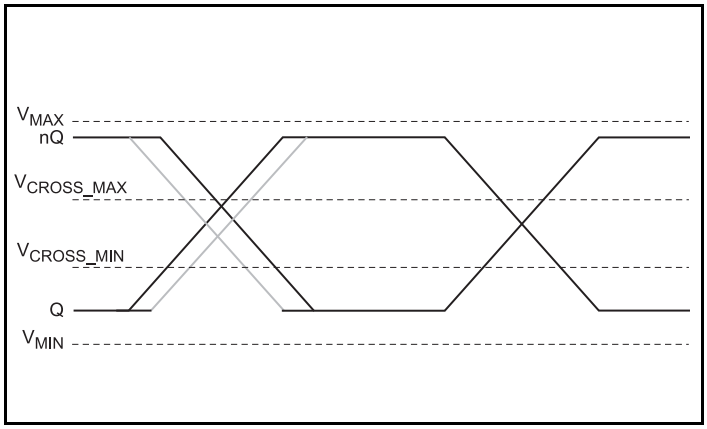


Differential Measurement Points for Duty Cycle/Period

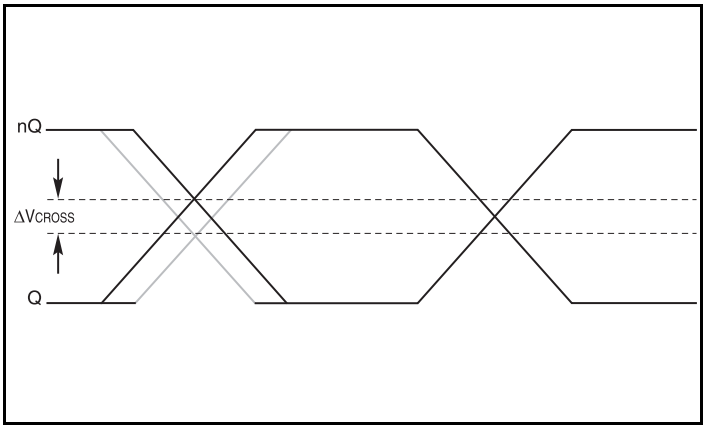


Differential Measurement Points for Ringback

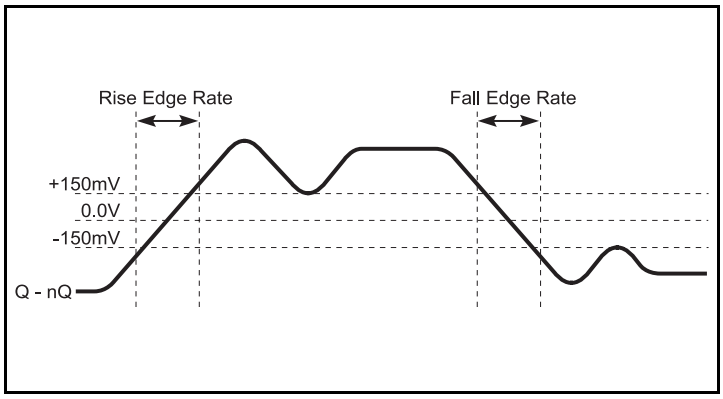
Parameter Measurement Information, continued



Single-ended Measurement Points for Absolute Cross Point and Swing



Single-ended Measurement Points for Delta Cross Point



Output Rise/Fall Time

Application Information

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 871002I-02 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} and V_{DDA} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{DDA} pin.

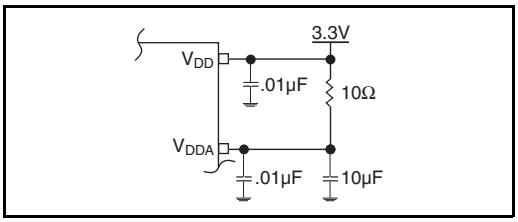


Figure 1. Power Supply Filtering

Wiring the Differential Input to Accept Single-Ended Levels

Figure 2 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{DD}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{DD} = 3.3V, R1 and R2 value should be adjusted to set V_{REF} at 1.25V. The values below are for when both the single ended swing and V_{DD} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{DD} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

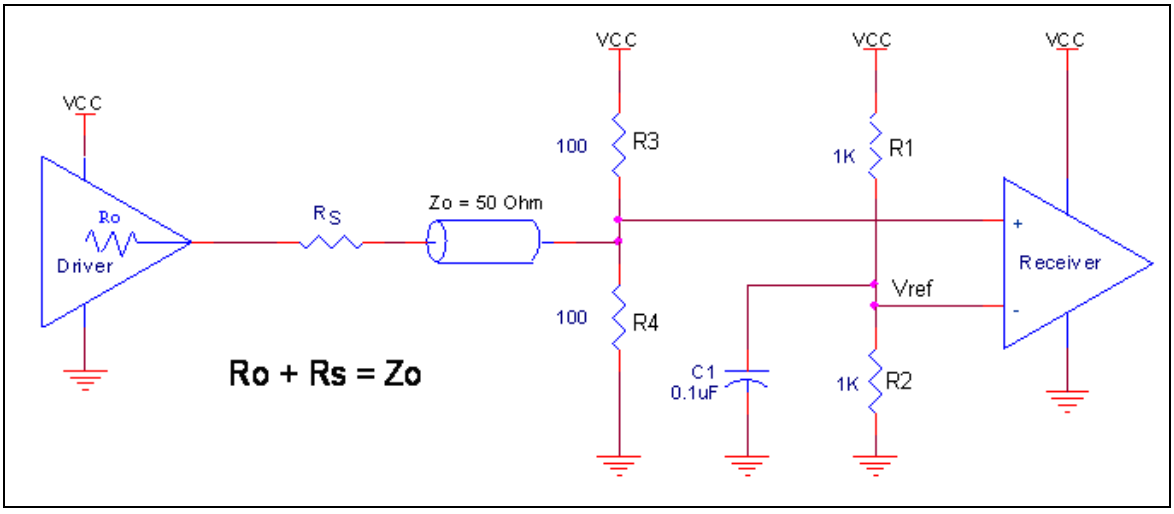
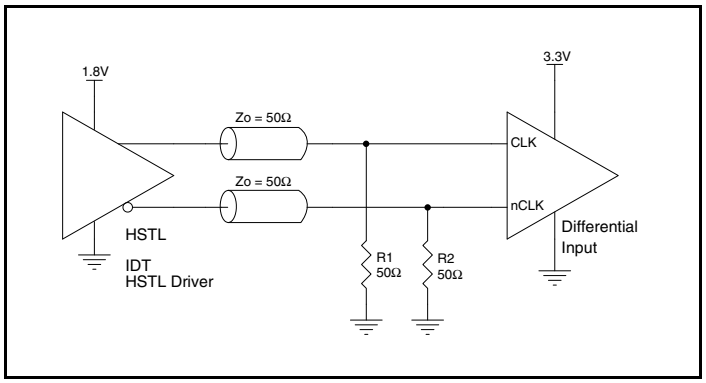


Figure 2. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, HSTL, SSTL, HCSL and other differential signals. The differential signal must meet the V_{PP} and V_{CMR} input requirements. *Figures 3A to 3F* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only.

Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 3A, the input termination applies for IDT open emitter HSTL drivers. If you are using an HSTL driver from another vendor, use their termination recommendation.



3A. CLK/nCLK Input Driven by an IDT Open Emitter HSTL Driver

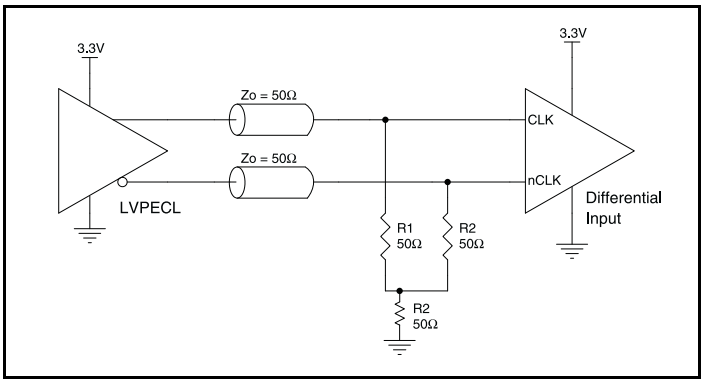


Figure 3B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

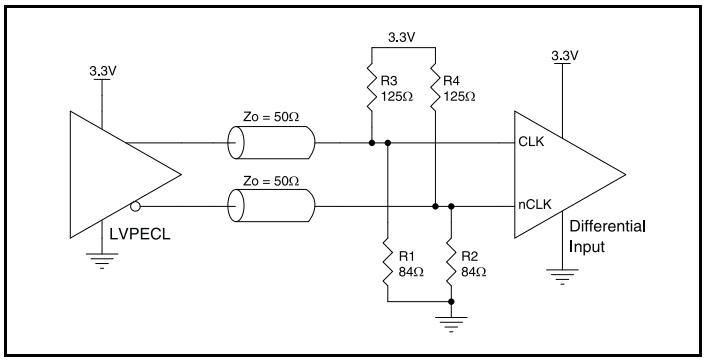


Figure 3C. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

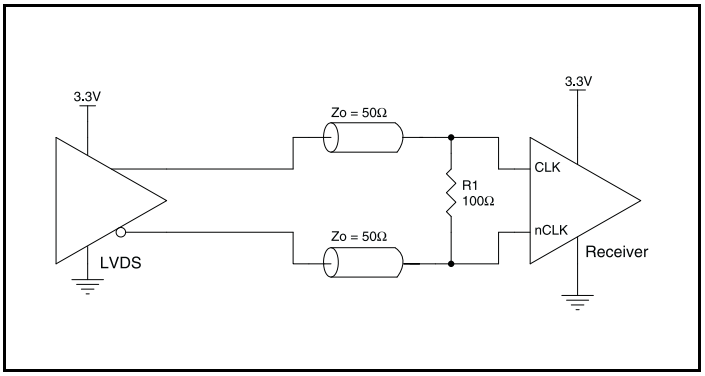


Figure 3D. CLK/nCLK Input Driven by a 3.3V LVDS Driver

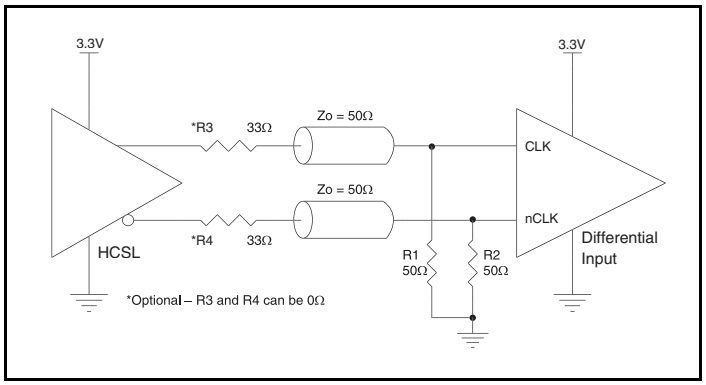


Figure 3E. CLK/nCLK Input Driven by a 3.3V HCSL Driver

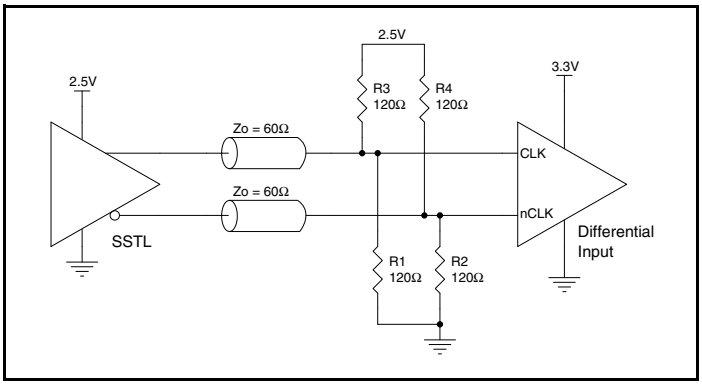


Figure 3F. CLK/nCLK Input Driven by a 2.5V SSTL Driver

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

Differential Outputs

All unused differential outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Recommended Termination

Figure 4A is the recommended termination for applications which require the receiver and driver to be on a separate PCB. All traces should be 50Ω impedance.

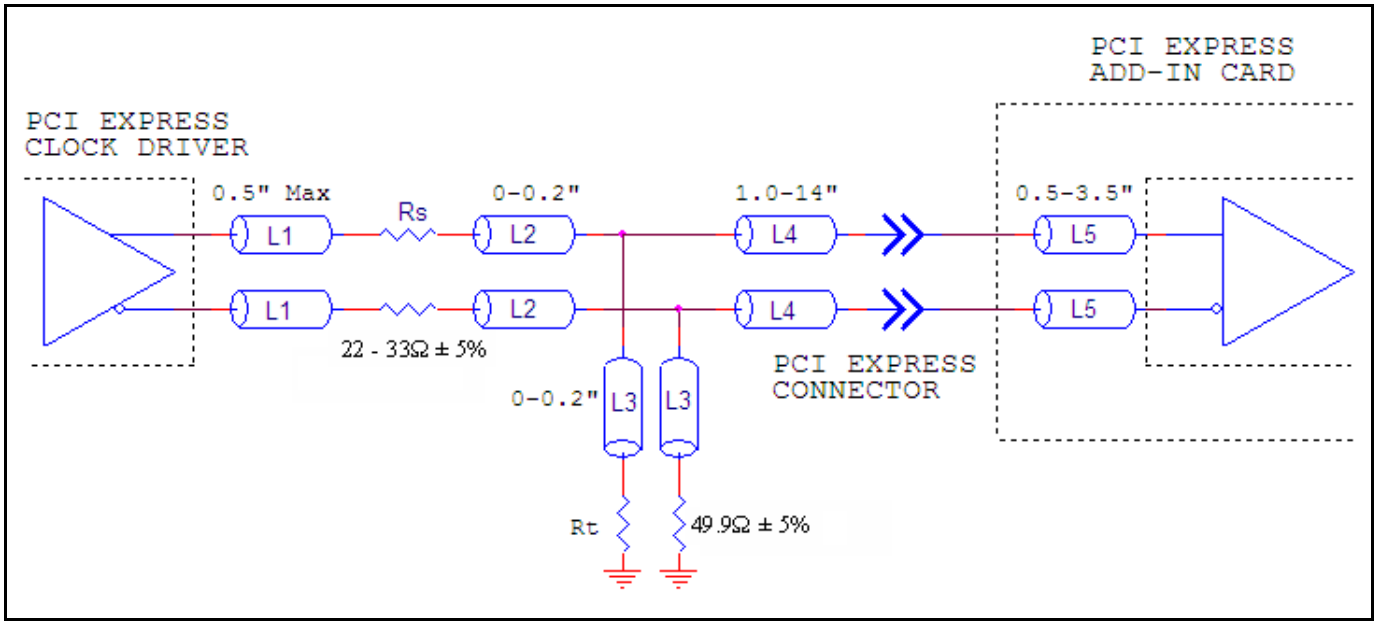


Figure 4A. Recommended Termination

Figure 4B is the recommended termination for applications which require a point to point connection and contain the driver and receiver on the same PCB. All traces should all be 50Ω impedance.

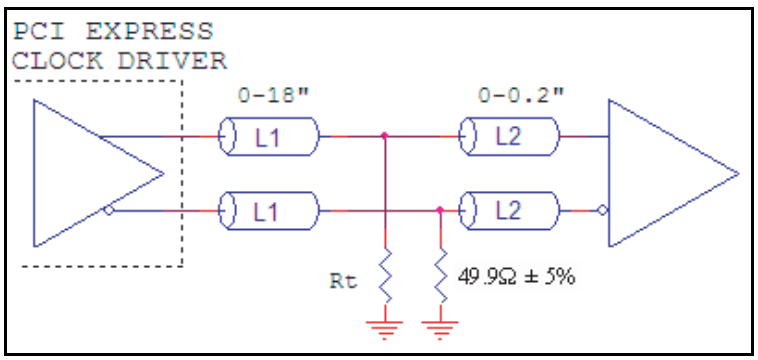


Figure 4B. Recommended Termination

Schematic Layout

Figure 5 shows an example of 871002I-02 application schematic. In this example, the device is operated at V_{DD}= 3.3V. The decoupling capacitors should be located as close as possible to the power pin. The input is driven by a 3.3V LVPECL driver. Two examples of HCSL termination are shown in this schematic.

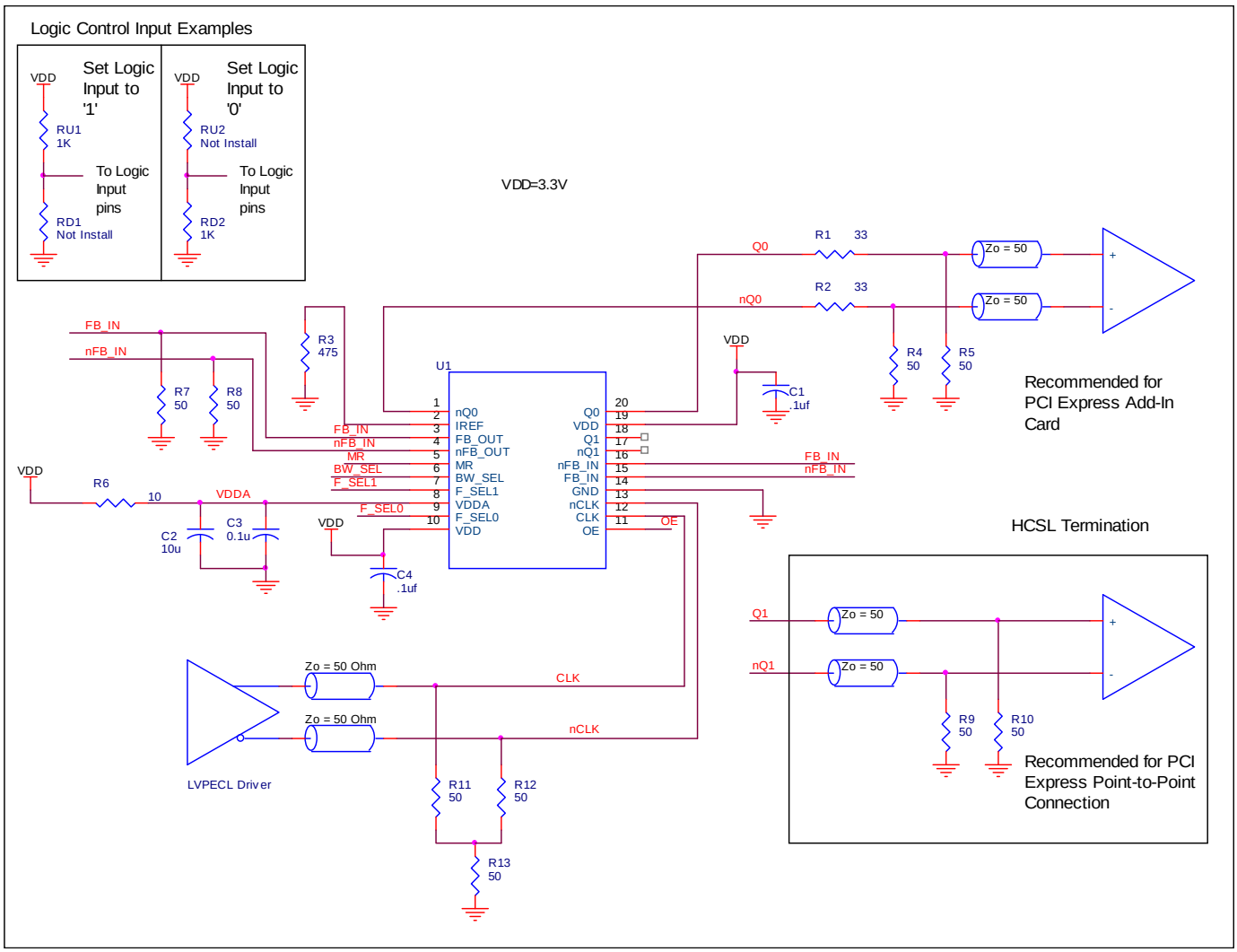


Figure 5. 871002I-02 Schematic Layout

Power Considerations

This section provides information on power dissipation and junction temperature for the 871002I-02.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS71002I-02 is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for V_{DD} = 3.3V + 10% = 3.63V, which gives worst case results.

- Power $(core)_{MAX} = V_{DD\_MAX} * (I_{DD\_MAX} + I_{DDA\_MAX})$ = 3.63V * (75mA + 12mA) = **315.81mW**
- Power $(outputs)_{MAX}$ = **46.8mW/Loaded Output Pair**
  If all outputs are loaded, the total power is 3 * 46.8mW = **140.4mW**

Total Power$_{\_MAX}$ (3.63V, with all outputs switching) = 315.81mW + 140.4mW = **456.21mW**

-

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 86.7°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.456W * 86.7°C/W = 124.6°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 20 Lead TSSOP, Forced Convection

θ_{JA} **by Velocity**			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	86.7°C/W	82.4°C/W	80.2°C/W

The purpose of this section is to calculate power dissipation on the IC per HCSL output pair.

HCSL output driver circuit and termination are shown in *Figure 6.*

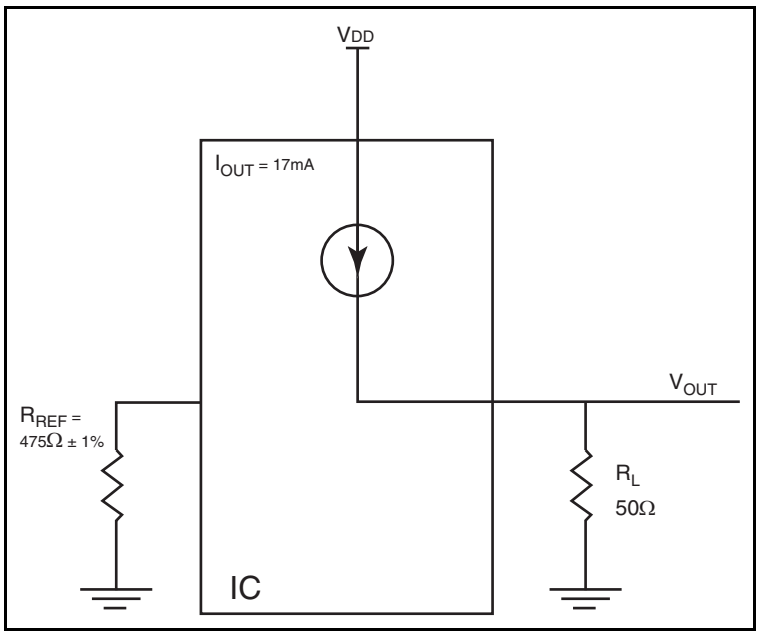


Figure 6. HCSL Driver Circuit and Termination

HCSL is a current steering output which sources a maximum of 17mA of current per output. To calculate worst case on-chip power dissipation, use the following equations which assume a 50Ω load to ground.

The highest power dissipation occurs when V_{DD_MAX}.

Power = $(V_{DD\_MAX} - V_{OUT}) * I_{OUT}$,
since $V_{OUT} - I_{OUT} * R_L$

= $(V_{DD\_MAX} - I_{OUT} * R_L) * I_{OUT}$

= (3.6V – 17mA * 50Ω) * 17mA

Total Power Dissipation per output pair = **46.8mW**

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 20 Lead TSSOP

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	86.7°C/W	82.4°C/W	80.2°C/W

Transistor Count

The transistor count for 871002I-02 is: 1,704

Package Outline and Package Dimensions

Package Outline - G Suffix for 20 Lead TSSOP

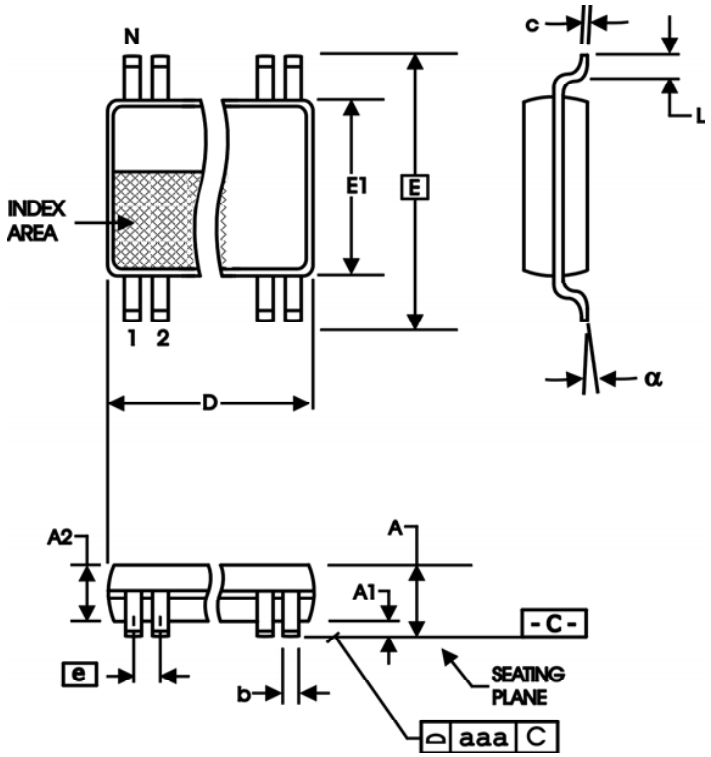


Table 8 Package Dimensions

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	20	
A		1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
871002AGI-02LF	ICS1002AI02L	“Lead-Free” 20 Lead TSSOP	Tube	-40°C to 85°C
871002AGI-02LFT	ICS1002AI02L	“Lead-Free” 20 Lead TSSOP	Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	T9	15	Ordering Information - removed leaded devices. Updated data sheet format.	7/13/15

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