Differential-to-3.3V LVPECL Zero Delay/Multiplier/Divider

873996

DATA SHEET

General Description

The 873996 is a Zero Delay/Multiplier/Divider with hitless input clock switching capability and a member of the family of low jitter/phase noise devices from IDT. The 873996 is ideal for use in redundant, fault tolerant clock trees where low phase noise and low jitter are critical. The device receives two differential LVPECL clock signals from which it generates 6 LVPECL clock outputs with “zero” delay. The output divider and feedback divider selections also allow for frequency multiplication or division.

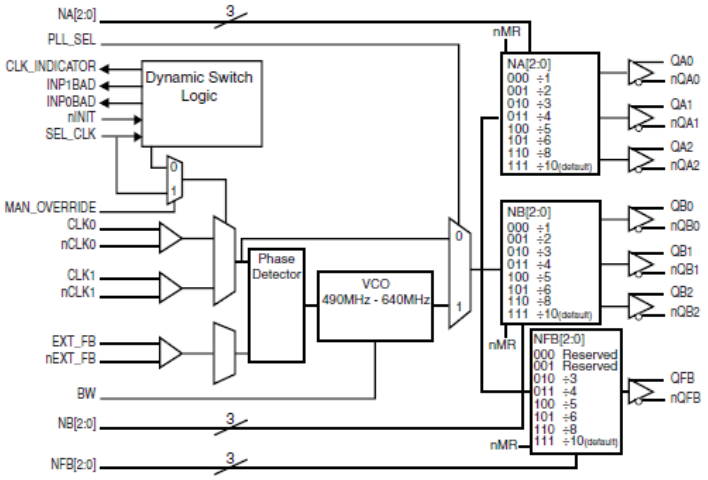
The 873996 Dynamic Clock Switch (DCS) circuit continuously monitors both input clock signals. Upon detection of a failure (input clock stuck LOW or HIGH for at least 1 period), INP_BAD for that clock will be set HIGH. If that clock is the primary clock, the DCS will switch to the good secondary clock and phase/frequency alignment will occur with minimal output phase disturbance.

The low jitter characteristics combined with input clock monitor-ing and automatic switching from bad to good input clocks make the 873996 an ideal choice for mission critical applications that utilize 1G or 10G Ethernet or 1G/4G/10G Fibre Channel.

Features

- Six differential 3.3V LVPECL outputs
- Selectable differential clock inputs
- CLKx, nCLKx pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, HCSL, SSTL
- Input clock frequency range: 49MHz to 213.33MHz
- Output clock frequency range: 49MHz to 640MHz
- VCO range: 490MHz to 640MHz
- External feedback for “zero delay” clock regeneration with configurable frequencies
- Output skew: 100ps (maximum)
- RMS phase jitter (1.875MHz - 20MHz): 0.6ps (typical) assuming a low phase noise reference clock input
- 3.3V supply voltage
- 0°C to 70°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Block Diagram



Pin Assignment

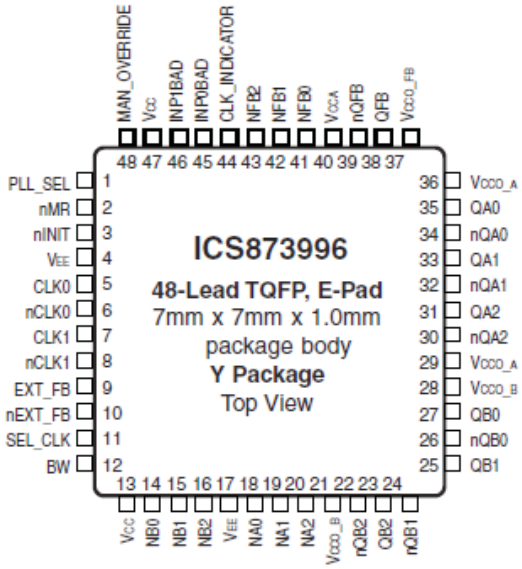


Table 1. Pin Descriptions

Number	Name	Type		Description
1	PLL_SEL	Input	Pullup	Selects between the PLL and reference clock as the input to the dividers. When LOW, selects reference clock.When HIGH, selects PLL. LVCMOS / LVTTL interface levels.
2	nMR	Input	Pullup	Active LOW Master Reset. When logic LOW, the internal dividers are reset causing the true outputs Qx to go low and the inverted outputs nQx to go high. When logic HIGH, the internal dividers and the outputs are enabled. LVCMOS / LVTTL interface levels.
3	nINIT	Input	Pullup	When HIGH-to-LOW, resets the input bad flags and aligns CLK_INDICATOR to SEL_CLK. LVCMOS / LVTTL interface levels.
4, 17	V_{EE}	Power		Negative supply pins.
5	CLK0	Input	Pulldown	Non-inverting differential clock input.
6	nCLK0	Input	Pullup/ Pulldown	Inverting differential clock input. V_{CC}/2 default when left floating.
7	CLK1	Input	Pulldown	Non-inverting differential clock input.
8	nCLK1	Input	Pullup/ Pulldown	Inverting differential clock input. V_{CC}/2 default when left floating.
9	EXT_FB	Input	Pulldown	Differential external feedback.
10	nEXT_FB	Input	Pullup/ Pulldown	Differential external feedback. V_{CC}/2 default when left floating.
11	SEL_CLK	Input	Pulldown	Selects the primary reference clock. When LOW, selects CLK0 as the primary clock source. When HIGH, selects CLK1 as the primary clock source. LVCMOS / LVTTL interface levels.
12	BW	Input	Pullup/ Pulldown	Bandwidth control pin. LVCMOS / LVTTL interface levels. Float (default) = Medium Bandwidth (~800kHz), 1 = High Bandwidth (~2000kHz), 0 = Low Bandwidth (~400kHz).
13, 47	V_{CC}	Power		Core supply pins.
14, 15, 16	NB0, NB1, NB2	Input	Pullup	Bank B output divider control pins LVCMOS / LVTTL interface levels.
18, 19, 20	NA0, NA1, NA2	Input	Pullup	Bank A output divider control pins LVCMOS / LVTTL interface levels.
21, 28	V_{CCO_B}	Power		Output supply voltage for B Bank outputs.
22, 23	nQB2, QB2	Output		Differential output pair. LVPECL interface levels.
24, 25	nQB1, QB1	Output		Differential output pair. LVPECL interface levels.
26, 27	nQB0, QB0	Output		Differential output pair. LVPECL interface levels.
29, 36	V_{CCO_A}	Power		Output supply voltage for A Bank outputs.
30, 31	nQA2, QA2	Output		Differential output pair. LVPECL interface levels.
32, 33	nQA1, QA1	Output		Differential output pair. LVPECL interface levels.
34, 35	nQA0, QA0	Output		Differential output pair. LVPECL interface levels.
37	V_{CCO_FB}	Power		Output supply voltage for FB output.
38, 39	QFB, nQFB	Output		Feedback outputs. LVPECL interface levels.
40	V_{CCA}	Power		Analog supply pin.
41, 42, 43	NFB0, NFB1, NFB2	Input	Pullup	Feedback divider control pins. LVCMOS / LVTTL interface levels.
44	CLK_INDICATOR	Output		Clock indicator pin. When LOW, CLK0, nCLK0 is selected. When HIGH, CLK1, nCLK1 is selected. LVCMOS / LVTTL interface levels.

NOTE: Pullup and Pulldown refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Continued on next page...

Table 1. Pin Descriptions, continued

Number	Name	Type		Description
45	INP0BAD	Output		Indicates detection of a bad input reference clock 0 with respect to the feedback signal. The output is active HIGH. LVCMOS / LVTTL interface levels.
46	INP1BAD	Output		Indicates detection of a bad input reference clock 1 with respect to the feedback signal. The output is active HIGH. LVCMOS / LVTTL interface levels.
48	MAN_OVERRIDE	Input	Pulldown	Manual override. When HIGH, disables internal clock switch circuitry and CLK_INDICATOR will track SEL_CLK. When LOW, Dynamic Clock Switch is enabled. LVCMOS / LVTTL interface levels.

NOTE: and refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Table 3A. Feedback Divider Function Table

NFB[2:0]	Feedback Divider Value	Output Frequency Range
000	1	N/A[NOTE1]
001	2	N/A[NOTE1]
010	3	163.33MHz - 200MHz
011	4	122.5MHz - 160MHz
100	5	98MHz - 128MHz
101	6	81.66MHz - 106.66MHz
110	8	61.25MHz - 80MHz
111	10	49MHz - 64MHz

NOTE 1: The Phase Detector has a maximum frequency limit of 200MHz, so these values cannot be used for feedback. The reason these options are available is for applications that use an output on Bank A or Bank B for feedback and the QFB/nQFB pair for a high frequency output. For example, a user may need two 62.5MHz outputs, three 125MHz outputs and one 625MHz output from a 62.5MHz reference clock. For this case, the user would use one of the Bank A Outputs for feedback and set the bank for /10, and use the other two Bank A Outputs to drive the 2 loads. The Bank B Output Divider would be set for /5, and the Feedback Divider would be set for /1.

Table 3B. NA/NB Bank Divider Function Table

NA[2:0], NB[2:0]	Bank A/B Divider Value	Output Frequency Range
000	1	490MHz - 640MHz
001	2	245MHz - 320MHz
010	3	163.33MHz - 213.33MHz
011	4	122.5MHz - 160MHz
100	5	98MHz - 128MHz
101	6	81.66MHz - 106.66MHz
110	8	61.25MHz - 80MHz
111	10	49MHz - 64MHz

Table 3C. PLL Bandwidth Control Table

Inputs	PLL Band-width	Description
BW		
0	~400kHz	LOW (L)
1	~2000kHz	HIGH (H)
Float (default)	~800kHz	Medium (M)

Absolute Maximum Ratings

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5 V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	47.9°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{CC} = V_{CCO\_A} = V_{CCO\_B} = V_{CCO\_FB} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0°C$ to $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		V_{CC} – 0.15	3.3	V_{CC}	V
$V_{CCO\_A, \_B, \_FB}$	Output Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				300	mA
I_{CCA}	Analog Supply Current				15	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, $V_{CC} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0°C$ to $70°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	LVCMOS Inputs		2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	LVCMOS Inputs		-0.3		0.8	V
I_{IH}	Input High Current	NA[2:0], NB[2:0], NFB[2:0], PLL_SEL, nINIT, nMR, BW	$V_{IN} = V_{CC} = 3.465V$			5	µA
		SEL_CLK, BW MAN_ OVERRIDE	$V_{IN} = V_{CC} = 3.465V$			150	µA
I_{IL}	Input Low Current	NA[2:0], NB[2:0], NFB[2:0], PLL_SEL, nINIT, nMR, BW	$V_{IN} = 0V$, $V_{CC} = 3.465V$	-150			µA
		SEL_CLK, BW, MAN_ OVERRIDE	$V_{IN} = 0V$, $V_{CC} = 3.465V$	-5			µA

Table 4C. Differential DC Characteristics, $V_{CC} = V_{CCO\_A} = V_{CCO\_B} = V_{CCO\_FB} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0°C$ to $70°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK0, CLK1, EXT_ FB	$V_{IN} = V_{CC} = 3.465V$			150	µA
		nCLK0, nCLK1, nEXT_FB	$V_{IN} = V_{CC} = 3.465V$			150	µA
I_{IL}	Input Low Current	CLK0, CLK1, EXT_ FB	$V_{IN} = 0V$, $V_{CC} = 3.465V$	-5			µA
		nCLK0, nCLK1, nEXT_FB	$V_{IN} = 0V$, $V_{CC} = 3.465V$	-150			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			V_{EE} + 0.5		V_{CC} - 0.85	V

NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single ended appliations, the maximum input voltage for CLKx, nCLKx is V_{CC} + 0.3V.

TABLE 4D. LVPECL DC CHARACTERISTICS, $V_{CC} = V_{CCO\_A} = V_{CCO\_B} = V_{CCO\_FB} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CCO_X} - 1.4		V_{CCO_X} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CCO_X} - 2.0		V_{CCO_X} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

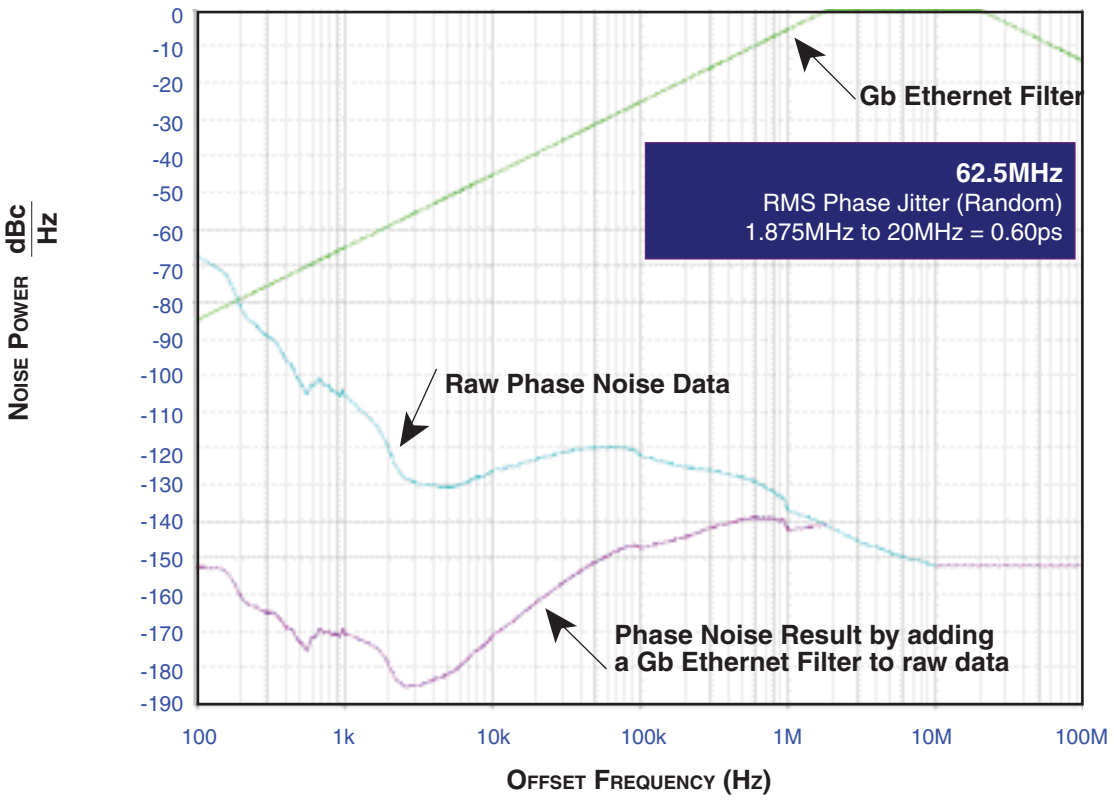
NOTE 1: Outputs terminated with 50W to VCCO_A, _B, _FB = - 2V.

TABLE 5. AC CHARACTERISTICS, $V_{CC} = V_{CCO\_A} = V_{CCO\_B} = V_{CCO\_FB} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0°C$ TO $70°C$

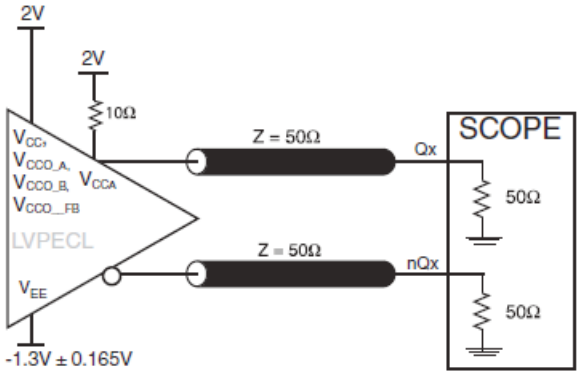
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{VCO}	PLL VCO Lock Range			490		640	MHz
t(Ø)	Static Phase Offset; NOTE 2		PLL_SEL = HIGH	-35		75	ps
tjit(ø)	RMS Phase Jitter (Random); NOTE 7		BW = HIGH		0.6		ps
tsk(o)	Output Skew; NOTE 3					100	ps
tsk(b)	Bank Skew; NOTE 4					80	ps
$D_{PER/CYCLE}$	Rate of change of Periods	62.5MHz Output; NOTE 1, 5	BW = L		30		ps/cycle
			BW = H		55		ps/cycle
			BW = M		40		ps/cycle
		125MHz Output; NOTE 1, 5	BW = L		60		ps/cycle
			BW = H		110		ps/cycle
			BW = M		80		ps/cycle
		62.5MHz Output; NOTE 1, 6	BW = L		45		ps/cycle
			BW = H		60		ps/cycle
			BW = M		55		ps/cycle
		125MHz Output; NOTE 1, 6	BW = L		90		ps/cycle
			BW = H		120		ps/cycle
			BW = M		110		ps/cycle
odc	Output Duty Cycle		M > 2	47		53	%
			M = 2	45		55	%
			M = 1	40		60	%
t_R / t_F	Output Rise/Fall Time		20% to 80%	250		600	ps

All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: These parameters are guaranteed by characterization. Not tested in production.
NOTE 2: Defined as the time difference between the input reference clock and the average feedback input signal, when the PLL is locked and the input reference frequency is stable.
NOTE 3: Defined as skew within a bank of outputs at the same voltages and with equal load conditions.
NOTE 4: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 5: Specification holds for a clock switch between two signals no greater than 400ps out of phase. Delta period change per cycle is averaged over the clock switch excursion.
NOTE 6: Specification holds for a clock switch between two signals greater than 400ps out of phase. Delta period change per cycle is averaged over the clock switch excursion.
NOTE 7: Please refer to the Phase Noise Plot.

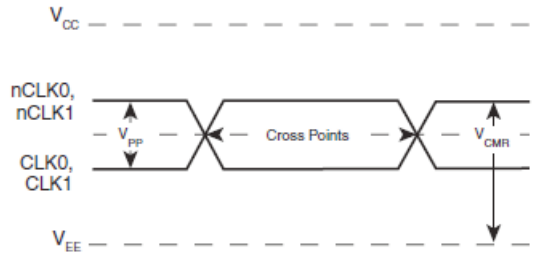
Typical Phase Noise at 62.5MHz



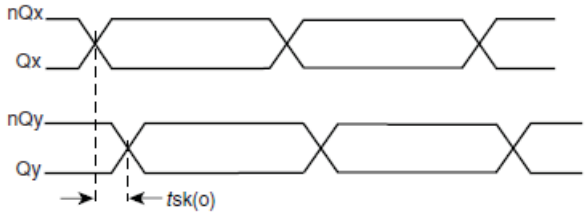
Parameter Measurement Information



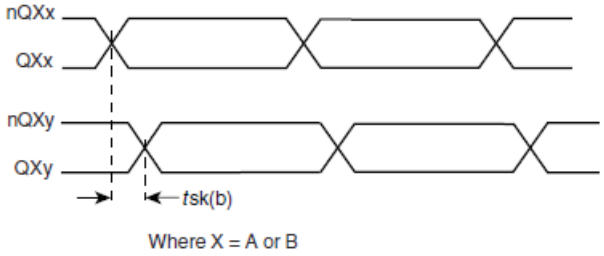
3.3V Output Load AC Test Circuit



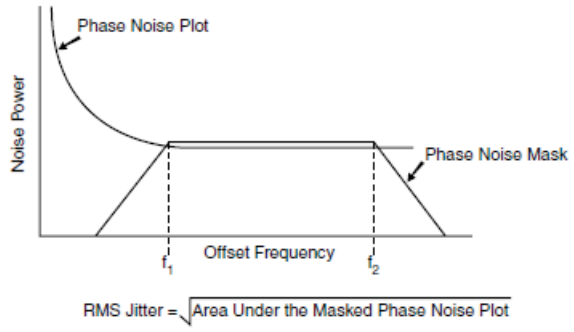
Differential Input Level



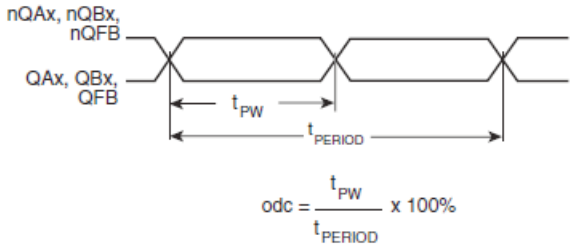
Output Skew



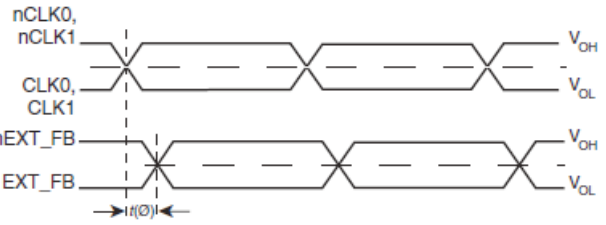
Bank Skew



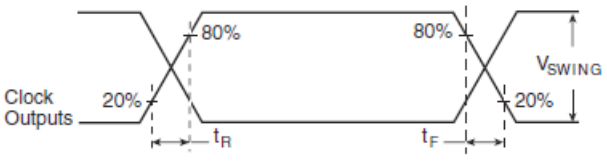
RMS Phase Jitter



Output Duty Cycle/Pulse Width/Period



Static Phase Offset



Output Rise/Fall Time

Applications Information

Clock Redundancy and Reference Selection

The 873996 accepts two differential input clocks, CLK0/nCLK0 and CLK1/nCLK1, for the purpose of redundancy. Only one of these clocks can be selected at any given time for use as the reference. One clock will be defined during the initialization process as the initial, or primary clock, while the remaining clock is the redundant or secondary clock. During the initialization process, input signal SEL_CLK determines which input clock will be used as the initial clock. When SEL_CLK is driven HIGH, the initial clock to be used as the reference is CLK1/nCLK1, otherwise an internal pulldown pulls this input LOW so that the initial clock input is CLK0/nCLK0. The output signal CLK_INDICATOR indicates which clock input is being used as the reference (LOW = CLK0/nCLK0, HIGH = CLK1/nCLK1), and will initially be at the same level as SEL_CLK.

Initialization Event

An initialization event is required to specify the initial input clock. In order to run an initialization event, nINIT must transition from HIGH-to-LOW. Following a HIGH-to-LOW transition of nINIT, the input clock specified on the SEL_CLK input will be set as the initial input clock. In addition, both input-bad flags (INP0BAD and INP1BAD outputs) will be cleared.

Falilure Detection and Alarm Signaling

Within the 873996 device, CLK0/nCLK0 and CLK1/nCLK1 are continuously monitored for failures. A failure on either of these clocks is detected when one of the clock signals is stuck HIGH or LOW for at least 1 period of the Feedback. Upon detection of a failure, the corresponding input-bad signal, INP0BAD or INP1BAD, will be set HIGH. The input clocks are continuously monitored and the input-bad signals will continue to reflect the real-time status of each input clock.

Manual Clock Switching

When input signal MAN_OVERRIDE is driven HIGH, the clock specified by SEL_CLK will always be used as the reference, even when a clock failure is detected at the reference. In order to switch between CLK0/nCLK0 and CLK1/nCLK1 as the reference clock, the level on SEL_CLK must be driven to the appropriate level. When the level on SEL_CLK is changed, the selection of the new clock will take place, and CLK_INDICATOR will be updated to indicate which clock is now supplying the reference to the PLL.

Dynamic Clock Switching

The Dynamic Clock Switching (DCS) process serves as an automatic safety mechanism to protect the stability of the PLL when a failure occurs on the reference.

When input signal MAN_OVERRIDE is not driven HIGH, an internal pulldown pulls it LOW so that DCS is enabled. If DCS is enabled and a failure occurs on the initial clock, the 873996 device will check the status of the secondary clock. If the secondary clock is detected as a good input clock, the 873996 will automatically deselect the initial clock as the reference and multiplex in the secondary clock. When a successful switch from the initial to secondary clock has been accomplished, CLK_INDICATOR will be updated to indicate the new reference. If and when the fault on the initial clock is corrected, the corresponding input bad flag will be updated to represent this clock as good again. However, the DCS will not undergo an unneccessary clock switch as long as the secondary clock remains good. If, at a later time, a failure occurs on the secondary clock, the 873996 will then switch to the initial clock if it is detected as good. See the Dynamic Clock Switch State Diagram (page 10) and for additional details on the functionality of the Dynamic Clock Switching circuit.

Output Transitioning

After a successful manual or DCS initiated clock switch, the internal PLL of the 873996 will begin slewing to phase/frequency alignment. The PLL will achieve lock to the new input with minimal phase disturbance at the outputs.

Master Reset Operation

When the input signal is driven LOW, the internal dividers of the 873996 are reset causing the true outputs, Qx, to go LOW and the inverted outputs, nQx, to go HIGH. With no signal driving nMR, an internal pullup pulls nMR HIGH and the output clocks and internal dividers are enabled.

Recommended Power-up Sequence

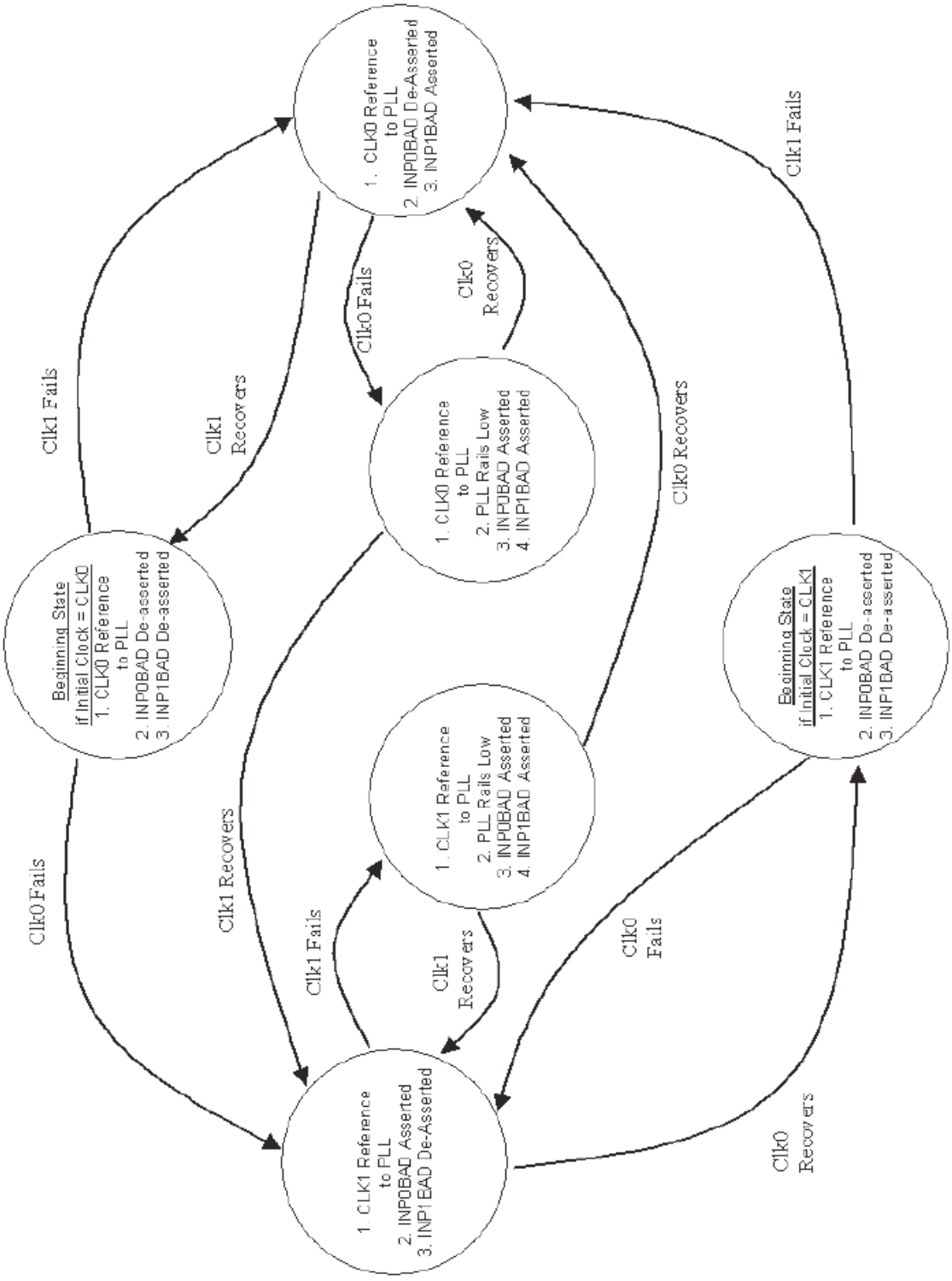
1. Before startup, set MAN_OVERRIDE HIGH and set SEL_CLK to the desired input clock. This will ensure that, during startup, the PLL will acquire lock using the input clock specified by SEL_CLK.
2. Once powered-up, and assuming a stable clock free of failures is present at the clock designated by SEL_CLK, the PLL will begin to phase/frequency slew as it attempts to achieve lock with the input reference clock.
3. Drive MAN_OVERRIDE LOW to enable DCS mode.
4. Transition nINIT from HIGH-to-LOW in order to clear both input-bad flags and to set the initial input clock.

Alternate Power-up Sequence

If both input clocks are valid before power up, the part may be powered-up in DCS mode. However, it cannot be guaranteed that the PLL will achieve lock with one specific input clock.

1. Before startup, leave MAN_OVERRIDE floating and the internal pulldown will enable DCS mode.
2. Once powered up, the PLL will begin to phase/frequency slew as it attempts to achieve lock with one of the input reference clocks.
3. Transition nINIT from HIGH-to-LOW in order to clear both input-bad flags and to set the initial input clock.

873996 STATE DIAGRAM



Power Supply Filtering Techniques

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 873996 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC}, V_{CCA} and V_{CCOx} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{CC} pin and also shows that V_{CCA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{CCA} pin.

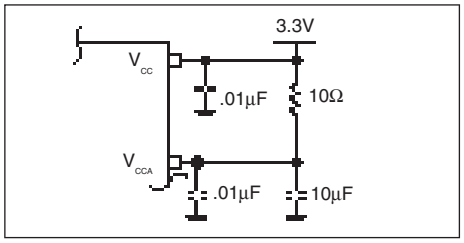


Figure 1. Power Supply Filtering

Wiring the Differential Input to Accept Single Ended Levels

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{CC}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{CC} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

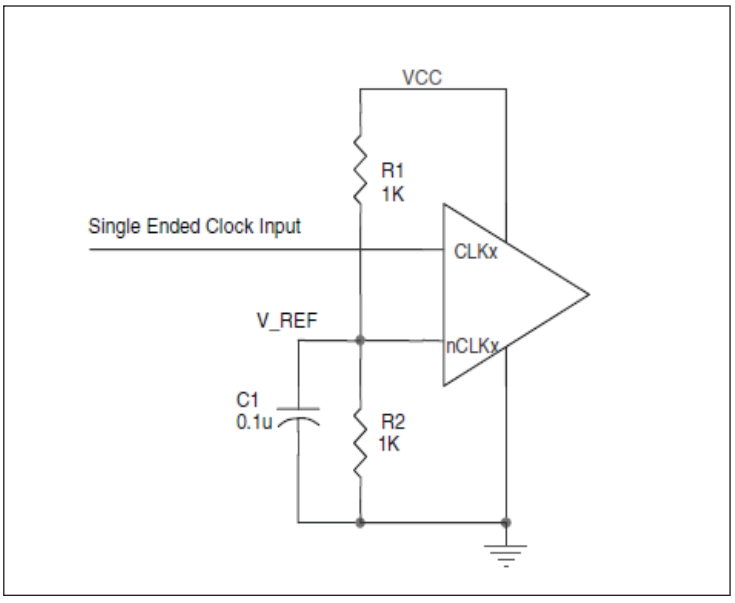


Figure 2. Single Ended Signal Driving Differential Input

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 3A to 3F* show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only.

Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in Figure 3A, the input termination applies for IDT HiPerClockS open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

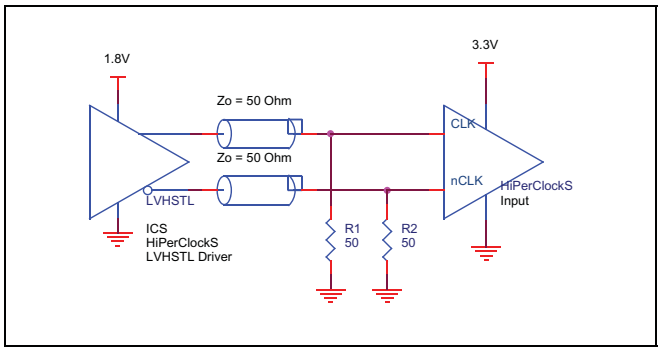


Figure 3A. HiPerClockS CLK/nCLK Input Driven by an IDT Open Emitter HiPerClockS LVHSTL Driver

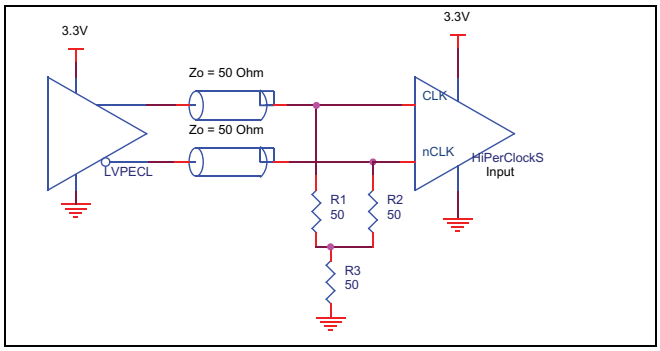


Figure 3B. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver

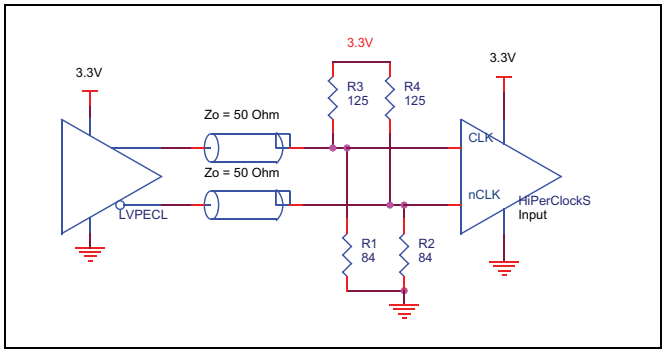


Figure 3C. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver

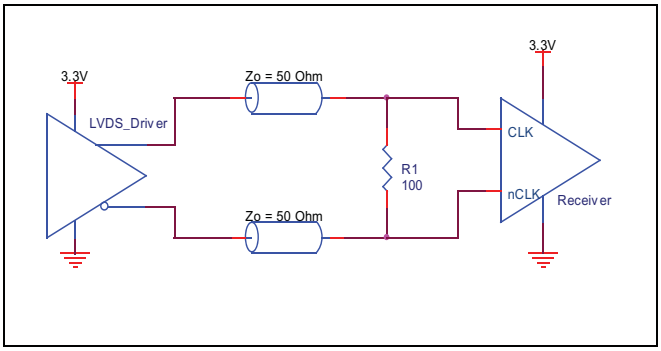


Figure 3D. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVDS Driver

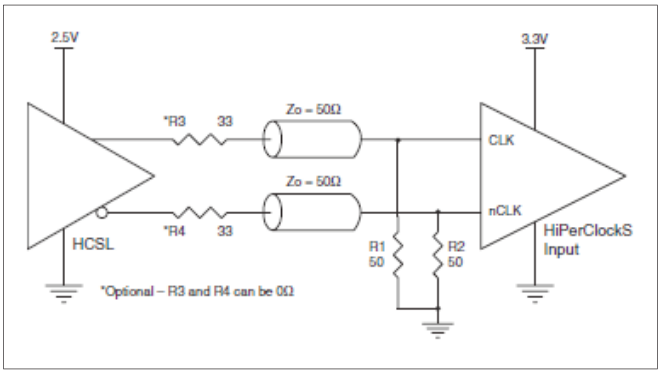


Figure 3E. HiPerClockS CLK/nCLK Input Driven by a 3.3V HCSL Driver

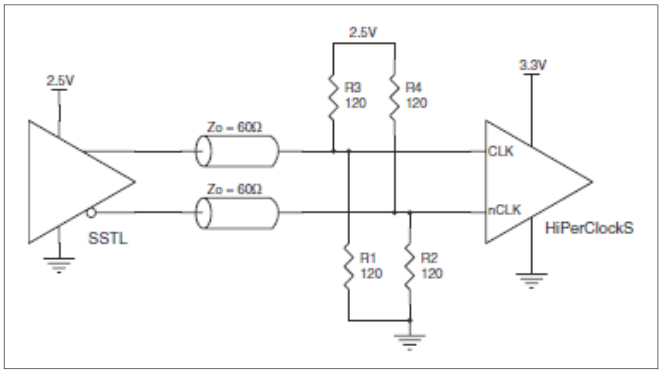


Figure 3F. HiPerClockS CLK/nCLK Input Driven by a 2.5V SSTL Driver

Recommendations for Unused Input and Output Pins

Inputs:

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Termination for LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

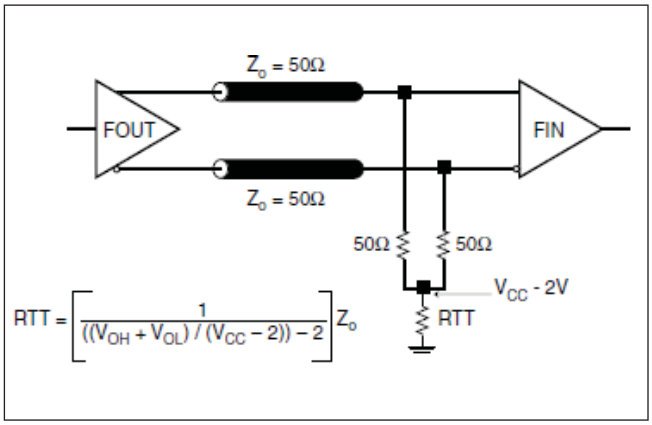


Figure 4A. LVPECL Output Termination

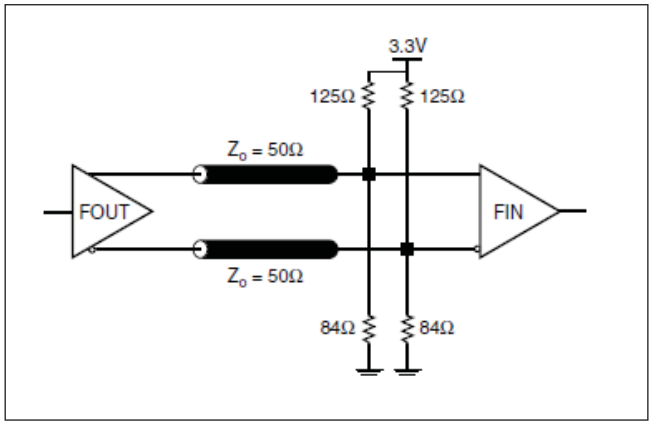


Figure 4B. LVPECL Output Termination

EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 5.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as "heat pipes". The number of vias (i.e. "heat pipes") are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor's Thermally/Electrically Enhance Leadfame Base Package, Amkor Technology.

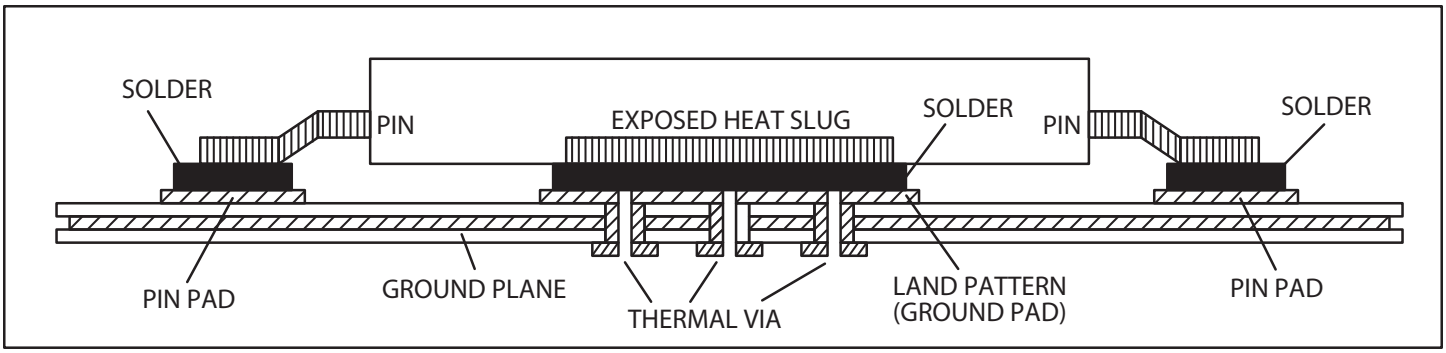


Figure 5. Assembly for Exposed Pad Thermal Release Path –Side View (Drawing not to Scale)

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the 873996.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the 873996 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.465V * 300mA = **1039.5mW**
- Power $(outputs)_{MAX}$ = **30mW/Loaded Output pair**
  If all outputs are loaded, the total power is 6 * 30mW = **180mW**

Total Power $_{MAX}$ (3.465V, with all outputs switching) = 1039.5mW + 180mW = **1219.56mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)
T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 1 meter per second and a multi-layer board, the appropriate value is 25.8°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:
70°C + 1.220W * 25.8°C/W = 101.5°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 48-PIN TQFP, E-PAD FORCED CONVECTION

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	31.8°C/W	25.8°C/W	24.2°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 6.*

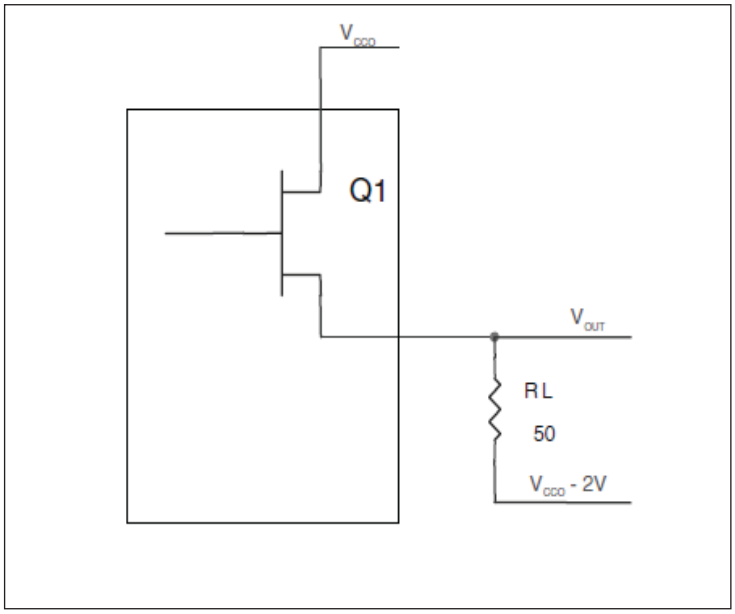


FIGURE 6. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CCO\_MAX} - 0.9V}$

  $(V_{CCO\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CCO\_MAX} - 1.7V}$

  $(V_{CCO\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.9V)/50\Omega] * 0.9V =$ **19.8mW**

$Pd\_L = [(V_{OL\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.7V)/50\Omega] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for 48 Lead TQFP, E-Pad

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	31.8°C/W	25.8°C/W	24.2°C/W

Transistor Count

The transistor count for 873996 is: 5969

Package Outline - Y Suffix for 48 Lead TQFP, E-Pad

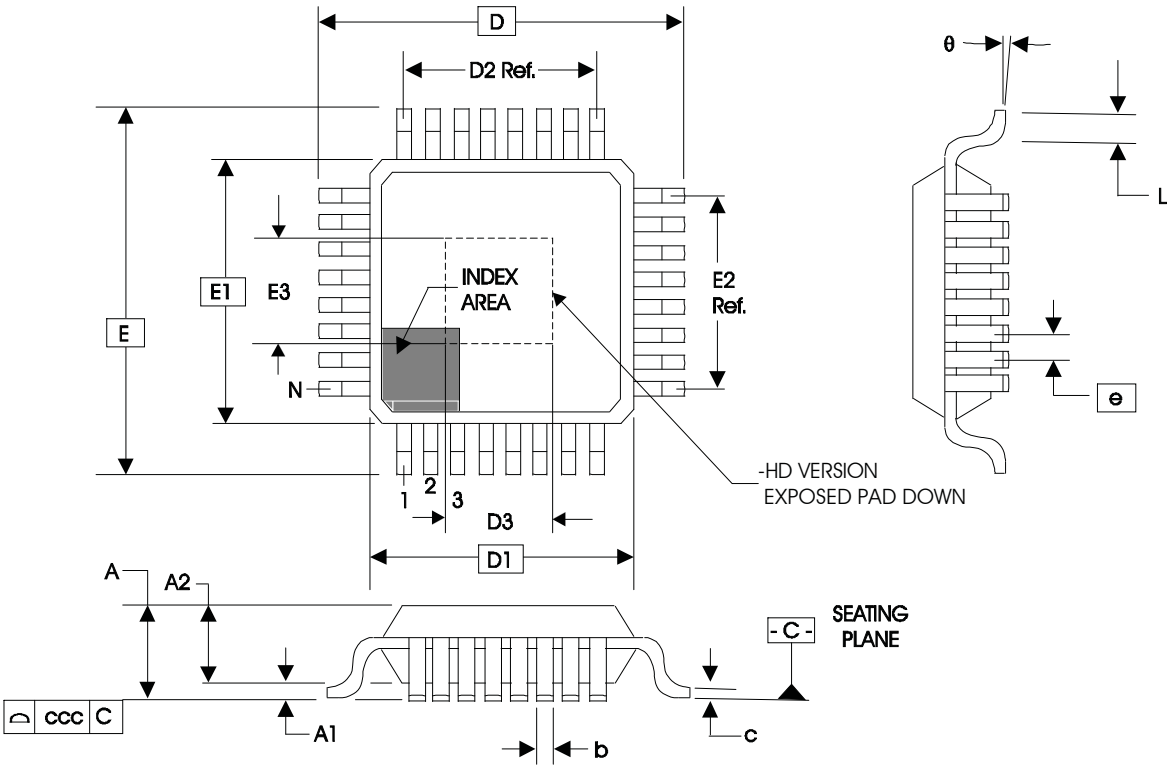


Table 8. Package Dimensions

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	**ABC - HD**		
	MINIMUM	**NOMINAL**	**MAXIMUM**
N		48	
A	--	--	1.20
A1	0.05	--	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
c	0.09		0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.50 BASIC	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.50 BASIC	
e		0.5 BASIC	
L	0.45	0.60	0.75
θ	0°		7°
ccc	--	--	0.08
D3 & E3	3.5		4.5

Reference Document: JEDEC Publication 95, MS-026

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
873996AYLF	ICS873996AYL	48 Lead “Lead-Free” TQFP, E-Pad	tray	0°C to 70°C
873996AYLFT	ICS873996AYL	48 Lead “Lead-Free” TQFP, E-Pad	tape & reel	0°C to 70°C

NOTE: Parts that are ordered with an “LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
A	 T8	12 14 18	Updated Differential Clock Input Interface. Updated Thermal Release Path section. Package Dimensions - corrected D3 & E3.	2/19/08
A	T9	19	Ordering Information - removed leaded devices. Updated data sheet format.	11/10/15

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